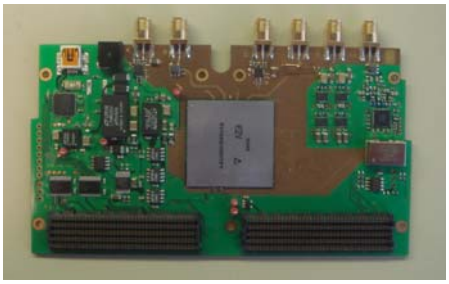
EV10AQ190-DK
Demo Kit Quad10 ADC

Demo Kit Summary

Main Features



- Demonstrator Board with VITA57 Standard Connectors
- Quad ADC with 10-bit Resolution
  - 1.25 Gsps Sampling Rate in 4-channel Mode(1)
  - 2.5 Gsps Sampling Rate in 2-channel Mode(1)
  - 5 Gsps Sampling Rate in 1-channel Mode(1)
  - Built-in 4 to 4 Cross Point Switch
- On Board PLL Generated 2 GHz Clock
- External Clock
- Four Analog Inputs with Different Configurations
  - Differential Driver (AC or DC Coupling)
  - Balun RF Transformer
  - Direct Input
- Full Compatibility with Xilinx ML605 Development Kit
- Control and Acquisition Display Using P.C. Based GUI
  - FFT Computation (PC Software Provided)
  - Flexible and Easy to Operate via USB2 (PC Software Provided without any License)
  - Monitoring of ADC Currents and Junction Temperature
- +12V Supply Adaptor Supplied

Operating Conditions

- Temperature Range: $10°C < T_{amb} < 40°C$
- Operating with a Microsoft Windows PC environment (Windows 2000, Windows XP, Windows Vista) via USB interface

Applications

- Demonstration and Evaluation of EV10AQ190 quad 10 bit analog to digital converter

Note: 1. Due to an input speed limitation of the ML605 the maximum data rate is 1 Gbps which limits the sampling rates to 1, 2 and 4 Gsps. If a higher speed grade FPGA is used the above sampling rates apply.

Visit our website: www.e2v.com
for the latest version of the datasheet

1. General Overview

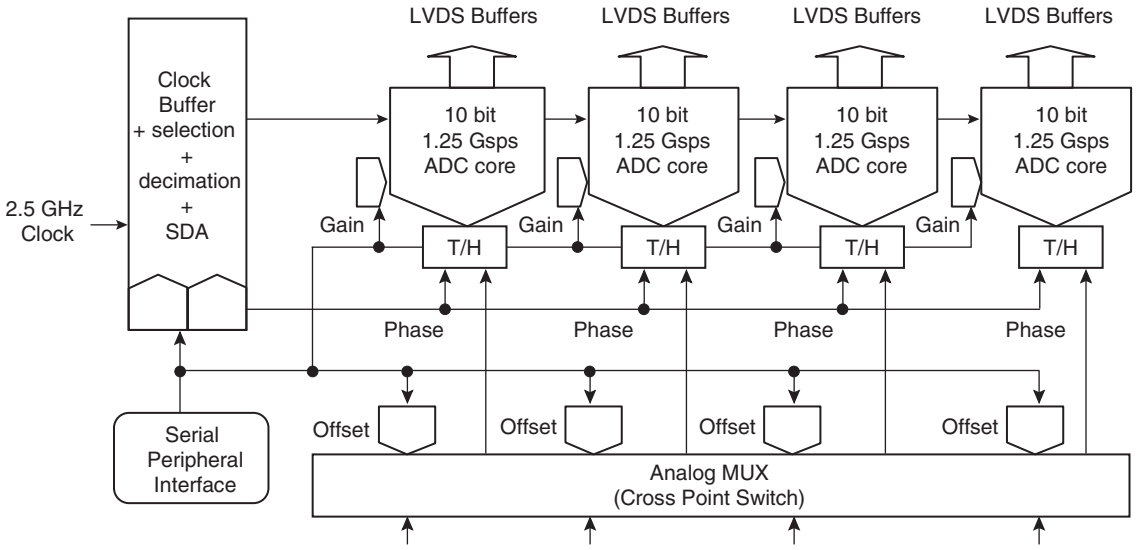
The QUAD 10bit Demo Kit enables the easy evaluation of the characteristics and performance of ADC QUAD 10bit EV10AQ190. The Demo kit is plug_and_play and needs little external equipment. The Demo kit is delivered with software which allows acquisition of data using the FPGA.

The QUAD 10bit Demo Kit is compatible with VITA57 FMC (FPGA Mezzanine Card) standard. The Demo kit QUAD 10bit is 100% compatible with XILINX VIRTEX 6 evaluation kit ML605.

This board is designed for use as a reference design. All front end devices are fitted including: DC-DC regulator, ADC driver, clock generator….
The FPGA VHDL data acquisition code for the ML605 board is supplied.

2. EV10AQ190 Block Diagram

Figure 2-1. Simplified Block Diagram



3. EV10AQ190 Description

The Quad ADC integrates four 10-bit ADC cores which can operate independently (4-channel mode) or grouped by 2 cores (2-channel mode with the ADCs interleaved two by two or 1-channel mode where all four ADCs are all interleaved).

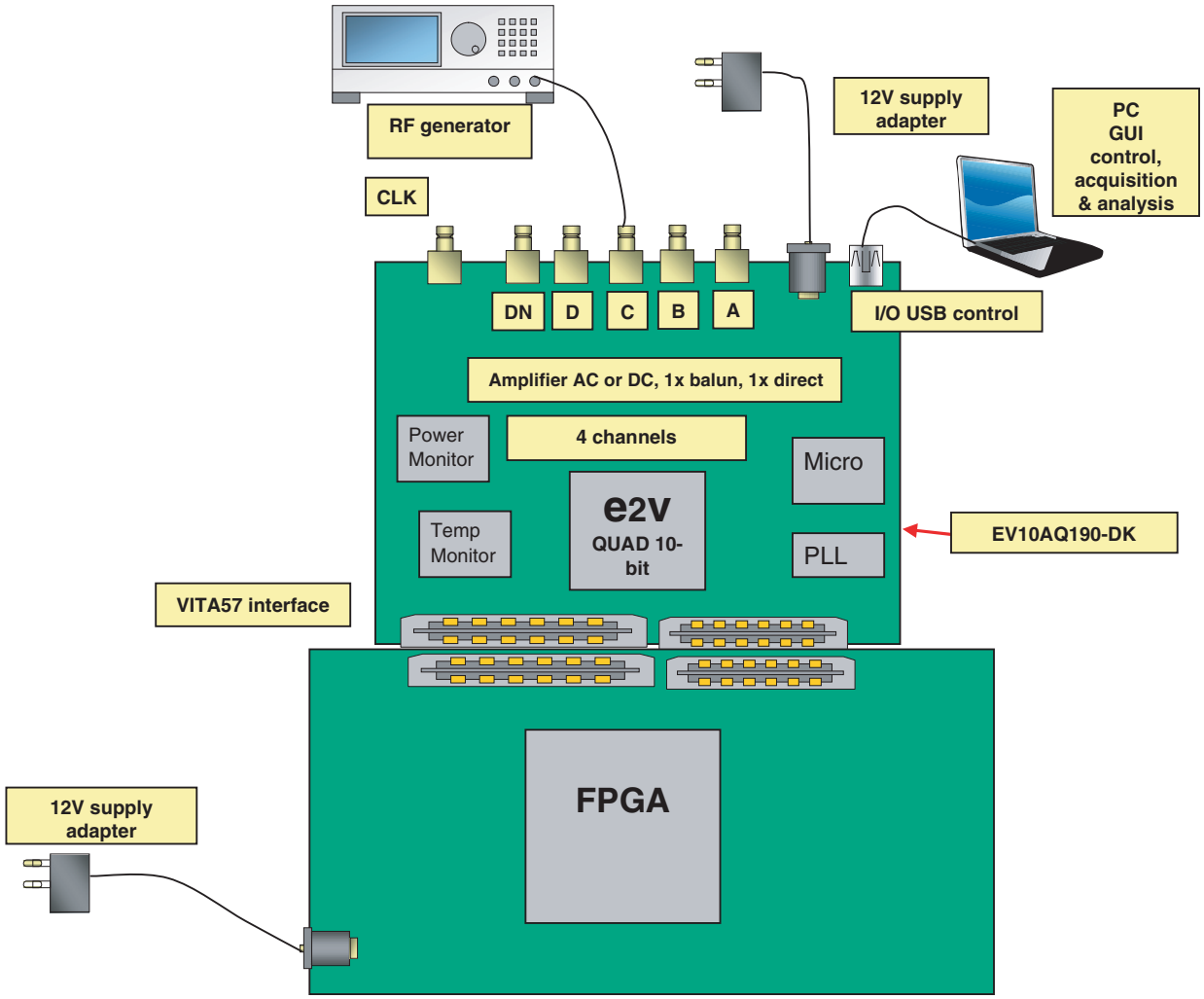
All four ADCs are clocked by the same external input clock signal and controlled via an SPI (Serial Peripheral Interface). An analog multiplexer (Cross point Switch) is used to select the analog input depending on the mode the Quad ADC is used.

The Clock Circuit is common to all four ADCs. This block receives an external 2 GHz clock (maximum frequency using FPGA evaluation board ML605) and preferably a low jitter symmetrical signal. In this block, the external clock signal is then divided by two in order to generate the internal sampling clocks:

- in 4-channel mode, the same 1 GHz clock is directed to all four ADC cores and T/H;
- in 2-channel mode, the in-phase 1 GHz clock is sent to ADC A or C and the inverted 1 GHz clock is sent to ADC B or D, while the analog input is sent to both ADCs, resulting in an interleaved mode with an equivalent sampling frequency of 2 Gsps.

- in 1-channel mode, the in-phase 1 GHz clock is sent to ADC A while the inverted 1 GHz clock is sent to ADC B, the in-phase 1 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 4 Gsps.

Figure 3-1. EV10AQ190-DK Demo Kit System Architecture (When Connected with a VIRTEX6 Evaluation Kit)



The complete system is built with the e2v demo kit and an FPGA development kit.

e2v Demo kit contains the following items:

- Quad 10-bit Demo kit with EV10AQ190CTPY
- Cables & Power Supply
  - Universal 12V power Adapter & Cables
  - USB Cable to communicate with a PC (control of ADC settings and settings for data acquisition)
- Four analog inputs with SMA connectors
- One clock input with SMA connector (if external clock input is programming)

- 2 SAMTEC MC-HPC-8.5L connectors HPC (High Pin Count) compatible with VITA57 standard for ADC LVDS digital outputs
- CD ROM with GUI Software

Note: The ML605 VIRTEX 6 Evaluation kit with XC6VVLX240T-1FFG1156 FPGA is not supplied within the e2v kit and should be purchased separately from Xilinx or its authorized distributors.

Figure 3-2. EV10AQ190-DK Demo Kit Simplified Schematic

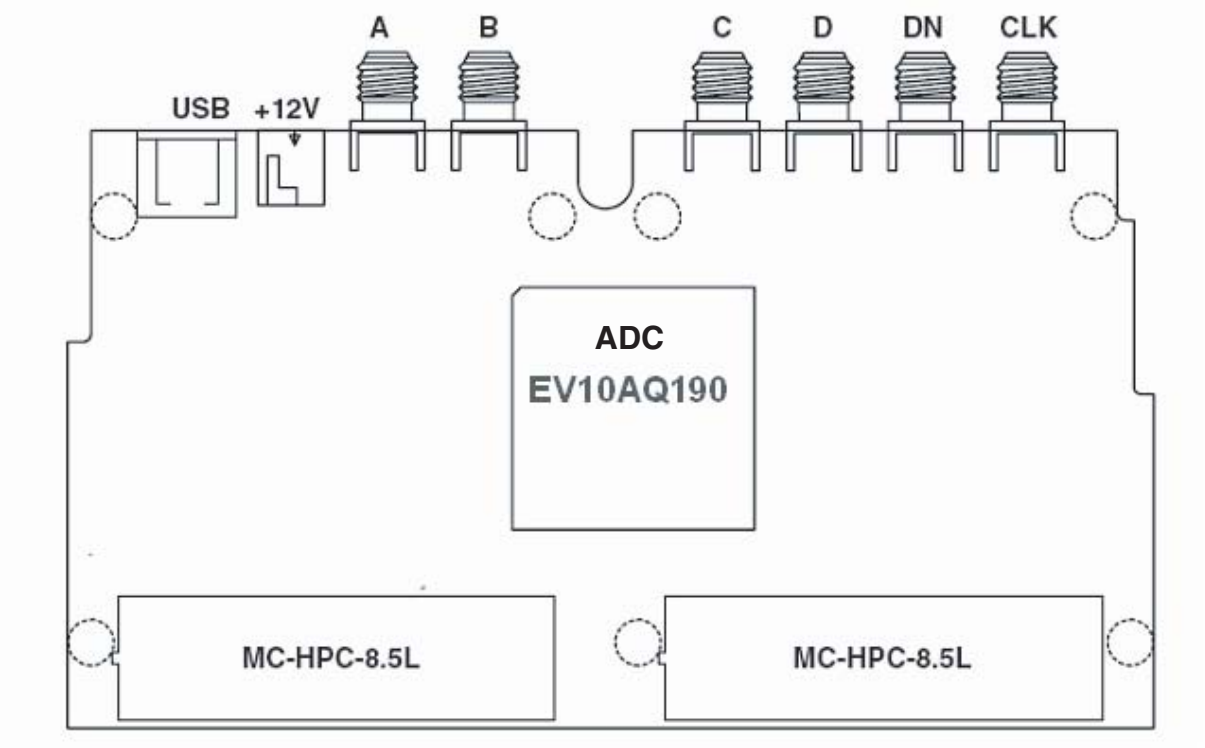
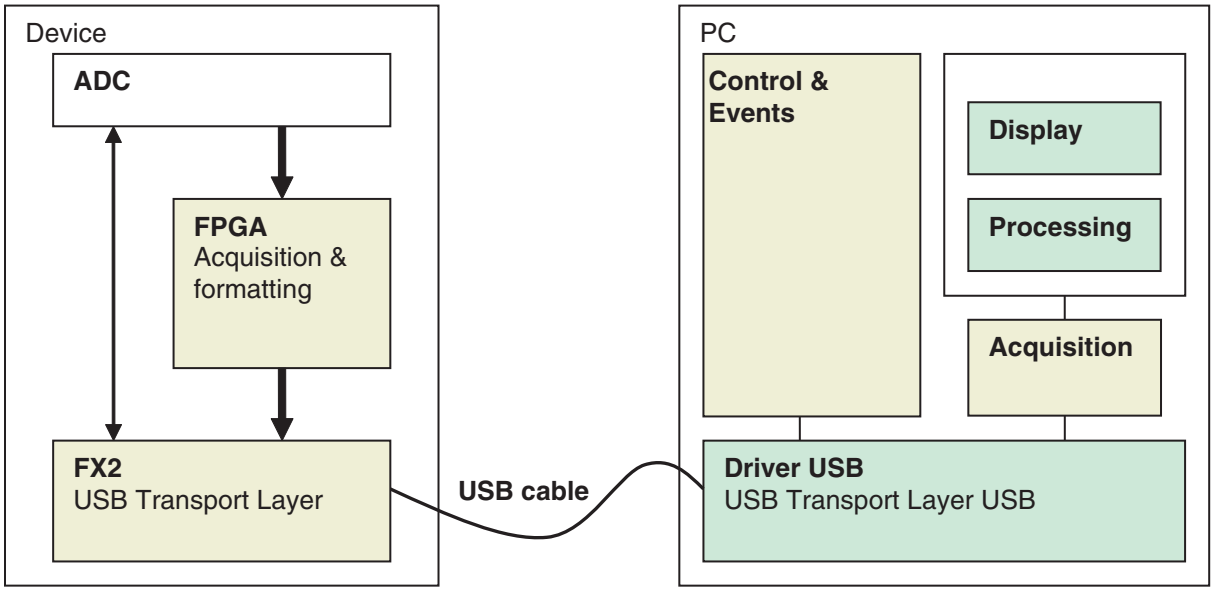


Figure 3-3. EV10AQ190-DK Demo Kit Functional Architecture



Acquisition and formatting of ADC digital output data are done within the FPGA Evaluation Kit. Data is then transmitted again to the ADC Demo Kit.

A USB driver on the ADC Demo kit allows for transmission of the data to the computer that performs the display and processing of ADC output data (FFT).

Software and Graphical User Interface are provided with the Demo Kit. The provided software operates using Labview RunTime (no license required).

4. Ordering Information

Table 4-1. Ordering Information

Part Number	Temperature Range	Comments
EV10AQ190TPY-DK	Ambient	ROHS compliant

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