EV12AQ600
Quad 12bit 1.6 GSps ADC with embedded cross-point switch, Digitizing up to 6.4 GSps
Datasheet 1203

OVERVIEW

EV12AQ600 is a quad channel 12-bit 1.6 GSps ADC. The built-in Cross-Point-Switch (CPS) allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates. In 4-channel operating mode, the four cores can sample, in phase, four independent inputs at 1.6 GSps. In 2-channel operating mode, the cores are interleaved by 2 in order to reach 3.2 GSps sampling rate on each of two inputs. In 1-channel operating mode, a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6.4 GSps. This high flexibility enables digitization of IF and RF signals with up to 3.2 GHz of instantaneous bandwidth.

With an extended input bandwidth above 6 GHz (EFPBW) the EV12AQ600 allows sampling of signals directly in the C-band (4-8 GHz) without the need to translate the signal to baseband through a down-conversion stage.

The ADC includes a multiple ADC chained synchronization feature to enable design of multi-channel systems found in phased-array or MIMO applications.

The EV12AQ600 enables the qualification of a single component which is capable of meeting a wide variety of application needs from single to multi-channel, from baseband to more than 6.4 GHz of input bandwidth.

The device is built in a non-hermetic flip-chip package using HiTCE glass ceramic material in order to reach optimized RF performance and higher pin density.

This circuit is designed, manufactured and will be qualified to be compliant with ESCC (European Space Components Coordination) and QML-Y space requirements.

PERFORMANCE

- **Single core performance**

4-channel mode at 1.6 GSps:

Output Level	Fin (MHz)	ENOB (bit)	SNR (dBFS)	SFDR (dBFS)
-1 dB_{FS} (NFPBW)	100 (NZ1)	8.7/(9.6)*	54.6/(59.9)*	71.3
	780 (NZ1)	8.7/(9.5)*	54.3/(59.4)*	70.2
	1580 (NZ2)	8.4/(9.1)*	53.4/(58.4)*	62.8
	2380 (NZ3)	8.1/(8.8)*	51.3/(56.3)*	61
-8 dB_{FS} (EFPBW)	3280 (NZ4)	8.4/(9.2)*	52.5/(57.7)*	65.9
	3980 (NZ5)	8.3/(9.2)*	52.2/(57.3)*	69.1
	4780 (NZ6)	8.2/(8.9)*	51.7/(56.8)*	61.7
	5580 (NZ7)	8.1/(8.7)*	51.3/(56.3)*	58.2

(*) Averaged simultaneous sampling by averaging the samples of the 4 cores when they are in phase.

SFDR at -8dB_{FS} is better than 60 dB_{FS} up to the 6th Nyquist zone and ENOB is better than 8.0 bit.

SFDR at -8 dB_{FS}, without H2 and H3 harmonics, is better than 74 dB_{FS} up to the 8th Nyquist zone.

- **Interleaved cores performance**

1-channel mode at 6.4 GSps:

Output level	Fin (MHz)	ENOB (bit)	SFDR (dBFS)
-1 dBFS	100 (NZ1)	8.0	55.3
	2380 (NZ1)	8.0	64.8
-8 dBFS	3980 (NZ2)	7.8	52.9

- **Broadband performance at -12dB loading factor:**

4-channel mode at 1.6 GSps over 600 MHz bandwidth
- NPR = 43.4 dB in 1st Nyquist (NFPBW) (at LF = -14dBFS)
- NPR = 41 dB in 2nd Nyquist (NFPBW)
- NPR = 42 dB in 3rd Nyquist (NFPBW)

- **Gain Flatness:**

0.5 dB Gain Flatness in extended bandwidth is typically 4 GHz.

FEATURES

- 1 Vpp 100 Ω differential DC/AC coupled input voltage
- 100 Ω Differential input AC coupled clock
- Cross-point switch enabling 1, 2 or 4 channel mode at 6.4 GSps / 3.2 GSps / 1.6 GSps
- 4.5 / >6 GHz selectable analog input bandwidth (-3 dB)
- Low Latency ESIstream serial link at 12.8 Gbps

Power supply: 3.3 V (analog), 2.5 V (I/O), 1.2 V (digital), optional 1.8 V (SPI)
- Power consumption: 6.6 W
- SPI digital interface
- Manufacturing calibration sets for interleaving
- ADC Gain, Offset, Sampling delay adjustment
- Package: CBGA323 (HiTCE) 16x16 mm pitch 0.80 mm
- Clock and SYNC chaining
- Extended temperature range: Tc -55°C / Tj +125°C

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1 INTRODUCTION

This document is the Preliminary Datasheet of 12-bit 4x1.6 GSps ADC with embedded Cross Point Switch (P/N EV12AQ600)

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2 DESCRIPTION

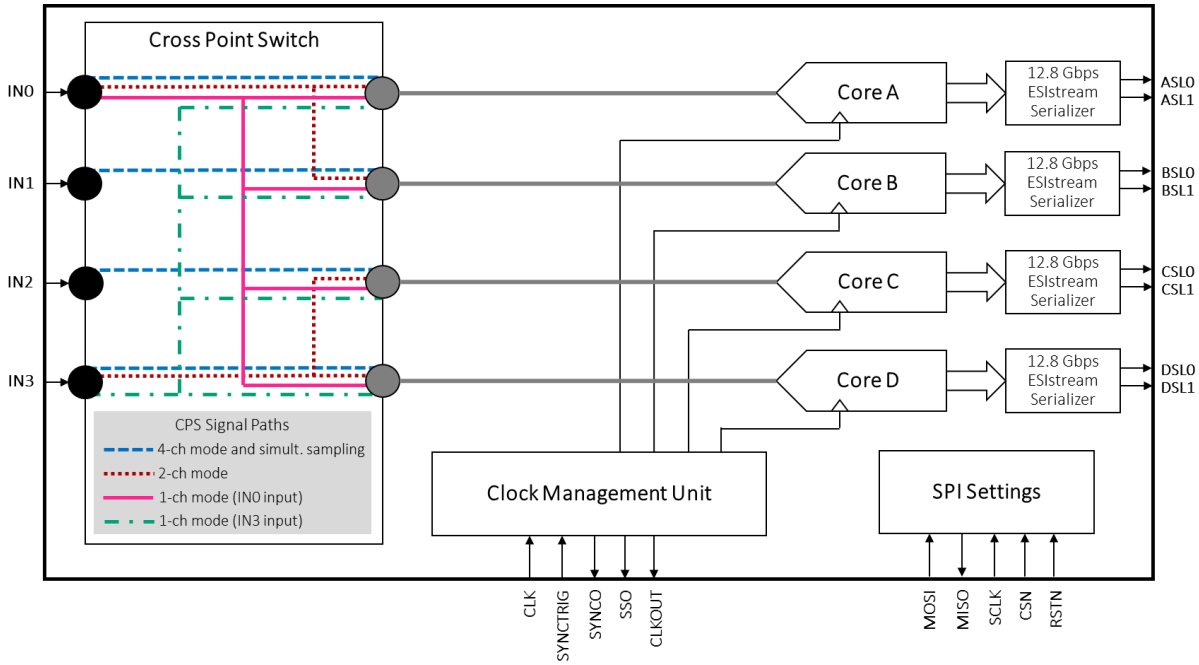


Figure 1 - Quad 12-bit ADC with 12.8 Gbps serial link

EV12AQ600 is a quad 12 bit 1.6 GSps ADC featuring a built in cross-point switch (controlled through the SPI) allowing 1, 2 or 4 channel digitizing at respectively 6.4 GSps, 3.2 GSps or 1.6 GSps sampling rate.

The four ADC cores can operate in phase or interleaved (option controlled though the SPI). External clock must be provided at four times the individual sampling rate.
The architecture uses four high sampling rate single cores (up to 1.6 GSps) without interleaving thus providing high level of spectral purity.

Data is output on a short latency serial link at up to 12.8 Gbps, using ESIstream protocol.

ADC synchronization is possible through SYNC pin and multiple ADC synchronization is simplified thanks to ability of SYNC chaining through SYNCO.

Digital CMOS input levels can be configured in 1.8V, 2.5V or 3.3V logic compatibility.

Tuning and functionalities are controlled through a Serial Peripheral Interface (SPI):

Functionalities controlled through the SPI are:

- Test mode activation and selection (ramp, PRBS, …)
- Clocking modes: 4 ADC cores sampling simultaneously, 2 ADC cores sampling simultaneously in opposition with 2 others, 4 ADC cores interleaved.
- Clocking features: enable/disable CLKOUT, SSO and SYNCO outputs (in order to save power if these features are not needed).
- Inputs selection: 4 ADC cores interleaved and driven by the same input IN0 (or IN3), 2 ADC cores driven simultaneously by IN0 (and IN3), 4 ADCs core driven simultaneously by IN0, IN1, IN2 and IN3.
- Analog input bandwidth: 4.5 GHz (nominal) or >6 GHz (extended).
- Sampling Delay Adjust enabled (for fine tuning of aperture delay) or disabled (recommended for clock Jitter Reduction)
- Manufacturing calibration sets selection and temperature interpolation for interleaved mode. Custom interleaved mode calibration through Offset/Gain/Phase adjustment.
- Selection of bit functionality: In range, Parity Bit, timestamp or Trigger bit.
- Trigger mode or SYNC select (in trigger mode the input on SYNCTRIG is propagated with the same delay as the Analog input, in SYNC mode the input on SYNCTRIG is used to reinitialize internal clock dividers of the ADC, SYNCO is a synchronized copy of SYNCTRIG, PRBS are reset by a SYNC pulse).
- Swing Adjust: Output swing of both serial links and timer CML or LVDS buffers is reduced by 30% for power dissipation reduction purpose.
- Output buffer impedance adjust (trim by a range of 20%) to improve transmission.
- 12.8 Gbps Serial link polarity can be inverted.

The ADC features internal DACs controlled though the SPI for tuning:

- Sampling Delay Adjust 12 bit with 120ps tuning range :
  - 2 bit for coarse step (~ 30ps/step)
  - 10 bit for fine step (~ 30fs/step)
- Gain Adjust: 4096 steps (12 bit DAC), ± 214 LSB (±0.9 dB) full scale variation, step of ~0.1 LSB.
- Offset Adjust: 512 steps (9 bit DAC), ± 27 LSB offset variation, step of ~ 0.11 LSB.
- Phase Adjust: 512 steps (9 bit DAC), ± 0.9 ps phase variation, step of ~3.5fs.
- Analog Input impedance termination trimming (5 bit DAC, 1.7Ω step) common to all analog inputs.
- Input common mode trimming (5 bit DAC) common to all analog inputs, step of 5mV.
- CML output impedance termination trimming (2 bit DAC) by lane, 14 Ω step.

3 SPECIFICATIONS

3.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions.
Exposure above those conditions may cause permanent damage. Long exposure to maximum ratings may affect device reliability

Table 1. Absolute Maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
Analog supply voltage 3.3V	V_{CCA}	AGND – 0.3	3.8 (TBC)	V
Output supply voltage 2.5V	V_{CCO}	GNDO – 0.3	TBD	V
Digital supply voltage 1.2V	V_{CCD}	DGND – 0.3	TBD	V
SPI supply voltage 1.8V, 2.5V or 3.3V	VCC_{SPI}	DGND – 0.3	TBD	V
V_{SPI_SEL} supply voltage	V_{SPI_SEL}	TBD	TBD	V
Analog input swing (mode ON)	| INxP – InxN | (x=0,1, 2 or 3)		4.8 (TBD)	Vppdiff
Analog input swing (mode OFF)	| INxP – InxN | (x=0,1, 2 or 3)		Note (1)	Vppdiff
Analog input peak voltage	INxN or INxP (x=0,1, 2 or 3)	AGND – 0.3	V_{CCA} + 0.3	V
Clock input swing (mode ON)	$\|V_{CLKP} - V_{CLKN}\|$		4	Vppdiff
Clock input swing (mode OFF)	$\|V_{CLKP} - V_{CLKN}\|$		Note (1)	Vppdiff
Clock input voltage	V_{CLKP} or V_{CLKN}	AGND – 0.3	V_{CCA}+ 0.3	V
SYNC input swing (mode ON)	$\|V_{SYNCP} - V_{SYNCN}\|$		4	Vppdiff
SYNC input swing (mode OFF)	$\|V_{SYNCP} - V_{SYNCN}\|$		Note (1)	Vppdiff
SYNC input peak voltage	V_{SYNCP} or V_{SYNCN}	AGND – 0.3	V_{CCA}+ 0.3	V
SPI input voltage	CSN, SCLK, RSTN, MOSI	DGND - 0.3	V_{CC0} + 0.3	V
Max Junction Temperature	T_{JMAX}		150	°C
Storage Temperature	T_{stg}	-65	150	°C
VDIODEA input voltage to prevent leakage (VDIODEC=GND)	$VDIODE_A$	-0.3	0.30	V
Maximum input current on DIODE	$IDIODE_A$		1	mA

Note (1): For cold sparing application, see application note AN 60S 217359
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
Input buffers and associated ESD protection have been designed to allow “cold sparing”.

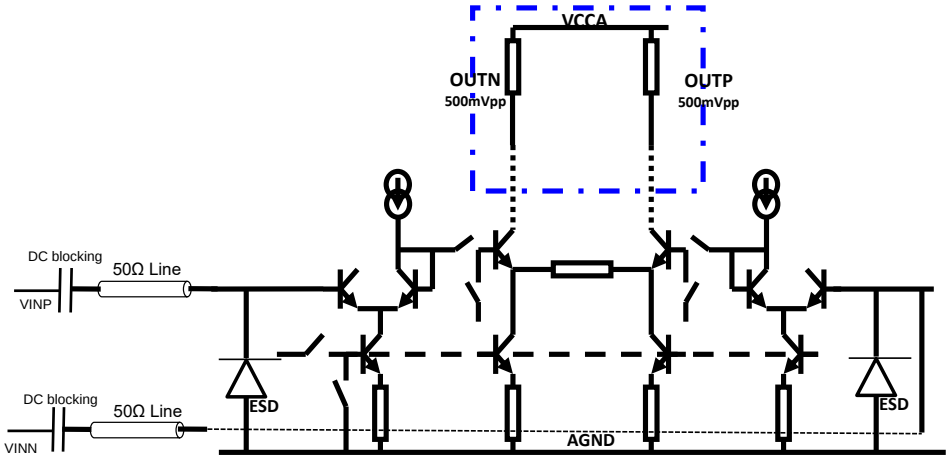


Figure 2 – Analog input scheme regarding max ratings

3.2 Qualification requirements

This circuit is designed and manufactured and will be qualified to be compliant with space requirement (ESCC9000 and QML-Y specifications).

Parameter	Symbol	Value	Unit
Die operating life at Tj =degC	HTOL	TBD	Years
ESD protection (HBM)	HBM	1000	V
Latch up (JEDEC 78A)	LU	+/- 100	mA

3.3 Recommended conditions of use

Table 2. Recommended conditions of use

Parameter	Symbol	Comments	Recommended Value	Unit
Analog supply voltage	V_{CCA}	Analog Part	3.3V	V
Output supply voltage	V_{CCO}	Output buffers	2.5V	V
Digital supply voltage	V_{CCD}	Digital buffers	1.2V	V
SPI supply voltage	V_{CC_SPI}		1.8V if V_D = 1.8V 2.5V if V_D = 2.5V 3.3V if V_D = 3.3V	V
Differential analog input voltage (Full Scale)	V_{IN} -V_{INN}		1 1	Vpp dBm
Clock input power level	P_{CLK} P_{CLKN}		1	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0 3.3 or 2.5 or 1.8 (1)	V
External Clock frequency	Fc		≤ 6.4	GHz
Operating Temperature Range	T_C; T_J		-55°C <T_C ; T_J< 125°C	°C

Note 1: To be configured depending on configuration of pin V_{SPI_SEL}. Refer to section 6.1.

3.4 Explanation of test levels

Table 3. Explanation of test levels

Test level	Comment
1A	100% tested over specified temperature range and specified power supply range, Fclock = 6GHz
1B	100% tested over specified temperature range at typical power supplies, Fclock = 6GHz
1C	100% tested at room temperature over specified supply range, Fclock = 6GHz
1D	100% tested in 25°C environment at typical power supplies, Fclock = 6GHz
2	100% production tested in 25°C environment and samples tested at specified temperatures.
3	Samples tested only at specified temperature.
4	Parameter value is guaranteed by characterization testing (thermal steady-state conditions at specified temperature), Fclock = 6.4GHz unless specified otherwise
5	Parameter value is only guaranteed by design

Only Min and Max values are guaranteed.

3.5 Electrical Characteristics for supplies, Inputs and Outputs

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA} = 3.3V, V_{CCD} = 1.2V, V_{CCO} = 2.5V at room temperature with Fclk = 6GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
Minimum and Maximum values are given over temperature and power supplies.

Table 4. Electrical characteristics for Supplies, Inputs and Outputs

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
RESOLUTION			12			bit	
POWER REQUIREMENTS							
Power Supply voltage							
Analog		V_{CCA}	3.20	3.3	3.40	V	(1)
Output		V_{CCO}	2.35	2.5	2.65		
Digital		V_{CCD}	1.1	1.2	1.3		
SPI		V_{CC_SPI}					
Power Supply current							
Analog	1A	I_{CCA}	1450	1675	1900	mA	(2)
Output							
Full swing	1A	I_{CCO}		365			
Reduced swing	1A	I_{CCO}	300	330	380		
Digital	1A	I_{CCD}	150	195	280		
SPI	1A	I_{CC_SPI}	0	0.2	2.5		
Power Supply current standby mode							
Analog	1A	I_{CCA}	400	510	650	mA	
Output	1A	I_{CCO}	10	20	30		
Digital	1A	I_{CCD}	10	20	60		
SPI	1A	I_{CC_SPI}	0	0.2	2.5		
Power dissipation - Full power mode							
Full swing		PD		6.76		W	(2)
Reduced swing	1A		5.55	6.65	7.75		
Stand-by mode	1A			1.5	1.77	2.1	
Maximum number of power-up		NbPWRup	1E6				(3)
ANALOG INPUTS							
Common mode compatibility for analog inputs		AC or DC					(4)
Input Common Mode (default register value)	1A	VICM	1.5	1.6	1.7	V	
Full Scale Input Voltage range on each differential input		VIN-pp		1000		mVpp Diff	
Analog Input power Level (in 100Ω differential termination)		PIN		+1		dBm	
Input leakage current		IIN	TBD	40	TBD	µA	
Input Resistance (differential)		RIN	TBD	100	TBD	Ω	(5)
Before digital trimming through SPI							
After digital trimming through SPI at given temperature				100		Ω	
Cross-talk between inputs @ Fin=2.4GHz	4			70		dB	

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
CLOCK INPUTS							
Source Type		Low Phase noise Differential Sinewave					
Clock input common mode voltage	1A	V_{CM}	2.4	2.6	2.8	V	
Clock input power level in 100Ω	4	$P_{CLK, CLKN}$	TBD	+1	+7	dBm	
Clock input voltage on each single ended input	4	V_{CLK} or V_{CLKN}	TBD	±250	±500	mV	
Clock input voltage into 100Ω differential clock input	4	$\lvert V_{CLK} - V_{CLKN} \rvert$	TBD	1	2	Vpp	
Clock input minimum slew rate (square or sinewave clock)	4	SR_{CLK}	8	12		GV/s	
Clock input capacitance (die + package)		C_{CLK}		1		pF	
Clock input resistance (differential)	1B	R_{CLK}	95	105	115	Ω	(5)
Clock Jitter (max. allowed on clock source) For 6.4 GHz sinewave analog input	4	Jitter		70		fs_{rms}	(6)
Clock Duty Cycle	4	Duty Cycle	TBD	50	TBD	%	
CLOCK output (CLKOUT)							
Logic Compatibility		CML					
50Ω transmission lines,100Ω (2 x50Ωdifferential termination)							
Output levels : swing adjust off = full swing							
Logic low	1A	V_{OL}		V_{CCA} – 0.31	V_{CCA} – 0.26	V	
Logic high	1A	V_{OH}	V_{CCA} – 0.20	V_{CCA} - 0.14		V	
Differential output	1A	V_{OH}- V_{OL}	140	175	220	mVp	
Common mode	1A	V_{OCM}	V_{CCA} – 0.29	V_{CCA} - 0.22	V_{CCA} – 0.19	V	
Output levels : swing adjust on = reduced swing							
Logic low	1A	V_{OL}		V_{CCA} – 0.17	V_{CCA} – 0.12	V	
Logic high	1A	V_{OH}	V_{CCA} – 0.15	V_{CCA} - 0.09		V	
Differential output	1A	V_{OH}- V_{OL}	70	90	110	mVp	
Common mode	1A	V_{OCM}	V_{CCA} – 0.2	V_{CCA} - 0.13	V_{CCA} – 0.1	V	
SYNC, SYNCN Signal							
Input Voltages to be applied Swing	1A	V_{IH}- V_{IL}	100	350	450	mV	
Common Mode	1A	V_{ICM}	1.125	1.25	1.375	V	
SYNCTRIGP, SYNCTRIGN input capacitance		C_{SYNC}		1		pF	
SYNCTRIGP, SYNCTRIGN input resistance	1B	R_{SYNC}	100	118	130	Ω	
Digital input signals (CSN, SCLK, RSTN, MOSI)							
Low level threshold of Schmitt trigger VCCSPI = 2.5V VCCSPI = 1.8V or 3.3V	1A	Vtminusc			0.35 * VCC_{SPI} 0.8	V	
High level threshold of Schmitt trigger VCCSPI = 2.5V VCCSPI = 1.8V or 3.3V	1A	Vtplusc	0.65 * VCC_{SPI} 1.70			V	
CMOS Schmitt trigger hysteresis		Vhystc	0.10 * V_{CCO}			V	
CMOS low level input current (Vinc=0 V)		Iilc			300	nA	
CMOS high level input current (Vinc=VCCD max)		Iihc			1000	nA	
CMOS low level output voltage (Iolc = 3 mA)	1A	Volc			0.20 * VCC_{SPI}	V	

CMOS high level output voltage (lohc = 3 mA)	1A	Vohc	0.8 * VCC_{SPI}			V	

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
LVDS OUTPUTS (SSO, SYNCO)							
Logic Compatibility				LVDS			
50Ω transmission lines, 100Ω (2 x 50Ω) differential termination							
Output levels : swing adjust off = full swing							
Logic low	1A	V_{OL}			1. 460	V	
Logic high	1A	V_{OH}	1. 16			V	
Differential output	1A	V_{OH}- V_{OL}	200	310	375	mV	
Common mode	1A	V_{OCM}	1.05	1.30	1.55	V	
Output levels : swing adjust on = reduced swing							
Differential output	1A	V_{OH}- V_{OL}	80	210	275	mV	
Common mode	1A	V_{OCM}	1.1		1.6	V	
SERIAL LINK OUTPUTS (ASLx,BSLx,CSLx,DSLx) with x=0 or 1							
Logic Compatibility				CML			
50Ω transmission lines, 100Ω (2 x 50Ω) differential termination							
Output levels : swing adjust off = full swing							
Logic low	1A	V_{OL}		V_{CCO} – 0.65	Vcco – 0.55	V	
Logic high	1A	V_{OH}	V_{CCO} – 0.42	V_{CCO} – 0.324		V	
Differential output	1A	V_{OH}- V_{OL}	260	325	400	mVp	
Common mode	1A	V_{OCM}	V_{CCO} – 0.6	V_{CCO} - 0.45	V_{CCO} – 0.4	V	
Output levels : swing adjust on = reduced swing							
Logic low	1A	V_{OL}		V_{CCO} – 0.45	V_{CCO} – 0.35	V	
Logic high	1A	V_{OH}	V_{CCO} – 0.32	V_{CCO} - 0.22		V	
Differential output	1A	V_{OH}- V_{OL}	170	215	280	mVp	
Common mode	1A	V_{OCM}	V_{CCO} – 0.45	V_{CCO} - 0.35	V_{CCO} – 0.25	V	

Notes:

1. VCC_{SPI} supply value is fixed according to the chosen SPI input signals level. Refer to section 6.1.
2. Enabling either SDA or other features (CLKOUT, SSO, SYNCO) increases power consumption by 170mW (51mA on V_{CCA}). Maximum power consumption is estimated at Tj = 125°C, maximum supplies value and all features enabled.
3. Maximum number of power-up is limited by the maximum number of OTP reading.
4. The DC analog common mode voltage is provided by the ADC.
5. For optimal performance in term of VSWR, characteristic impedance of input traces on the PCB must be differential 100 Ω ± 5% and analog input impedance must be digitally trimmed to cope with process deviation.
6. Jitter calculation integrated up to 6.4 GHz.

3.6 Converter Characteristics

Unless otherwise specified:

- Typical values are given for typical supplies V_{CCA} = 3.3V, V_{CCD} = 1.2V, V_{CCO} = 2.5V at room temperature with Fclk = 6.4GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
- Minimum and Maximum values are given over temperature and power supplies with Fclk = 6 GHz.
- ADC output level -1 dB_{FS}.
- Clock input differentially driven @ +7dBm at ADC input.
- Input common mode is trimmed using 2 different register values (see Table 38): 0x1B for 1st, 2nd and 3rd Nyquist and default value for higher frequencies.
- Nominal bandwidth is selected for 1st and 2nd Nyquist and extended one is applied for other frequencies.

Table 5. Low frequency characteristics

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
DC ACCURACY							
Part to part Gain deviation		G	TBD		TBD	dB	
Gain variation versus temperature		G(T)	TBD		TBD	dB	
Mismatch DC offset		OFFSET	TBD	0	TBD	LSB	(1)
Fin = 100 MHz, -1 dBFS, 1-Channel mode							
DNLrms	1A	DNLrms		0.15	0.28	LSB	
Differential non linearity	1A	DNL	-0.85	-0.5/+0.5	1.2	LSB	
INLrms	1A	INLrms		0.6	1.4	LSB	
Integral non linearity	1A	INL	-4.5	-1.75/+1.75	4.5	LSB	

Notes:

1. After DC offset calibration

3.7 AC Analog Inputs

Table 6. Dynamic Characteristics

Parameter	Test level	Symbol Unit	Min	Typ	Max	Note
Full Power Input Bandwidth						
Nominal Full Power Bandwidth (selected by SPI)	4	GHz		4.5		
Extended Full Band Power Bandwidth (selected by SPI)		GHz		>6		
Gain Flatness (+/- 0.5 dB) (1)						
Nominal Gain Flatness bandwidth (selected by SPI)	4	GHz		1		
Extended Gain Flatness bandwidth (selected by SPI)		GHz		4		
Input Voltage Standing Wave Ratio						
up to 2.4 GHz	4	VSWR			< 1.25:1	
up to 6 GHz					< 2:1	

1. Gain flatness is the bandwidth over which the difference between the gain and the DC gain is lower than 0.5dB

3.8 Dynamic Performances - 4-channel mode – 1.6 GSps

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
SFDR - Spurious Free Dynamic Range - Single tone - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin=98 MHz	4			72.9	73.0		
Fin=778 MHz	4			73.7	75.2		
Fin=1578 MHz	4			64.7	66.9		
Fin=2230 MHz	1A-4	SFDR	55	66.8	TBD		
Fin=2378 MHz	4			64.3	69.7		(1)(2)(3)
Fin=3178 MHz	4	dBFS		56.1	69.2		
Fin=3978 MHz	4			49.5	65.2		
Fin=4778 MHz	4			45.4	74.0		
Fin=5578 MHz	4			47.2	72.2		
At -3 dBFS output level							
Fin=98 MHz	4			67.2	69.0		
Fin=778 MHz	4			71.2	72.9		
Fin=1578 MHz	4			68.6	68.6		
Fin=2230 MHz	4	SFDR		TBD	TBD		
Fin=2378 MHz	4			70.1	70.9		(1)(2)(3)
Fin=3178 MHz	4	dBFS		64.5	74.9		
Fin=3978 MHz	4			56.9	71.3		
Fin=4778 MHz	4			50.7	73.3		
Fin=5578 MHz	4			51.6	73.1		
At -8 dBFS output level							
Fin=98 MHz	4			74.6	76.0		
Fin=778 MHz	4			72.0	76.1		
Fin=1578 MHz	4			71.4	76.1		
Fin=2230 MHz	4	SFDR		TBD	TBD		
Fin=2378 MHz	4			73.2	75.9		(1)(2)(3)
Fin=3178 MHz	4	dBFS		66.2	76.0		
Fin=3978 MHz	4			70.9	75.6		
Fin=4778 MHz	4			62.0	73.7		
Fin=5578 MHz	4			64.7	74.9		
At -12 dBFS output level							
Fin=98 MHz	4			75.3	75.8		
Fin=778 MHz	4			75.0	75.6		
Fin=1578 MHz	4			75.0	75.3		
Fin=2230 MHz	4	SFDR		TBD	TBD		
Fin=2378 MHz	4			74.3	75.3		(1)(2)(3)
Fin=3178 MHz	4	dBFS		73.9	75.2		
Fin=3978 MHz	4			73.9	75.1		
Fin=4778 MHz	4			71.1	74.5		
Fin=5578 MHz	4			72.7	75.1		

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
THD - Total harmonic distortion - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin=98 MHz	4			-66.9			
Fin=778 MHz	4			-66.9			
Fin=1578 MHz	4			-61.1			
Fin=2230 MHz	1A-4	THD		-62.2		-52	
Fin=2378 MHz	4			-60.8			(1)
Fin=3178 MHz	4	dBFS		-55.4			
Fin=3978 MHz	4			-49.2			
Fin=4778 MHz	4			-45.1			
Fin=5578 MHz	4			-45.6			
At -3 dBFS output level							
Fin=98 MHz	4			-63.6			
Fin=778 MHz	4			-66.4			
Fin=1578 MHz	4			-65.0			
Fin=2230 MHz	4	THD		TBD			
Fin=2378 MHz	4			-65.1			(1)
Fin=3178 MHz	4	dBFS		-62.4			
Fin=3978 MHz	4			-56.2			
Fin=4778 MHz	4			-50.3			
Fin=5578 MHz	4			-49.9			
At -8 dBFS output level							
Fin=98 MHz	4			-68.0			
Fin=778 MHz	4			-67.0			
Fin=1578 MHz	4			-66.7			
Fin=2230 MHz	4	THD		TBD			
Fin=2378 MHz	4			-67.0			(1)
Fin=3178 MHz	4	dBFS		-64.0			
Fin=3978 MHz	4			-66.1			
Fin=4778 MHz	4			-60.5			
Fin=5578 MHz	4			-62.0			
At -12 dBFS output level							
Fin=98 MHz	4			-68.8			
Fin=778 MHz	4			-68.6			
Fin=1578 MHz	4			-68.5			
Fin=2230 MHz	4	THD		TBD			
Fin=2378 MHz	4			-67.8			(1)
Fin=3178 MHz	4	dBFS		-67.6			
Fin=3978 MHz	4			-67.8			
Fin=4778 MHz	4			-66.1			
Fin=5578 MHz	4			-66.9			

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Averaged Simul. Sampling (*)	Max	Note
SNR - Signal to noise ratio - 4-channel mode – 1.6 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.6	59.9		(1)
Fin=778 MHz	4			54.3	59.4		
Fin=1578 MHz	4			53.5	58.4		
Fin=2230 MHz	1A-4		49	51.1	TBD		
Fin=2378 MHz	4			51.3	56.3		
Fin=3178 MHz	4			50.3	54.9		
Fin=3978 MHz	4			49.3	54.0		
Fin=4778 MHz	4			48.4	52.9		
Fin=5578 MHz	4			47.4	51.8		
At -3 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.7	59.9		(1)
Fin=778 MHz	4			54.4	59.7		
Fin=1578 MHz	4			53.9	58.9		
Fin=2230 MHz	4			TBD	TBD		
Fin=2378 MHz	4			51.9	57.0		
Fin=3178 MHz	4			51.1	55.9		
Fin=3978 MHz	4			50.4	55.1		
Fin=4778 MHz	4			49.6	54.2		
Fin=5578 MHz	4			48.7	53.2		
At -8 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.8	60.2		(1)
Fin=778 MHz	4			54.8	60.1		
Fin=1578 MHz	4			54.6	59.8		
Fin=2230 MHz	4			TBD	TBD		
Fin=2378 MHz	4			52.9	58.0		
Fin=3178 MHz	4			52.6	57.7		
Fin=3978 MHz	4			52.2	57.3		
Fin=4778 MHz	4			51.8	56.8		
Fin=5578 MHz	4			51.4	56.3		
At -12 dBFS output level							
Fin=98 MHz	4	SNR dBFS		55.1	60.4		(1)
Fin=778 MHz	4			55.0	60.3		
Fin=1578 MHz	4			54.8	60.1		
Fin=2230 MHz	4			TBD	TBD		
Fin=2378 MHz	4			53.2	58.5		
Fin=3178 MHz	4			53.1	58.3		
Fin=3978 MHz	4			52.9	58.1		
Fin=4778 MHz	4			52.8	57.9		
Fin=5578 MHz	4			52.6	57.7		

Parameter	Test level	Symbol Unit	Min	Typical			Max	Note
				Nominal	Without H2 – H3	Averaged Simul. Sampling(*)		
SINAD - Signal to noise and distortion ratio - 4 Channels mode – 1.6GSps								
At -1 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.1		59.3		(1)
Fin=778 MHz	4			53.8		59.0		
Fin=1578 MHz	4			52.6		56.5		
Fin=2230 MHz	1A-4		48	50.8		TBD		
Fin=2378 MHz	4			50.7		54.7		
Fin=3178 MHz	4			48.9		52.5		
Fin=3978 MHz	4			46.2		47.8		
Fin=4778 MHz	4			43.3		44.0		
Fin=5578 MHz	4			43.2		TBD		
At -3 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.0		58.4		(1)
Fin=778 MHz	4			54.0		58.9		
Fin=1578 MHz	4			53.3		57.8		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			51.5		56.3		
Fin=3178 MHz	4			50.6		55.2		
Fin=3978 MHz	4			49.2		52.4		
Fin=4778 MHz	4			46.8		48.4		
Fin=5578 MHz	4			46.1		TBD		
At -8 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.4		59.8		(1)
Fin=778 MHz	4			54.3		59.7		
Fin=1578 MHz	4			54.1		59.4		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			52.5		57.7		
Fin=3178 MHz	4			52.1		57.1		
Fin=3978 MHz	4			51.8		56.8		
Fin=4778 MHz	4			51.1		55.3		
Fin=5578 MHz	4			50.8		TBD		
At -12 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.7		60.1		(1)
Fin=778 MHz	4			54.6		60.1		
Fin=1578 MHz	4			54.5		59.9		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			52.9		58.3		
Fin=3178 MHz	4			52.8		58.1		
Fin=3978 MHz	4			52.6		58.0		
Fin=4778 MHz	4			52.4		57.5		
Fin=5578 MHz	4			52.2		TBD		

Parameter	Test level	Symbol Unit	Min	Typ			Max	Note
				Nominal	Without H2 – H3	Averaged Simul. Sampling(*)		
ENOB - Effective Number Of Bits - 4-channel mode – 1.6 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7		9.6		(1)
Fin=778 MHz	4			8.6		9.5		
Fin=1578 MHz	4			8.4		9.1		
Fin=2230 MHz	1A-4		7.7	8.1		TBD		
Fin=2378 MHz	4			8.1		8.8		
Fin=3178 MHz	4			7.8		8.4		
Fin=3978 MHz	4			7.4		7.6		
Fin=4778 MHz	4			6.9		7.0		
Fin=5578 MHz	4			6.9		TBD		
At -3 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7		9.4		(1)
Fin=778 MHz	4			8.7		9.5		
Fin=1578 MHz	4			8.6		9.3		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			8.3		9.1		
Fin=3178 MHz	4			8.1		8.9		
Fin=3978 MHz	4			7.9		8.4		
Fin=4778 MHz	4			7.5		7.7		
Fin=5578 MHz	4			7.4		TBD		
At -8 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7		9.6		(1)
Fin=778 MHz	4			8.7		9.6		
Fin=1578 MHz	4			8.7		9.6		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			8.4		9.3		
Fin=3178 MHz	4			8.4		9.2		
Fin=3978 MHz	4			8.3		9.2		
Fin=4778 MHz	4			8.2		8.9		
Fin=5578 MHz	4			8.1		8.7		
At -12 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.8		9.7		(1)
Fin=778 MHz	4			8.8		9.7		
Fin=1578 MHz	4			8.8		9.7		
Fin=2230 MHz	4			TBD		TBD		
Fin=2378 MHz	4			8.5		9.4		
Fin=3178 MHz	4			8.5		9.4		
Fin=3978 MHz	4			8.5		9.3		
Fin=4778 MHz	4			8.4		9.3		
Fin=5578 MHz	4			8.4		9.2		

Parameter	Test level	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 4-channel mode – 1.6 GSps - Nominal Bandwidth						
At -1 dBFS output level						
1st Nyquist		NSD dBm/Hz		TBD		(1)
2nd Nyquist						
At -8 dBFS output level						
1st Nyquist		NSD dBm/Hz		TBD		(1)
2nd Nyquist						
NPR - Noise Power Ratio - 4-channel mode – 1.6 GSps - Nominal Bandwidth						
At loading factor = -14 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at Fs/4						
1st Nyquist (NFPBW)		NPR dB	43.3	43.4	43.4	
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 3Fs/4						
2nd Nyquist (NFPBW)		NPR dB	41.4	40.9	41,4	
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 5 Fs/4						(1)
3rd Nyquist (NFPBW)		NPR dB	42.4	42.0	42.4	
At loading factor = -12 dBFS - 640 MHz noise pattern width - 5 MHz notch centered at 7Fs/4						
4th Nyquist (NFPBW)		NPR dB		TBD		

(*) Averaged Simul.Sampling :

Simultaneous sampling is obtained by setting the 4 cores in phase (CLK_MODE_SEL = 0b11, see section 6.3 Register map).
Average simultaneous sampling is obtained by averaging the samples of the 4 cores when they are in phase.

Notes:

1. Optimal bandwidth selection depends on signal characteristic. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.6 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth must be set to Extended. The extended bandwidth degrades noise floor up to 1dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dB_{FS} at -1 dB_{FS}. Removing H2 and H3 allows an SFDR performance higher than 68 dB_{FS} up to 5980 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.

3.9 Dynamic Performances - 2-channel mode – 3.2 GSps

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
SFDR - Spurious Free Dynamic Range - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	SFDR dBFS		69.6			(1)(2)(3)(4)
Fin=778 MHz	4			64.0			
Fin=1578 MHz	4			62.2			
Fin=2230 MHz	4			62.5			
Fin=2378 MHz	4			56.4			
Fin=3178 MHz	4			49.1			
Fin=3978 MHz	4			43.3			
Fin=4778 MHz	4			38.9			
Fin=5578 MHz	4			TBD			
At -3 dBFS output level							
Fin=98 MHz	4	SFDR dBFS		67.2			(1)(2)(3)(4)
Fin=778 MHz	4			65.0			
Fin=1578 MHz	4			64.3			
Fin=2230 MHz	4			65.2			
Fin=2378 MHz	4			60.0			
Fin=3178 MHz	4			51.0			
Fin=3978 MHz	4			45.1			
Fin=4778 MHz	4			40.9			
Fin=5578 MHz	4			TBD			
At -8 dBFS output level							
Fin=98 MHz	4	SFDR dBFS		73.1			(1)(2)(3)(4)
Fin=778 MHz	4			59.3			
Fin=1578 MHz	4			68.0			
Fin=2230 MHz	4			68.1			
Fin=2378 MHz	4			65.0			
Fin=3178 MHz	4			56.3			
Fin=3978 MHz	4			50.1			
Fin=4778 MHz	4			46.0			
Fin=5578 MHz	4			TBD			
At -12 dBFS output level							
Fin=98 MHz	4	SFDR dBFS		76.0			(1)(2)(3)(4)
Fin=778 MHz	4			73.0			
Fin=1578 MHz	4			72.2			
Fin=2230 MHz	4			73.7			
Fin=2378 MHz	4			70.6			
Fin=3178 MHz	4			59.9			
Fin=3978 MHz	4			54.0			
Fin=4778 MHz	4			50.0			
Fin=5578 MHz	4			TBD			

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
THD - Total harmonic distortion - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin=98 MHz	4			-70.0			
Fin=778 MHz	4			-70.7			
Fin=1578 MHz	4			-62.3			
Fin=2230 MHz	4	THD		-62.5			
Fin=2378 MHz	4			-56.5			
Fin=3178 MHz	4	dBFS		-51.0			
Fin=3978 MHz	4			-47.8			
Fin=4778 MHz	4			-48.0			
Fin=5578 MHz	4			TBD			
At -3 dBFS output level							
Fin=98 MHz	4			-64.8			
Fin=778 MHz	4			-68.3			
Fin=1578 MHz	4			-66.5			
Fin=2230 MHz	4	THD		-67.0			
Fin=2378 MHz	4			-63.8			
Fin=3178 MHz	4	dBFS		-58.5			
Fin=3978 MHz	4			-52.9			
Fin=4778 MHz	4			-52.1			
Fin=5578 MHz	4			TBD			
At -8 dBFS output level							
Fin=98 MHz	4			-70.5			
Fin=778 MHz	4			-69.1			
Fin=1578 MHz	4			-68.3			
Fin=2230 MHz	4	THD		-68.7			
Fin=2378 MHz	4			-65.0			
Fin=3178 MHz	4	dBFS		-68.9			
Fin=3978 MHz	4			-62.5			
Fin=4778 MHz	4			-64.1			
Fin=5578 MHz	4			TBD			
At -12 dBFS output level							
Fin=98 MHz	4			-70.7			
Fin=778 MHz	4			-70.0			
Fin=1578 MHz	4			-70.6			
Fin=2230 MHz	4	THD		-69.9			
Fin=2378 MHz	4			-69.0			
Fin=3178 MHz	4	dBFS		-69.6			
Fin=3978 MHz	4			-67.9			
Fin=4778 MHz	4			-69.7			
Fin=5578 MHz	4			TBD			

Parameter	Test level	Symbol Unit	Min	Typ			Max	Note
				Nominal mode	Without H2 – H3	ILG recal at Fin (**)		
TILD - Total InterLeaving Distortion - Single tone - 2-channel mode – 3.2 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-68.7				(4)
Fin=778 MHz	4			-63.5				
Fin=1578 MHz	4			-62.2				
Fin=2230 MHz	4			-63.5				
Fin=2378 MHz	4			-58.4				
Fin=3178 MHz	4			-49.0				
Fin=3978 MHz	4			-43.3				
Fin=4778 MHz	4			-38.8				
Fin=5578 MHz	4			TBD				
At -3 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-69.3				(4)
Fin=778 MHz	4			-65.6				
Fin=1578 MHz	4			-64.1				
Fin=2230 MHz	4			-65.2				
Fin=2378 MHz	4			-59.9				
Fin=3178 MHz	4			-51.0				
Fin=3978 MHz	4			-45.1				
Fin=4778 MHz	4			-40.9				
Fin=5578 MHz	4			TBD				
At -8 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-75.5				(4)
Fin=778 MHz	4			-61.3				
Fin=1578 MHz	4			-69.3				
Fin=2230 MHz	4			-70.3				
Fin=2378 MHz	4			-66.5				
Fin=3178 MHz	4			-56.2				
Fin=3978 MHz	4			-50.1				
Fin=4778 MHz	4			-46.0				
Fin=5578 MHz	4			TBD				
At -12 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-78.2				(4)
Fin=778 MHz	4			-73.5				
Fin=1578 MHz	4			-73.2				
Fin=2230 MHz	4			-75.7				
Fin=2378 MHz	4			-70.4				
Fin=3178 MHz	4			-59.8				
Fin=3978 MHz	4			-54.0				
Fin=4778 MHz	4			-50.0				
Fin=5578 MHz	4			TBD				

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Averaged Simult. Sampling	Max	Note
SNR - Signal to noise ratio - Single tone - 2-channel mode – 3.2 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.3			
Fin=778 MHz	4			53.9			
Fin=1578 MHz	4			53.1			
Fin=2230 MHz	4			51.0			
Fin=2378 MHz	4			50.0			
Fin=3178 MHz	4			49.0			
Fin=3978 MHz	4			48.0			
Fin=4778 MHz	4			47.1			
Fin=5578 MHz	4			TBD			
At -3 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.4			
Fin=778 MHz	4			54.1			
Fin=1578 MHz	4			53.6			
Fin=2230 MHz	4			51.7			
Fin=2378 MHz	4			50.9			
Fin=3178 MHz	4			50.1			
Fin=3978 MHz	4			49.3			
Fin=4778 MHz	4			48.6			
Fin=5578 MHz	4			TBD			
At -8 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.6			
Fin=778 MHz	4			54.6			
Fin=1578 MHz	4			54.3			
Fin=2230 MHz	4			52.6			
Fin=2378 MHz	4			52.3			
Fin=3178 MHz	4			51.9			
Fin=3978 MHz	4			51.6			
Fin=4778 MHz	4			51.1			
Fin=5578 MHz	4			TBD			
At -12 dBFS output level							
Fin=98 MHz	4	SNR dBFS		54.8			
Fin=778 MHz	4			54.7			
Fin=1578 MHz	4			54.6			
Fin=2230 MHz	4			53.0			
Fin=2378 MHz	4			52.9			
Fin=3178 MHz	4			52.7			
Fin=3978 MHz	4			52.5			
Fin=4778 MHz	4			52.3			
Fin=5578 MHz	4			TBD			

Parameter	Test level	Symbol Unit	Min	Typical			Max	Note
				Nominal	Averaged Simult. Sampling(*)	Without H2 - H3		
SINAD - Signal to noise and distortion ratio - Single tone - 2-channel mode – 3.2 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		53.9				(1)
Fin=778 MHz	4			53.2				
Fin=1578 MHz	4			52.0				
Fin=2230 MHz	4			50.4				
Fin=2378 MHz	4			48.5				
Fin=3178 MHz	4			44.8				
Fin=3978 MHz	4			41.0				
Fin=4778 MHz	4			37.8				
Fin=5578 MHz	4			TBD				
At -3 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		53.8				(1)
Fin=778 MHz	4			53.4				
Fin=1578 MHz	4			52.9				
Fin=2230 MHz	4			51.3				
Fin=2378 MHz	4			50.1				
Fin=3178 MHz	4			47.1				
Fin=3978 MHz	4			43.2				
Fin=4778 MHz	4			39.9				
Fin=5578 MHz	4			TBD				
At -8 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.4				(1)
Fin=778 MHz	4			54.3				
Fin=1578 MHz	4			54.0				
Fin=2230 MHz	4			52.4				
Fin=2378 MHz	4			51.8				
Fin=3178 MHz	4			50.4				
Fin=3978 MHz	4			47.5				
Fin=4778 MHz	4			44.6				
Fin=5578 MHz	4			TBD				
At -12 dBFS output level								
Fin=98 MHz	4	SINAD dBFS		54.6				(1)
Fin=778 MHz	4			54.5				
Fin=1578 MHz	4			54.4				
Fin=2230 MHz	4			52.9				
Fin=2378 MHz	4			52.7				
Fin=3178 MHz	4			51.9				
Fin=3978 MHz	4			50.1				
Fin=4778 MHz	4			47.9				
Fin=5578 MHz	4			TBD				

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Averaged Simult. Sampling(*)	Typ Without H2 – H3	Max	Note
ENOB - Effective Number Of Bits - Single tone - 2-channel mode – 3.2 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7				(1)
Fin=778 MHz	4			8.6				
Fin=1578 MHz	4			8.4				
Fin=2230 MHz	4			8.1				
Fin=2378 MHz	4			7.7				
Fin=3178 MHz	4			7.1				
Fin=3978 MHz	4			6.5				
Fin=4778 MHz	4			6.0				
Fin=5578 MHz	4			TBD				
At -3 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7				(1)
Fin=778 MHz	4			8.6				
Fin=1578 MHz	4			8.5				
Fin=2230 MHz	4			8.2				
Fin=2378 MHz	4			8.0				
Fin=3178 MHz	4			7.5				
Fin=3978 MHz	4			6.9				
Fin=4778 MHz	4			6.3				
Fin=5578 MHz	4			TBD				
At -8 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.7				(1)
Fin=778 MHz	4			8.7				
Fin=1578 MHz	4			8.7				
Fin=2230 MHz	4			8.4				
Fin=2378 MHz	4			8.3				
Fin=3178 MHz	4			8.1				
Fin=3978 MHz	4			7.6				
Fin=4778 MHz	4			7.1				
Fin=5578 MHz	4			TBD				
At -12 dBFS output level								
Fin=98 MHz	4	ENOB Bit_FS		8.8				(1)
Fin=778 MHz	4			8.8				
Fin=1578 MHz	4			8.8				
Fin=2230 MHz	4			8.5				
Fin=2378 MHz	4			8.5				
Fin=3178 MHz	4			8.3				
Fin=3978 MHz	4			8.0				
Fin=4778 MHz	4			7.6				
Fin=5578 MHz	4			TBD				

Parameter	Test level	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 2-channel mode – 3.2 GSps - Nominal Bandwidth						
At -1 dBFS output level						
1st Nyquist		NSD dBm/Hz		TBD		(1)
2nd Nyquist						
At -8 dBFS output level						
1st Nyquist		NSD dBm/Hz		TBD		(1)
2nd Nyquist						
NPR - Noise Power Ratio - 2-channel mode – 3.2 GSps						
1st Nyquist (NFPBW)		NPR dB		TBD		(1)
2nd Nyquist (NFPBW)						
3rd Nyquist (NFPBW)						
4th Nyquist (NFPBW)						

(*) Averaged Simul.Sampling :

Simultaneous sampling is obtained by setting the 4 cores in phase (CLK_MODE_SEL = 0b11, see section 6.3 Register map).
Average simultaneous sampling is obtained by averaging the samples of the 4 cores when they are in phase.

(**) **ILG recal at Fin:**

Performance after recalibration at measurement frequency

Notes:

1. Optimal bandwidth selection depends on signal characteristics. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.5 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth select must be set to Extended. The extended bandwidth degrades noise floor up to 1dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dB_{FS} at -1 dB_{FS}. Removing H2 and H3 allows an SFDR performance higher than 68 dB_{FS} up to 5980 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
4. For input frequencies < 800MHz, the SFDR is given with the interleaving calibration set CALSET2. For input frequencies > 800MHz, the SFDR is given with CALSET0.

3.10 Dynamic Performances - 1-channel mode – 6.4 GSps

Parameter	Test level	Symbol Unit	Min	Typ Nominal mode	Typ Without H2 – H3	Typ ILG recal at Fin	Max	Note
SFDR - Spurious Free Dynamic Range – Single tone - 1 channel mode – 6.4 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	SFDR dBFS		66.9				(1)(2)(3)(4)
Fin=778 MHz	4			63.0				
Fin=1578 MHz	4			60.4				
Fin=2230 MHz	1A-4		53	64.7				
Fin=2378 MHz	4			62.9				
Fin=3178 MHz	4			53.4				
Fin=3978 MHz	4			47.0				
Fin=4778 MHz	4			42.9				
Fin=5578 MHz	4			40.0				
At -3 dBFS output level								
Fin=98 MHz	4	SFDR dBFS		67.0				(1)(2)(3)(4)
Fin=778 MHz	4			65.6				
Fin=1578 MHz	4			62.2				
Fin=2230 MHz	4							
Fin=2378 MHz	4			64.4				
Fin=3178 MHz	4			55.5				
Fin=3978 MHz	4			48.9				
Fin=4778 MHz	4			44.8				
Fin=5578 MHz	4			42.0				
At -8 dBFS output level								
Fin=98 MHz	4	SFDR dBFS		69.7				(1)(2)(3)(4)
Fin=778 MHz	4			68.7				
Fin=1578 MHz	4			64.0				
Fin=2230 MHz	4							
Fin=2378 MHz	4			68.8				
Fin=3178 MHz	4			60.4				
Fin=3978 MHz	4			54.0				
Fin=4778 MHz	4			49.9				
Fin=5578 MHz	4			47.0				
At -12 dBFS output level								
Fin=98 MHz	4	SFDR dBFS		68.6				(1)(2)(3)(4)
Fin=778 MHz	4			69.0				
Fin=1578 MHz	4			66.9				
Fin=2230 MHz	4							
Fin=2378 MHz	4			70.4				
Fin=3178 MHz	4			64.9				
Fin=3978 MHz	4			58.1				
Fin=4778 MHz	4			54.0				
Fin=5578 MHz	4			51.2				

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
THD - Total harmonic distortion - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	THD dBFS		-70.2			(1) (4)
Fin=778 MHz	4			-70.2			
Fin=1578 MHz	4			-61.7			
Fin=2230 MHz	1A-4			62.9		-54	
Fin=2378 MHz	4			-61.3			
Fin=3178 MHz	4			-55.5			
Fin=3978 MHz	4			-49.3			
Fin=4778 MHz	4			-45.1			
Fin=5578 MHz	4			-45.8			
At -3 dBFS output level							
Fin=98 MHz	4	THD dBFS		-64.7			(1) (4)
Fin=778 MHz	4			-68.7			
Fin=1578 MHz	4			-66.5			
Fin=2230 MHz	4			TBD			
Fin=2378 MHz	4			-66.9			
Fin=3178 MHz	4			-63.3			
Fin=3978 MHz	4			-56.4			
Fin=4778 MHz	4			-50.4			
Fin=5578 MHz	4			-50.1			
At -8 dBFS output level							
Fin=98 MHz	4	THD dBFS		-71.0			(1) (4)
Fin=778 MHz	4			-69.0			
Fin=1578 MHz	4			-68.8			
Fin=2230 MHz	4			TBD			
Fin=2378 MHz	4			-69.5			
Fin=3178 MHz	4			-52.1			
Fin=3978 MHz	4			-68.3			
Fin=4778 MHz	4			-61.1			
Fin=5578 MHz	4			-62.9			
At -12 dBFS output level							
Fin=98 MHz	4	THD dBFS		-73.2			(1) (4)
Fin=778 MHz	4			-72.5			
Fin=1578 MHz	4			-72.7			
Fin=2230 MHz	4			TBD			
Fin=2378 MHz	4			-71.6			
Fin=3178 MHz	4			-70.8			
Fin=3978 MHz	4			-71.6			
Fin=4778 MHz	4			-68.5			
Fin=5578 MHz	4			-70.0			

Parameter	Test level	Symbol Unit	Min	Typ			Max	Note
				Nominal mode	Without H2 – H3	ILG recal at Fin (**)		
TILD - Total InterLeaving Distortion - Single tone - 1-channel mode – 6.4 GSps								
At -1 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-62.7				(1) (4)
Fin=778 MHz	4			-59.6				
Fin=1578 MHz	4			-57.1				
Fin=2230 MHz	1A-4			-61.8			-51	
Fin=2378 MHz	4			-60.5				
Fin=3178 MHz	4			-51.8				
Fin=3978 MHz	4			-46.0				
Fin=4778 MHz	4			-41.8				
Fin=5578 MHz	4			-38.3				
At -3 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-64.3				(1) (4)
Fin=778 MHz	4			-62.5				
Fin=1578 MHz	4			-58.8				
Fin=2230 MHz	4			TBD				
Fin=2378 MHz	4			-61.7				
Fin=3178 MHz	4			-54.0				
Fin=3978 MHz	4			-48.0				
Fin=4778 MHz	4			-43.7				
Fin=5578 MHz	4			-40.5				
At -8 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-67.1				(1) (4)
Fin=778 MHz	4			-65.9				
Fin=1578 MHz	4			-61.6				
Fin=2230 MHz	4			TBD				
Fin=2378 MHz	4			-65.4				
Fin=3178 MHz	4			-60.6				
Fin=3978 MHz	4			-53.0				
Fin=4778 MHz	4			-48.8				
Fin=5578 MHz	4			-45.6				
At -12 dBFS output level								
Fin=98 MHz	4	TILD dBFS		-66.9				(1) (4)
Fin=778 MHz	4			-66.8				
Fin=1578 MHz	4			-63.5				
Fin=2230 MHz	4			TBD				
Fin=2378 MHz	4			-67.3				
Fin=3178 MHz	4			-62.2				
Fin=3978 MHz	4			-56.8				
Fin=4778 MHz	4			-52.9				
Fin=5578 MHz	4			-49.6				

Parameter	Test level	Symbol Unit	Min	Typ	Max	Note
SNR - Signal to noise ratio - Single tone - 1-channel mode – 6.4 GSps						
At -1 dBFS output level						
Fin=98 MHz	4	SNR dBFS		54.2		(1) (4)
Fin=778 MHz	4			53.9		
Fin=1578 MHz	4			53.1		
Fin=2230 MHz	1A-4		49	51.0		
Fin=2378 MHz	4			50.0		
Fin=3178 MHz	4			49.0		
Fin=3978 MHz	4			48.0		
Fin=4778 MHz	4			47.1		
Fin=5578 MHz	4			TBD		
At -3 dBFS output level						
Fin=98 MHz	4	SNR dBFS		54.3		(1) (4)
Fin=778 MHz	4			54.1		
Fin=1578 MHz	4			53.6		
Fin=2230 MHz	4			51.7		
Fin=2378 MHz	4			50.9		
Fin=3178 MHz	4			50.1		
Fin=3978 MHz	4			49.3		
Fin=4778 MHz	4			48.5		
Fin=5578 MHz	4			TBD		
At -8 dBFS output level						
Fin=98 MHz	4	SNR dBFS		54.5		(1) (4)
Fin=778 MHz	4			54.5		
Fin=1578 MHz	4			54.3		
Fin=2230 MHz	4			52.6		
Fin=2378 MHz	4			44.0		
Fin=3178 MHz	4			51.9		
Fin=3978 MHz	4			51.5		
Fin=4778 MHz	4			51.1		
Fin=5578 MHz	4			TBD		
At -12 dBFS output level						
Fin=98 MHz	4	SNR dBFS		54.7		(1) (4)
Fin=778 MHz	4			54.7		
Fin=1578 MHz	4			54.6		
Fin=2230 MHz	4			53.0		
Fin=2378 MHz	4			52.9		
Fin=3178 MHz	4			52.7		
Fin=3978 MHz	4			52.5		
Fin=4778 MHz	4			52.3		
Fin=5578 MHz	4			TBD		

Parameter	Test level	Symbol Unit	Min	Typical Nominal	Typical Without H2 - H3	Max	Note
SINAD - Signal to noise and distortion ratio - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	SINAD dBFS		53.5			(1) (4)
Fin=778 MHz	4			52.8			
Fin=1578 MHz	4			51.2			
Fin=2230 MHz	1A-4		48	50.2			
Fin=2378 MHz	4			47.1			
Fin=3178 MHz	4			43.1			
Fin=3978 MHz	4			39.5			
Fin=4778 MHz	4			37.1			
Fin=5578 MHz	4			TBD			
At -3 dBFS output level							
Fin=98 MHz	4	SINAD dBFS		53.5			(1) (4)
Fin=778 MHz	4			53.4			
Fin=1578 MHz	4			52.2			
Fin=2230 MHz	4			51.1			
Fin=2378 MHz	4			49.0			
Fin=3178 MHz	4			45.5			
Fin=3978 MHz	4			42.0			
Fin=4778 MHz	4			39.5			
Fin=5578 MHz	4			TBD			
At -8 dBFS output level							
Fin=98 MHz	4	SINAD dBFS		54.2			(1) (4)
Fin=778 MHz	4			54.0			
Fin=1578 MHz	4			53.4			
Fin=2230 MHz	4			52.3			
Fin=2378 MHz	4			51.2			
Fin=3178 MHz	4			49.4			
Fin=3978 MHz	4			46.8			
Fin=4778 MHz	4			44.4			
Fin=5578 MHz	4			TBD			
At -12 dBFS output level							
Fin=98 MHz	4	SINAD dBFS		54.4			(1) (4)
Fin=778 MHz	4			54.3			
Fin=1578 MHz	4			54.0			
Fin=2230 MHz	4			52.8			
Fin=2378 MHz	4			52.3			
Fin=3178 MHz	4			51.2			
Fin=3978 MHz	4			49.6			
Fin=4778 MHz	4			47.7			
Fin=5578 MHz	4			TBD			

Parameter	Test level	Symbol Unit	Min	Typ Nominal	Typ Without H2 – H3	Max	Note
ENOB - Effective Number Of Bits - Single tone - 1-channel mode – 6.4 GSps							
At -1 dBFS output level							
Fin=98 MHz	4	ENOB Bit_FS		8.6			(1) (4)
Fin=778 MHz	4			8.5			
Fin=1578 MHz	4			8.2			
Fin=2230 MHz	1A-4		7.7	8.0			
Fin=2378 MHz	4			7.5			
Fin=3178 MHz	4			6.9			
Fin=3978 MHz	4			6.3			
Fin=4778 MHz	4			5.9			
Fin=5578 MHz	4			TBD			
At -3 dBFS output level							
Fin=98 MHz	4	ENOB Bit_FS		8.6			(1) (4)
Fin=778 MHz	4			8.6			
Fin=1578 MHz	4			8.4			
Fin=2230 MHz	4			8.2			
Fin=2378 MHz	4			7.8			
Fin=3178 MHz	4			7.3			
Fin=3978 MHz	4			6.7			
Fin=4778 MHz	4			6.3			
Fin=5578 MHz	4			TBD			
At -8 dBFS output level							
Fin=98 MHz	4	ENOB Bit_FS		8.7			(1) (4)
Fin=778 MHz	4			8.7			
Fin=1578 MHz	4			8.6			
Fin=2230 MHz	4			8.4			
Fin=2378 MHz	4			8.2			
Fin=3178 MHz	4			7.9			
Fin=3978 MHz	4			7.5			
Fin=4778 MHz	4			7.1			
Fin=5578 MHz	4			TBD			
At -12 dBFS output level							
Fin=98 MHz	4	ENOB Bit_FS		8.7			(1) (4)
Fin=778 MHz	4			8.7			
Fin=1578 MHz	4			8.7			
Fin=2230 MHz	4			8.5			
Fin=2378 MHz	4			8.4			
Fin=3178 MHz	4			8.2			
Fin=3978 MHz	4			7.9			
Fin=4778 MHz	4			7.6			
Fin=5578 MHz	4			TBD			

Parameter	Test level	Symbol Unit	Min	Typ	Max	Note
NSD - Noise Spectral Density - 1-channel mode – 6.4 GSps - Extended Bandwidth						
At -1 dBFS output level						
3rd Nyquist		NSD dBm/Hz		-145		
At -8 dBFS output level						
3rd Nyquist		NSD dBm/Hz		-147		
4th Nyquist				-148		
NPR - Noise Power Ratio - 1-channel mode – 6.4 GSps						
At loading factor = -12 dBFS – 2560 MHz noise pattern width - 5 MHz notch centered at Fs/4						
1st Nyquist (NFPBW)		NPR dB		TBD		
At loading factor = -12 dBFS – 2560 MHz noise pattern width - 5 MHz notch centered at 3Fs/4						
2nd Nyquist (NFPBW)		NPR dB		TBD		
3rd Nyquist (NFPBW)						
4th Nyquist (NFPBW)						

(**) ILG recalibr at Fin: Performance after recalibration at measurement frequency

Notes:

1. Optimal bandwidth selection depends on signal characteristics. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.5 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth select must be set to Extended. The extended bandwidth degrades noise floor up to 1dB, compensated at high frequency by inputing signals with lower signal attenuation.
2. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
3. SFDR without H3 harmonic is better than 60 dB_{FS} at -1 dB_{FS}. Removing H2 and H3 allows an SFDR performance higher than 68 dB_{FS} up to 5980 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
4. For input frequencies < 800MHz, the SFDR is given for with interleaving calibration set CALSET2. For input frequencies > 800MHz, the SFDR is given with CALSET0. See 8.3

3.11 Transient and Switching Characteristics

Unless otherwise specified:

- Typical values are given for typical supplies V_{CCA} = 3.3V, V_{CCD} = 1.2V, V_{CCO} = 2.5V at room temperature with Fclk = 6.4GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled).
- Minimum and Maximum values are given over temperature and power supplies.
- ADC output level -1 $dB_{FS.}$
- Clock input differentially driven @ +1dBm at ADC input.
- Non interleaved ADC.

Table 7. Transient characteristics

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
TRANSIENT PERFORMANCE							
Conversion Error Rate at 1.6 GSps Less than 128 LSB (TBC)	4	CER		$6.10E^{-15}$ (TBC)		Error/ sample	(1)
Serial link Bit Error Rate at 12.8 Gbps	4	BER		$10E^{-15}$(TBC)		Error/ sample	
Overvoltage Recovery Time	4	ORT		666 (TBC)		ps	

Notes:

1. Fs = 1.6 GSps, T_J = 110 °C. For Tj=125°C, CER value is $10E^{-12}$

Table 8. Switching characteristics

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS (Any Output Mode)							
External Clock low frequency range	4	F_{CLK}	800		2000	MHz	
External Clock high frequency range			4500		6400	MHz	
Sampling Clock low frequency range per core	4	Fs	200		500	MSps	
Sampling Clock high frequency range per core			1125		1600	MSps	
Sampling Clock to CLKOUT delay	4	Tclkout		TBD		ps	
Max crosstalk from CLKOUT on clock input signal@ 12Gbps	4	XTALK_CKO2CK			-40 (TBC)	dB	
Aperture Delay (SDA Disabled)	4	T_A		TBD		ps	
Sampling Delay Tuning Range (SDA Enabled)	4		0.03		120	ps	
ADC Aperture uncertainty (SDA Disabled)	4	$JitterSDA_{OFF}$		135(TBC)		fs_{rms}	(1)
ADC Aperture uncertainty (SDA enabled min)	4	$JitterSDA_{MIN}$		150(TBC)		fs_{rms}	
ADC Aperture uncertainty (SDA enabled max)	4	$JitterSDA_{MAX}$		180 (TBC)		fs_{rms}	
CLKOUT jitter	4	Jitterclkout		60 (TBC)		fs_{rms}	
Digital reset duration	4		10			µs	
ADC settling time after power up	4	TS		TBD		µs	
Minimum SYNC pulse width	4	TSYNC		TBD		External Clock cycles	
SWITCHING PERFORMANCE AND CHARACTERISTIC (SSO, SYNCO)							
Output rise time (20%-80%)	4	TR		250		ps	(2)
Output fall time (20%-80%)		TF		250		ps	(2)
SSO and SYNCO pipeline delay	4	TPD_{SSO}		TBD		External Clock cycles	
SWITCHING PERFORMANCE AND CHARACTERISTIC (Serial output)							

Parameter	Test level	Symbol	Min	Typ	Max	Unit	Note
Output Data delay (pipeline + delay)	4	TPD		TBD		External Clock cycles	
		TOD		TBD		ps	
Output rise time for DATA (20%-80%)	4	TR		30		ps	(3)
Output fall time for DATA (20%-80%)		TF		30		ps	(3)
Total jitter @ 12Gbps	4	2XT1		25		ps	(3)
Minimum buffer amplitude time @ 12Gbps	4	XT2		33.3		ps	(3)
Maximum buffer amplitude @ 12Gbps	4	YT1		260		mV	(3)
Minimum buffer amplitude @ 12Gbps		YT2		180		mV	(3)
Skew between serial output signal P and N	4	Tskew			0.6 (TBC)	ps	(3)
Conversion Core latency Total conversion latency	4			5 126		External Clock cycles	(4)
Crosstalk between xSL1 and xSL0@ 12Gbps (x= A, B, C or D)	4	XTALK_SL2SL			-40 (TBC)	dB	(3)
Max crosstalk between output serial link and analog input signal @ 12Gbps		XTALK_SL2IN			-80 (TBC)	dB	(3)

Notes:

1. See Definition of Terms.
2. 100Ω load + PCB line 17 cm.
3. 100Ω load + PCB line 17 cm.
4. The latency of the conversion core is fixed. The total latency of the ADC (including the serial interface) can take any system external clock cycle between 126 and 141. ESIstream protocol wipes out the variable latency on the receivers end due to its intrinsic synchronization procedure.

3.11.1 Latency

The conversion core latency is less than 5 clock cycles. The total latency (including serial output latency) is 126 clock cycles.
The serial output latency can vary from 0 to 16 clock cycles. This variable latency is wiped out on the receivers end thanks to the intrinsic synchronization feature of the ESIstream protocol.
It is also to be noted that the serial output latency will only be variable when asynchronous SYNC signal is used or at startup. Any synchronized SYNC signal will end up in the exact same latency at the serial output.

The Figure 3 depicts the different latencies of the device.

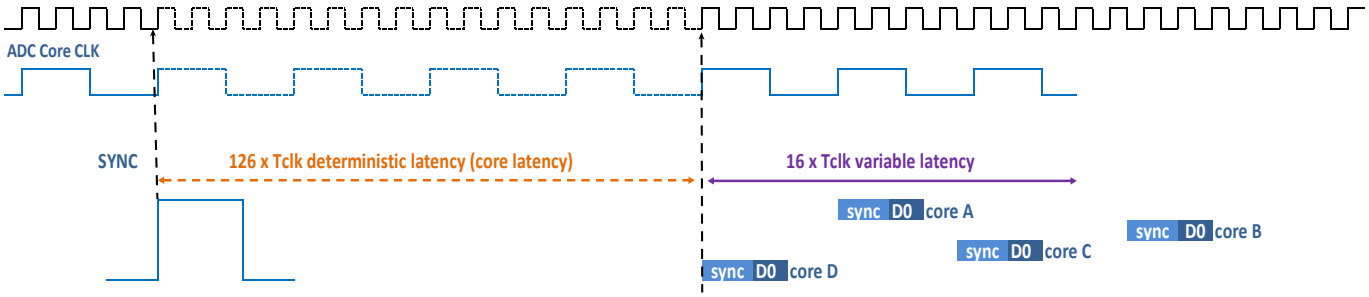


Figure 3 - Deterministic (core conversion) latency and non-deterministic (serial output) latency

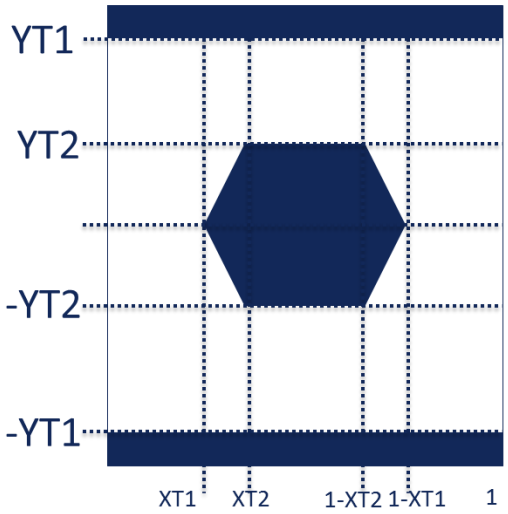


Figure 4 - Serial link eye diagram

Table 9. SPI Timing characteristics

Parameter	Test Level	Symbol	Value			Unit	Note
			Min	Typ	Max		
RSTN pulse length	4	T_{RSTN}	10			µs	
SCLK frequency	4	F_{SCLK}			10	MHz	
CSN to SCLK delay	4	$T_{CSN-SCLK}$	0.5			T_{SCLK}	
MISO setup time	4	T_{setup}	3			ns	
MISO hold time	4	T_{hold}	3			ns	
MOSI output delay	4	T_{delay}			TBD	ns	

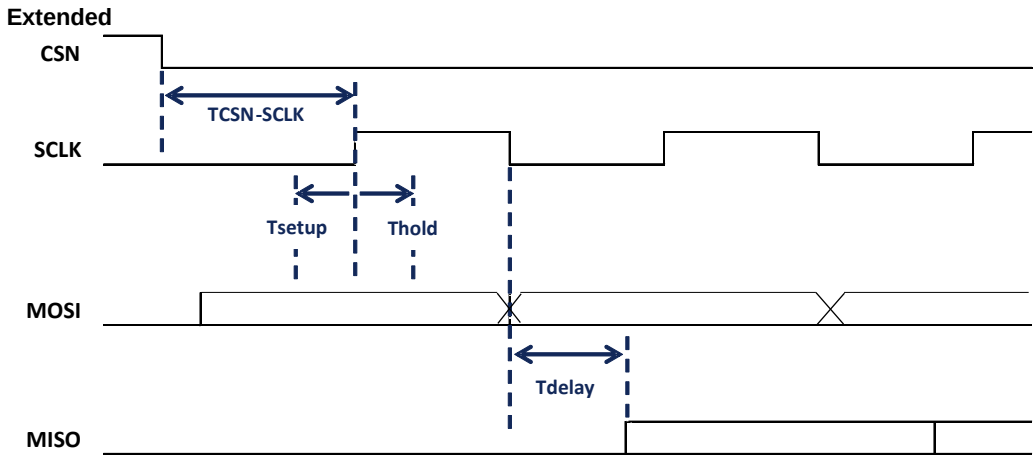


Figure 5 - SPI timing diagram

3.12 Digital Output Coding

Table 10. ADC Digital output coding table

Differential analog input	Voltage level	Binary MSB (bit 11).....LSB (bit 0)	In-Range
> + 500.125 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	0
+ 500.125 mV	Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	1
+ 500 mV	Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 0	1
+ 0.125 mV	Mid scale + ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0	1
- 0.125 mV	Mid scale - ½ LSB	0 1 1 1 1 1 1 1 1 1 1 1	1
- 500 mV	Bottom end of full scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1	1
-500.125 mV	Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	1
< - 500.125 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	0

3.13 Definition of Terms

Table 11. Definition of terms

Abbreviation	Term	Definition
(BER)	Bit Error Rate	Percentage of bits with errors divided by the total number of bits that have been transmitted, received or processed over a given time period.
(CER)	conversion Error Rate	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate due to ADC quantization. An error code is a code that differs by more than +/- 128 LSB from the correct code.
(DNL)	Differential non linearity	The Differential Non Linearity for an output code “” is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(ENOB)	Effective Number Of Bits	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(ILG)	Interleaving	Interleaving of the internal cores.
(IMD)	InterModulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(INL)	Integral non linearity	The Integral Non Linearity for an output code “I” is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(NSD)	Noise SpectralDensity	The NSD is the power spectral density magnitude of the ADC expressed in dBm/Hz.
(ORT)	Overvoltage recovery time	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB_{FS} (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(SINAD)	Signal to noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	Signal to noise ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the nine first harmonics.
(T_A)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which analog input (INxP, INxN where X = 0, 1, 2 or 3) is sampled.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(THD)	Total harmonic distortion	Ratio expressed in dB of the RMS sum up to n^{th} harmonic components, n to be specified, to the RMS input signal amplitude. It may be reported in dB_{FS} (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(TILD)	Total InterLeaving Distortion	Ratio expressed in dB of the RMS sum up to interleaving spurs (Fclock/4 +/- Fin, Fclock/2 - Fin, Fclock/4 in QUAD mode, and Fclock/2 +/- Fin in DUAL mode).
(TOD)	Digital data Output delay	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TPD)	Pipeline Delay	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).

(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TS)	Settling time	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(TSYNC)	SYNC duration	External SYNC pulse width needed for SYNC function.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).

4 PACKAGE DESCRIPTION

4.1 Type /Outline

HiTCE Ceramic Ball Grid Array CBGA323

- High TCE Glass-Ceramic substrate
- Body size: 16.0x16.0 mm
- Lands Pitch: 0.80mm
- Number of balls: 323
- Conductor: cofired copper

Package interconnection

- 18x18 BGA matrix (323 balls, A1 removed)
- 0.80 mm ball pitch
- Ball type : Pb90Sn10 or SAC305
- MSL3 (non-hermetic)

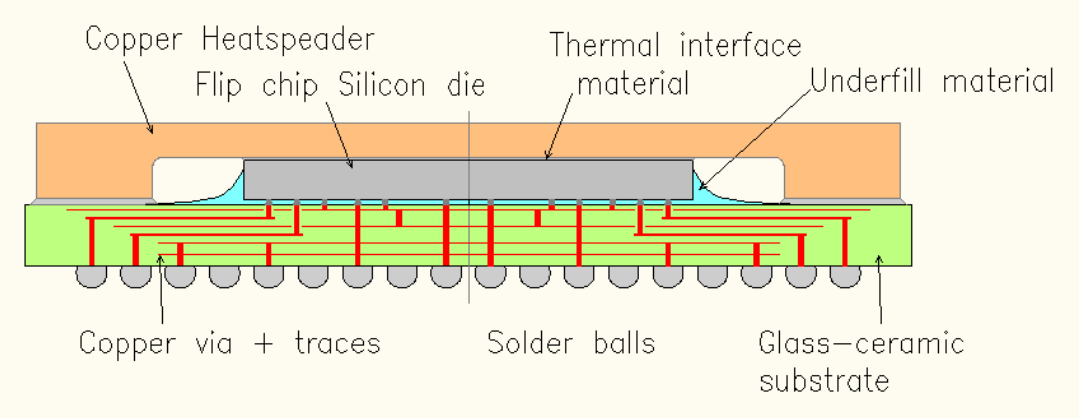


Figure 6 – Package cross-section

Package outline for Pb90Sn10 balls

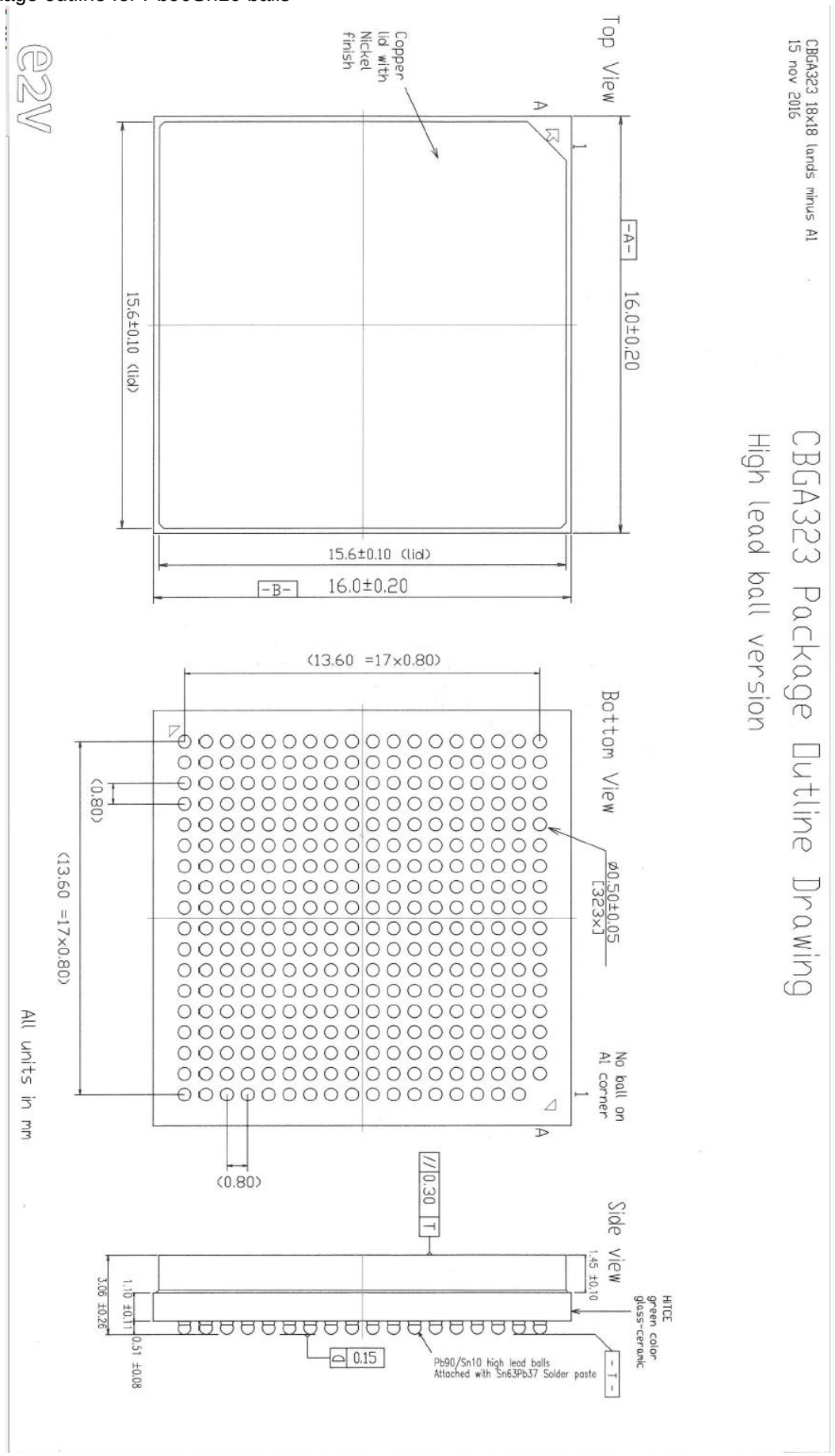


Figure 7 – Package outline for Pb90Sn10 balls

Package outline for SAC305 balls

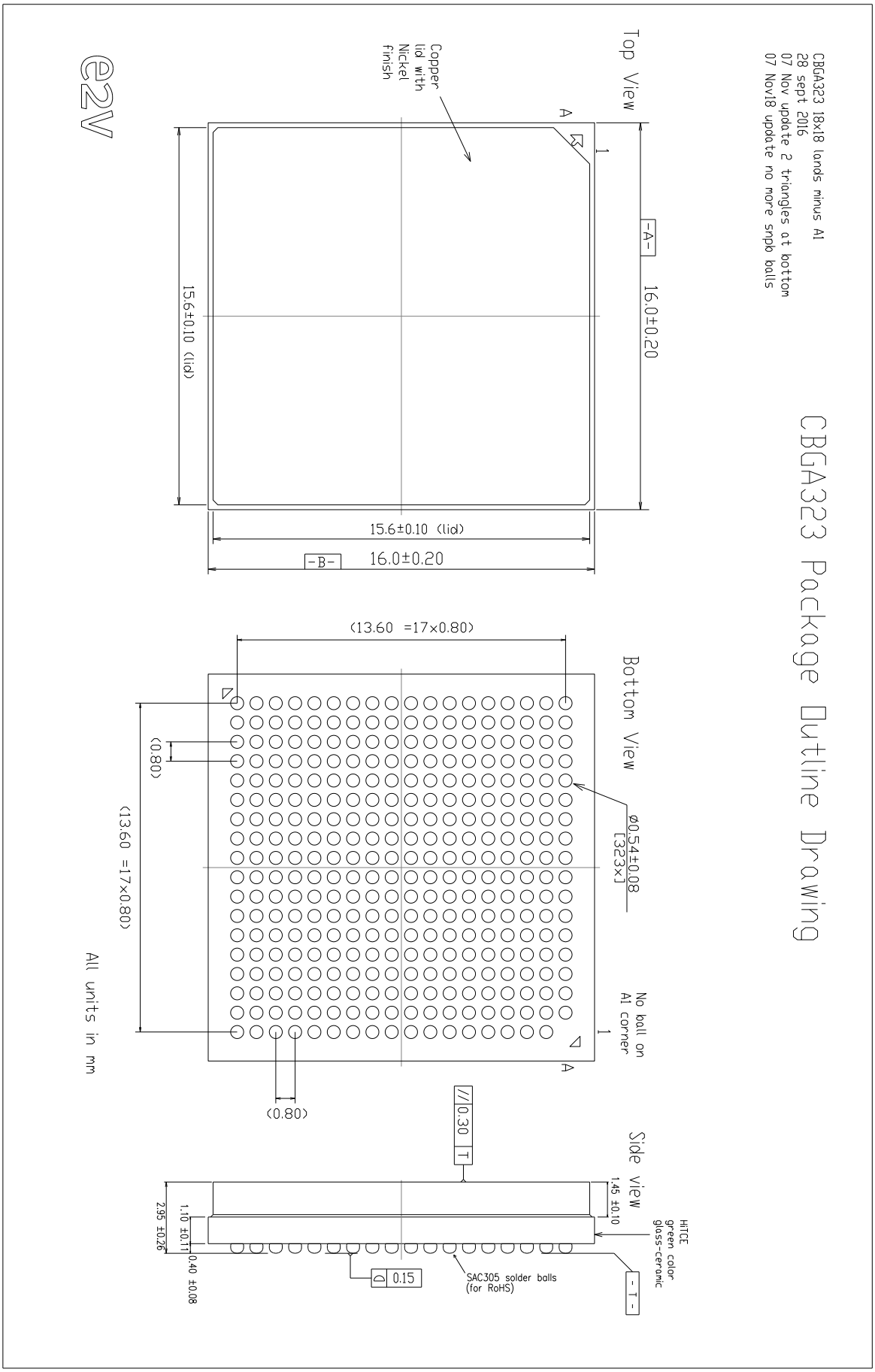


Figure 8 – Package outline for SAC305 balls

4.2 Pinout top view

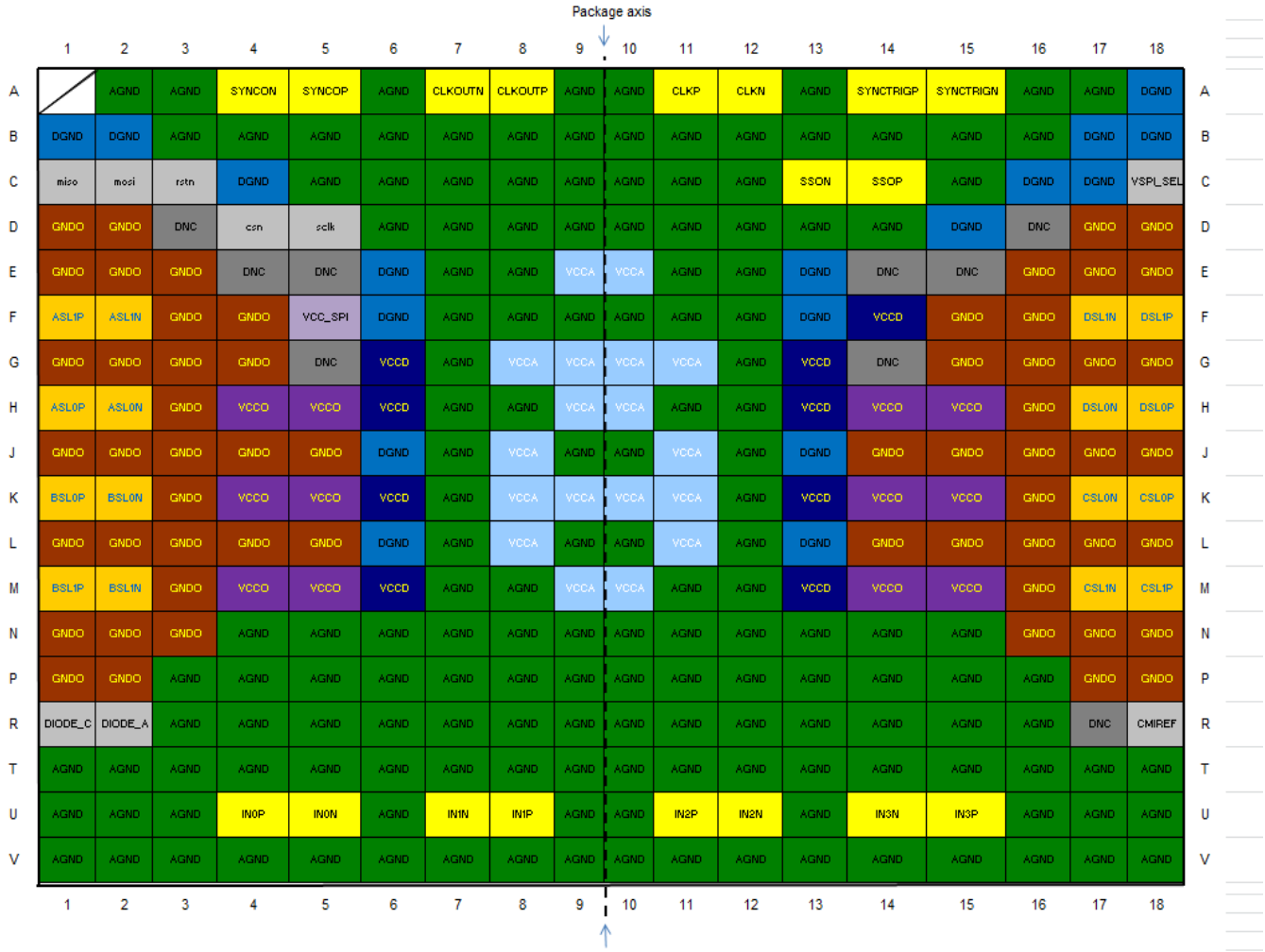


Figure 9 – Pinout

4.3 Relative skew for serial links view

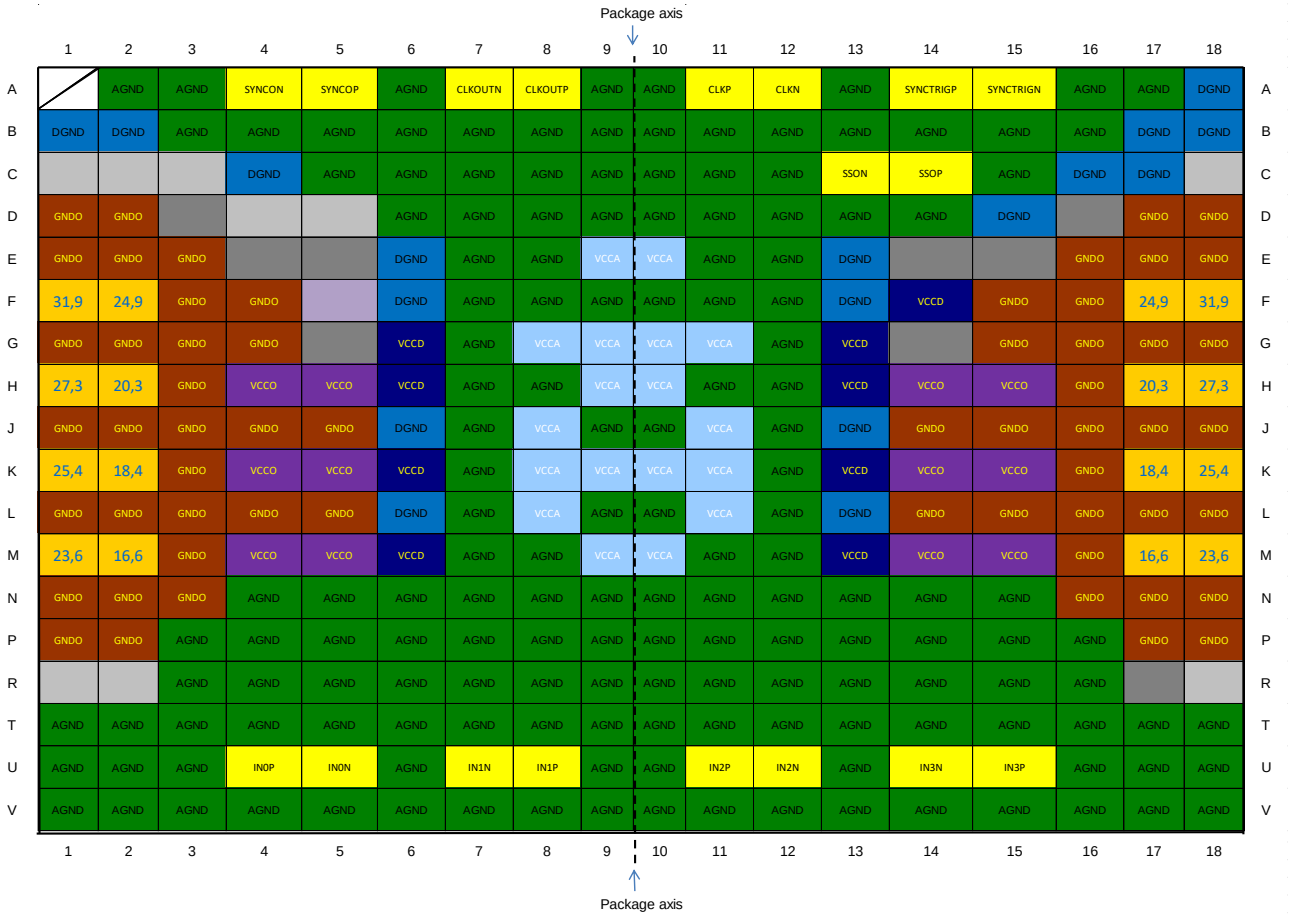
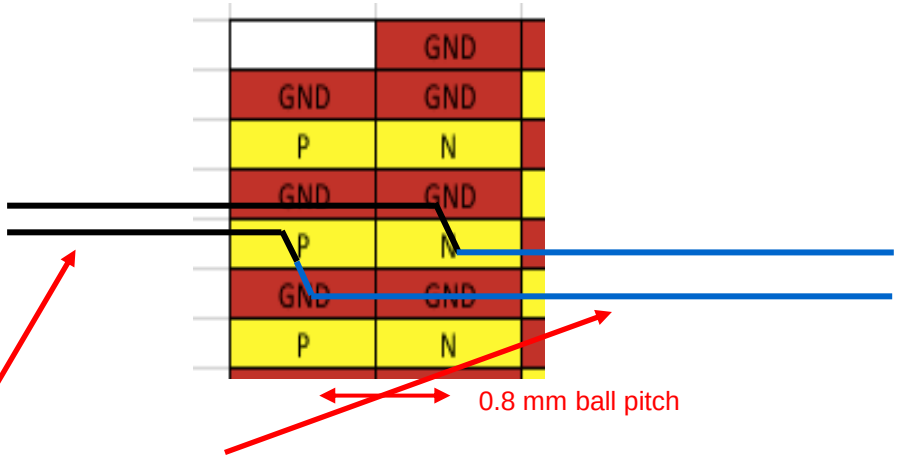


Figure 10 – Skew mapping (values are in ps)

Those skew values are relative to the same reference. BSL1P skew value is 23.6 ps and BSL1N skew value is 16.6 ps. The relative skew value between BSL1P and BSL1N is 7 ps.

With a special care on the board routing, it is possible to compensate the relative skew between differential serial links (N&P).



Length on board + length on package are almost the same on N and P (less routing on board for P results from more routing inside package for P).

With this routing, HFSS simulations have shown only 0.7° phase difference between P and N at 6 GHz.
This electrical compensation is not perfect because of board and package εr (relative permittivity) difference. HITCE package εr is 5.2 (higher value than for usual board).

4.4 Thermal characteristics

Table 12. Thermal characteristics

Parameter	Symbol	Value	Unit	Note
Thermal resistance from junction to bottom of balls	$Rth_{Junction\ to\ Bottom\ of\ balls}$	4.0	°C/Watt	(1)(2)
Thermal resistance from junction to board (JEDEC JESD51-8)	$Rth_{junction\ -\ board}$	5.5	°C/Watt	(1)(2)
Thermal resistance from junction to top of lid	$Rth_{Junction\ –\ lid}$	2.05	°C/Watt	(1)(2)
Thermal resistance from junction to ambient (JEDEC standard)	$Rth_{Junction\ –\ ambient}$	19.2	°C/Watt	(1)(3)
Delta temperature Hot spot – temperature from diode		+6.2	°C	

Notes:

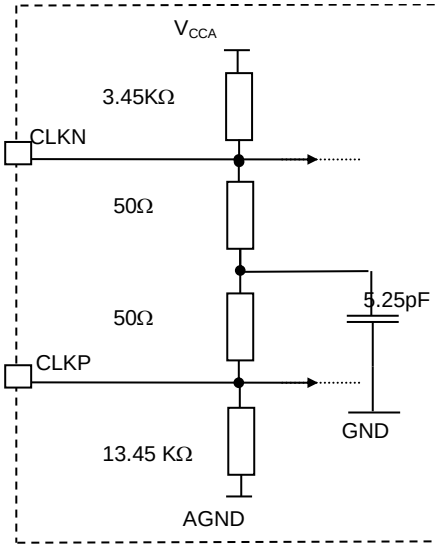
1. Rth are calculated from hot spot, not from average temperature of the die

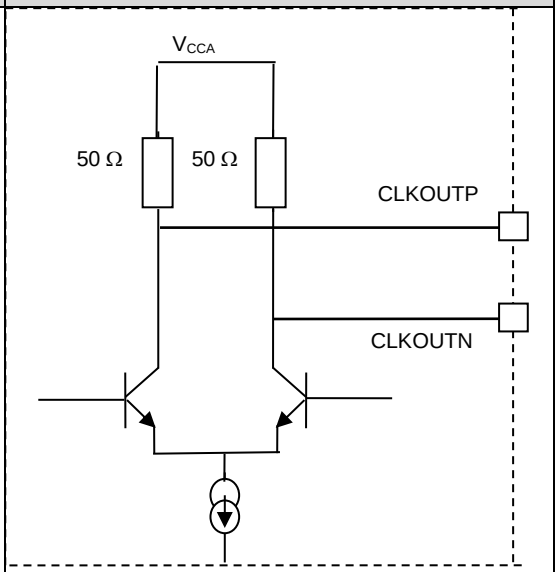
   These figures are thermal simulation results (finite elements method) with nominal cases.
2. Assumptions: no air, pure conduction, no radiation
3. Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 x 76.2 mm, 1.6 mm thickness

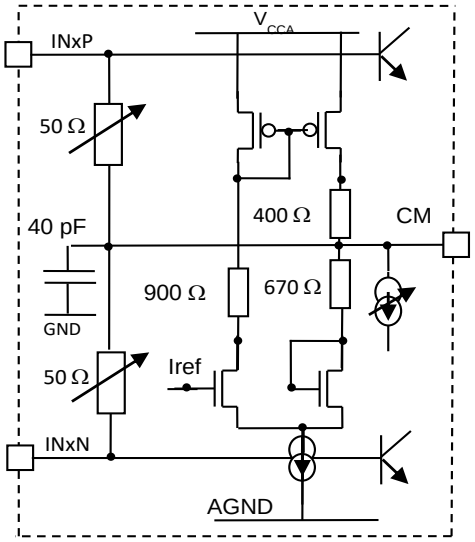
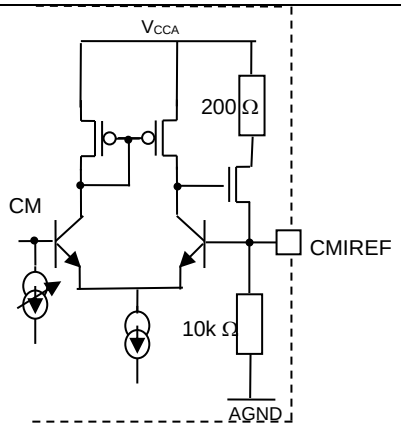
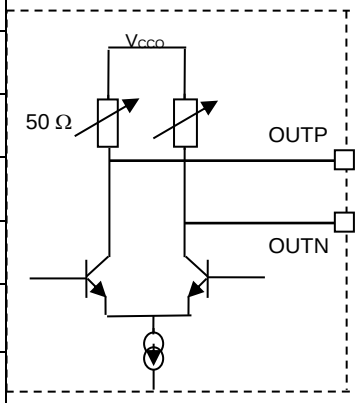
4.5 Pinout Table

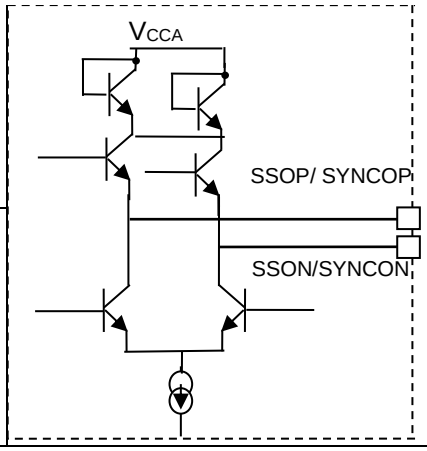
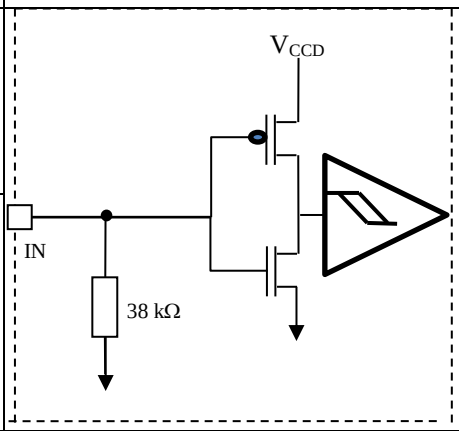
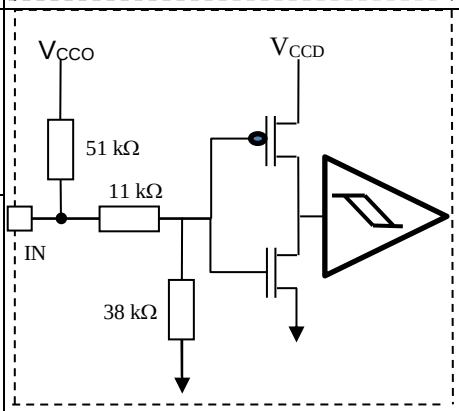
Table 13. Pinout Table

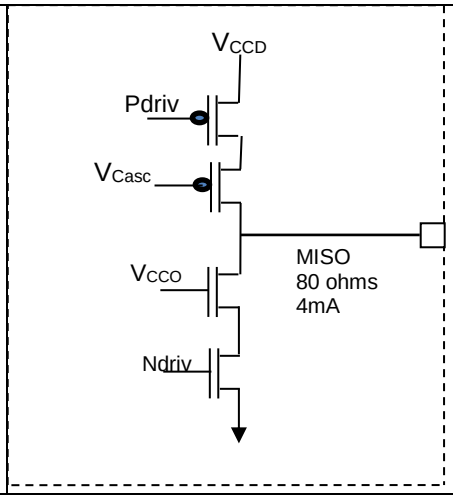
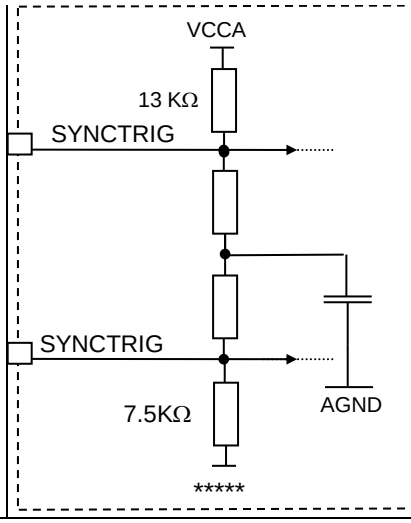
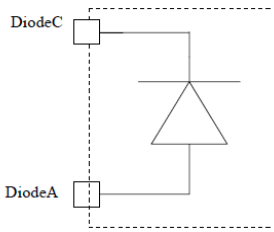
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
AGND	A2, A3, A6, A9, A10, A13, A16, A17; B3, B4, B5, B6, B7, B8, B9, B10, B11,B12, B13, B14, B15, B16; C5, C6, C7, C8, C9, C10, C11, C12, C15; D6, D7, D8, D9, D10, D11, D12, D13, D14; E7, E8, E11, E12 F7, F8, F9, F10, F11, F12; G7, G12; H7, H8, H11, H12; J7, J9, J10, J12; K7, K12; L7, L9, L10, L12; M7, M8, M11, M12; N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15; P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16; R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16; T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18; U1, U2, U3, U6, U9, U10, U13, U16, U17, U18; V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18;	Analog ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
DGND	A18; B1, B2, B17, B18; C4, C16, C17; D15; E6, E13; F6, F13; J6, J13; L6, L13;	Digital ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
GNDO	D1, D2, D17, D18; E1, E2, E3, E16, E17, E18; F3, F4, F15, F16; G1,G2, G3, G4, G15, G16, G17, G18; H3, H16;	Ground for Output buffers All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
	J1, J2, J3, J4, J5, J14, J15, J16, J17, J18; K3, K16; L1, L2, L3, L4, L5, L14, L15, L16, L17, L18; M3, M16 N1, N2, N3, N16, N17, N18; P1, P2, P17, P18;			
V_{CCA}	E9, E10; G8, G9, G10, G11; H9, H10; J8, J11; K8, K9, K10, K11; L8, L11; M9, M10;	Analog power supply		
V_{CC_SPI}	F5	SPI power supply (1.8V, 2.5V or 3.3V)		
V_{CCD}	F14; G6, G13; H6, H13; K6, K13; M6, M13;	Digital power supply		
V_{CCO}	H4, H5, H14, H15; K4, K5, K14, K15; M4, M5, M14, M15;	Output power supply		
Clock signal				
CLKP CLKN	A11, A12	In phase and Out of phase input clock signal	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
CLKOUTP CLKOUTN	A8, A7	In phase and Out of phase out clock signal	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Analog signals				
IN0P IN0N	U4, U5	In phase analog input 0 Out of phase analog input 0	I	
IN1P IN1N	U8, U7	In phase analog input 1 Out of phase analog input 1	I	
IN2P IN2N	U11, U12	In phase analog input 2 Out of phase analog i nput 2	I	
IN3P IN3N	U15, U14	In phase analog input 3 Out of phase analog input 3	I	
CMIREF	R18	Output voltage reference In AC coupling operation this output could be left floating (not used) In DC coupling operation, these pins provides an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	
Digital Output signals (CML)				
ASL0P, ASL0N	H1, H2	Channel A output data serial link 0	O	
ASL1P, ASL1N	F1, F2	Channel A output data serial link 1	O	
BSL0P, BSL0N	K1, K2	Channel B output data serial link 0	O	
BSL1P, BSL1N	M1, M2	Channel B output data serial link 1	O	
CSL0P, CSL0N	K18, K17	Channel C output data serial link 0	O	
CSL1P, CSL1N	M18, M17	Channel C output data serial link 1	O	
DSL0P, DSL0N	H18, H17	Channel D output data serial link 0	O	
DSL1P, DSL1N	F18, F17	Channel D output data serial link 1	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital output Signal (LVDS)				
SSOP, SSON	C14, C13	In phase and out of phase Slow Synchro Output.Fsso=Fclk/32	O	
SYNCOP, SYNCON	A5, A4	In phase and out of phase Sync Output.	O	
Digital I/0 (CMOS)				
V_{SPI_SEL}	C18	used for logical level selection		
Sclk	D5	SPI signal Input SPI serial Clock Serial data is shifted into and out SPI synchronously to this signal on positive transition of sclk Internal pull-down	I	
Mosi	C2	SPI signal Data SPI Input signal (Master Out Slave In) Serial data input is shifted into SPI while sldn is active low Internal pull-down	I	
Csn	D4	SPI signal Input Chip Select signal (Active low) When this signal is active low, sclk is used to clock data present on MOSI or MISO signal Internal pull-up	I	
Rstn	C3	SPI signal Input Digital asynchronous SPI reset (Active low) This signal allows to reset the internal value of SPI to their default value Internal pull-up	I	

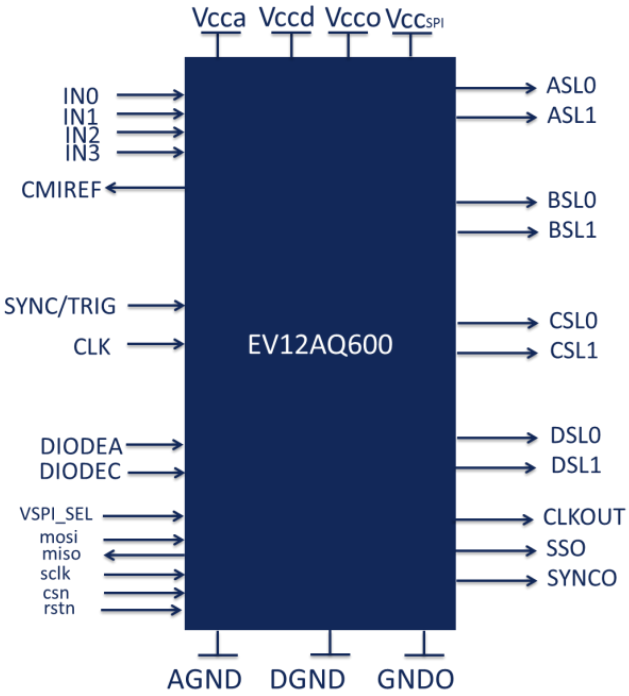
Miso	C1	SPI signal Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while csn is active low.	O	
DIGITAL INPUT (LVDS)				
SYNCTRIGP SYNCTRIGN	A14, A15	Differential Input Synchronization signal (LVDS) Active high signal This signal is used to synchronize internal ADC, if enabled Equivalent internal differential 100Ω input resistor Functionality SYNC or TRIG depends on SPI selection	I	
MISCELLANEOUS				
DiodeA, DiodeC	R2, R1	Junction Temperature Monitoring diode Anode Junction Temperature Monitoring diode Cathode Cathode must be connected to ground (AGND) externally	I	

5 THEORY OF OPERATION

Overview

Table 14. Functional description

Name	Function
V_{CCA}	Analog Power Supply
V_{CCD}	Digital Power Supply
V_{CCO}	Output buffer Power Supply
VCC_{SPI}	SPI Power Supply (1.8V or VCCO or VCCA)
V_{SPI_SEL}	Selection of SPI logical levels
AGND	Analog Ground
DGND	Digital Ground
GNDO	Ground for Output buffer
IN0P, IN0N	Differential Analog Input for ADC core A, core B, core C or core D (depending on cross point switch chosen configuration)
IN1P, IN1N	Differential Analog Input for ADC core B
IN2P, IN2N	Differential Analog Input for ADC core C
IN3P, IN3N	Differential Analog Input for ADC core A, core B, core C or core D
CLKP,CLKN	Differential Clock Input
ASL0P, ASL0N	Channel A output, serial link0 (CML)
ASL1P, ASL1N	Channel A output, serial link1 (CML)
BSL0P, BSL0N	Channel B output, serial link0 (CML)
BSL1P, BSL1N	Channel B output, serial link1 (CML)
CSL0P, CSL0N	Channel C output, serial link0 (CML)
CSL1P, CSL1N	Channel C output, serial link1 (CML)
DSL0P, DSL0N	Channel D output, serial link0 (CML)
DSL1P, DSL1N	Channel D output, serial link1 (CML)
csn	SPI Chip Select Input (Active Low)
rstn	SPI Asynchronous Reset Input (Active Low)
sclk	SPI Input Clock



mosi	SPI input Data (Master Out Slave In)
miso	SPI Output Data (Master In Slave Out)
CMIRef	Input common Mode reference
DIODEA, DIODEC	Diode Anode and Cathode Inputs for die junction temperature monitoring
CLKOUTP, CLKOUTN	Differential output clock (copy of CLK)
SSOP, SSON	Slow Synchro Output clock
SYNCTRIGP, SYNCTRIGN	LVDS input: Synchronization of Data Ready, or TRIGGER input depending on SPI selection
SYNCOP, SYNCON	Synchro output, resynchronized SYNCTRIG signal

The EV12AQ600 could be configured as follow:

- Both the analog inputs settings and the associated clocking mode (in phase or interleaved) of the 4 cores can be selected though the SPI.
- Test modes can be selected though the SPI.
- Factory calibration or custom calibration can be loaded though the SPI.

Refer to section 6 for registers description.

6 SERIAL PERIPHERAL INTERFACE (SPI)

The digital interface will be a standard SPI with:
- 16 bits for the address A[15] to A[0] including a R/W bit (A[15] = R/W, being A[15] is the MSB);
- 16 bits of data D[15] to D[0] with D[15] the MSB.

5 signals are required:
- RSTN for the SPI reset;
- SCLK for the SPI clock;
- CSN for the Chip Select;
- MISO for the Master In Slave Out SPI Output;
- MOSI for the Master Out Slave In SPI Input.

The MOSI sequence should start with one R/W bit (A[15]):
- R/W = 0 is a read procedure
- R/W = 1 is a write procedure

6.1 SPI logic compatibility

Logical levels of SPI Digital CMOS levels can be configured in 1.8V, 2.5V or 3.3V logic compatibility.
Table 15 presents the SPI pins configuration depending on expected logic level.
The selection of logic compatibility is done in settings appropriate voltage levels to pins VCC_{SPI} and V_{SPI_SEL}.
Default logic compatibility is 1.8V.

Table 15. SPI pins configuration depending on logic voltage required

Logic Level	VCC_{SPI} pin voltage	V_{SPI_SEL} pin voltage
1.8V	1.8V	0V (GND)
2.5V	2.5V	0V (GND)
3.3V	3.3V	3.3V

6.2 Timings

Register Write to a 16-bit register:

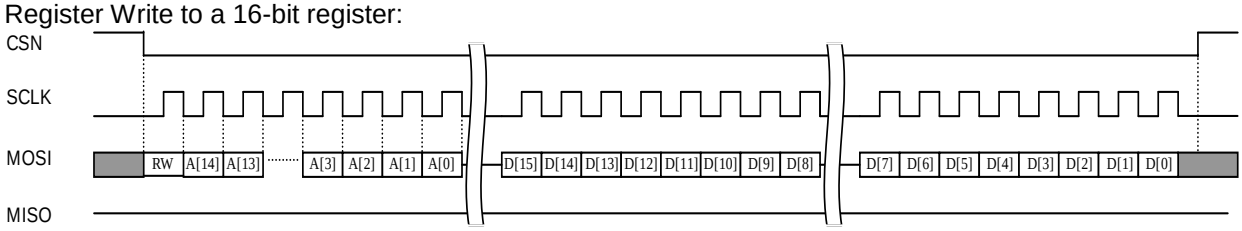


Figure 11 - SPI writing

Register Read from a 16-bit register:

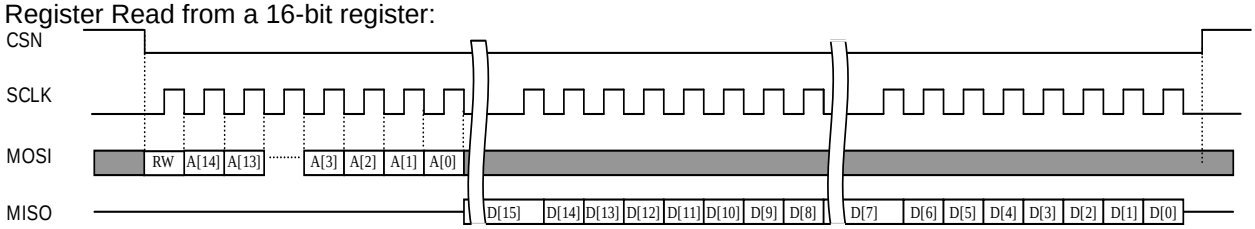


Figure 12 - SPI reading

See section 3.11 for SPI timing characteristics (max clock frequency…)

6.3 Register map

Table 16. SPI register map

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
OTP_LOADING	0x0001		The action of writing in this register causes the loading of OTP in secure SPI register	Table 30
EXTRA_SEE_PROTECT	0x0002	0	Additional protection against Single Event 0: major protection is available (default) 1: additional protection is available All SPI registers can't be access, except this registe SYNC is disabled The presence of the CLOCK SPI refreshes Triple Majority Redundancy registers	Table 33
SYNCO_SSO_CLKOUT_FULL_SWING_EN	0x0005	0	For all following bits : 0: reduced 1: full swing bit[1]= LVDS full swing on SSO and SYNCO bit[0]= CML CLKOUT full swing	Table 25
AB_HSSL_FULL_SWING_EN	0x0006	0	bit[0] 0: HSSL output swing is reduced (default) 1: full HSSL output swing	Table 26
CD_HSSL_FULL_SWING_EN	0x0007	0	bit[0] 0: HSSL output swing is reduced (default) 1: full HSSL output swing	Table 26
EXT_BW_DISABLE	0x0008	0	bit[0] 0: extended bandwidth (default) 1: nominal bandwidth	Table 20
CAL_SET_SEL	0x0009	0	bit[0]= INL calibration set selection 0: set 0 selected (default value) 1: set 1 selected (not defined) bit[2:1]= phase/gain/offset calibration set selection 00: set 0 selected 01: set 1 selected 10: set 2 selected 11: set 3 selected	Table 19
CLK_MODE_SEL	0x000A	0	bit[1:0]= clock control 11: clock A=B=C=D , all clocks are identical 10: clock A=C, clock B=D 01: clock A=B, clock C=D 00: all clocks are interleaved (default)	Table 18
CPS_CTRL	0x000B	0	1 channel mode 000 : input 0 to core A & B & C & D (default) 001 : input 3 to core A & B & C & D 2 channels mode 010 : input 0 to core A & B input 3 to core C & D 011 : input 0 to core C & D input 3 to core A & B 4 channels mode 100 : input 0 to core A input 1 to core B input 2 to core C input 3 to core D	Table 17
SYNC_CTRL	0x000C	0	bit[0] = **sync_edge** : Indicate system clock sampling edge for SYNC 0 : Positive edge 1 : Negative edge bit[2:1] = **sync_shift** : Add one(or more) system clock period on SYNC internal path	Table 23

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
			00 : No system clock period added 01 : One system clock period added 10 : two system clock periods added 11 : three system clock periods added	
SYNC_FLAG	0x000D	0	bit [0] = Indicate timing violation on SYNC bit [0] = 0 : SYNC has been correctly recovered bit [0] = 1 :Timing violation on SYNC	Table 21
SYNC_FLAG_RST	0x000E	0	bit [0] = 0 : reset the flag	Table 22
CHIP_ID	0x0011		Chip Identification number	Table 32
AB_HSSL_CFG	0x0013	18	bit[1:0]= DATA SELECTION FOR BIT[12] 00: IR selected (default) 01: TRIG selected (=> SYNC disabled) 10: TimeStamp selected 11: PARITY selected bit[3:2]= DATA SELECTION FOR BIT[13] 00: IR selected 01: TRIG selected (=> SYNC disabled) 10: TimeStamp selected (default) 11: PARITY selected bit[4]= LSB first enable 0: MSB first ‘ 1: LSB first (default)	Table 28
CD_HSSL_CFG	0x0014	18	Idem AB_HSSL_CFG	Table 28
AB_HSSL_POL	0x0015	06	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0]= Pin N/P configuration of serial output buffer 0 CHANNEL A bit[1]= Pin N/P configuration of serial output buffer 1 CHANNEL A bit[2]= Pin N/P configuration of serial output buffer 0 CHANNEL B bit[3]= Pin N/P configuration of serial output buffer 1 CHANNEL B	Table 27
CD_HSSL_POL	0x0016	09	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0]= Pin N/P configuration of serial output buffer 0 CHANNEL C bit[1]= Pin N/P configuration of serial output buffer 1 CHANNEL C bit[2]= Pin N/P configuration of serial output buffer 0 CHANNEL D bit[3]= Pin N/P configuration of serial output buffer 1 CHANNEL D	Table 27
OUTPUT_CLK_EN	0x0017	2	For all following bits : 0: disable 1: enable bit[0]= CLKOUT enable (disable by default) bit[1]= SSO enable (enable by default) bit[2]= SYNCO enable (disable by default)	Table 24
A_SET0_GAIN_CAL	0x0122	0800	A core Interleaving gain calibration	Table 41
A_SET0_PHASE_CAL	0x0123	0100	A core Interleaving phase calibration	Table 42
A_SET0_OFFSET_CAL	0x0124	0100	A core Interleaving offset calibration	Table 43
A_SET1_GAIN_CAL	0x0125	0800	A core Interleaving gain calibration	Table 41
A_SET1_PHASE_CAL	0x0126	0100	A core Interleaving phase calibration	Table 42
A_SET1_OFFSET_CAL	0x0127	0100	A core Interleaving offset calibration	Table 43
A_SET2_GAIN_CAL	0x0128	0800	A core Interleaving gain calibration	Table 41
A_SET2_PHASE_CAL	0x0129	0100	A core Interleaving phase calibration	Table 42

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
A_SET2_OFFSET_CAL	0x012A	0100	A core Interleaving offset calibration	Table 43
A_SET3_GAIN_CAL	0x012B	0800	A core Interleaving gain calibration	Table 41
A_SET3_PHASE_CAL	0x012C	0100	A core Interleaving phase calibration	Table 42
A_SET3_OFFSET_CAL	0x012D	0100	A core Interleaving offset calibration	Table 43
A_SDA_CTRL	0x012F	1000	A core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)	Table 35
B_SET0_GAIN_CAL	0x0322	0800	B core Interleaving gain calibration	Table 41
B_SET0_PHASE_CAL	0x0323	0100	B core Interleaving phase calibration	Table 42
B_SET0_OFFSET_CAL	0x0324	0100	B core Interleaving offset calibration	Table 43
B_SET1_GAIN_CAL	0x0325	0800	B core Interleaving gain calibration	Table 41
B_SET1_PHASE_CAL	0x0326	0100	B core Interleaving phase calibration	Table 42
B_SET1_OFFSET_CAL	0x0327	0100	B core Interleaving offset calibration	Table 43
B_SET2_GAIN_CAL	0x0328	0800	B core Interleaving gain calibration	Table 41
B_SET2_PHASE_CAL	0x0329	0100	B core Interleaving phase calibration	Table 42
B_SET2_OFFSET_CAL	0x032A	0100	B core Interleaving offset calibration	Table 43
B_SET3_GAIN_CAL	0x032B	0800	B core Interleaving gain calibration	Table 41
B_SET3_PHASE_CAL	0x032C	0100	B core Interleaving phase calibration	Table 42
B_SET3_OFFSET_CAL	0x032D	0100	B core Interleaving offset calibration	Table 43
B_SDA_CTRL	0x032F	1000	B core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)	Table 35
C_SET0_GAIN_CAL	0x0522		C core Interleaving gain calibration	Table 41
C_SET0_PHASE_CAL	0x0523		C core Interleaving phase calibration	Table 42
C_SET0_OFFSET_CAL	0x0524		C core Interleaving offset calibration	Table 43
C_SET1_GAIN_CAL	0x0525		C core Interleaving gain calibration	Table 41
C_SET1_PHASE_CAL	0x0526		C core Interleaving phase calibration	Table 42
C_SET1_OFFSET_CAL	0x0527		C core Interleaving offset calibration	Table 43
C_SET2_GAIN_CAL	0x0528		C core Interleaving gain calibration	Table 41
C_SET2_PHASE_CAL	0x0529		C core Interleaving phase calibration	Table 42
C_SET2_OFFSET_CAL	0x052A		C core Interleaving offset calibration	Table 43
C_SET3_GAIN_CAL	0x052B		C core Interleaving gain calibration	Table 41
C_SET3_PHASE_CAL	0x052C		C core Interleaving phase calibration	Table 42
C_SET3_OFFSET_CAL	0x052D		C core Interleaving offset calibration	Table 43
C_SDA_CTRL	0x052F	1000	C core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)	Table 35
D_SET0_GAIN_CAL	0x0722		D core Interleaving gain calibration	Table 41
D_SET0_PHASE_CAL	0x0723		D core Interleaving phase calibration	Table 42
D_SET0_OFFSET_CAL	0x0724		D core Interleaving offset calibration	Table 43

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
D_SET1_GAIN_CAL	0x0725		D core Interleaving gain calibration	Table 41
D_SET1_PHASE_CAL	0x0726		D core Interleaving phase calibration	Table 42
D_SET1_OFFSET_CAL	0x0727		D core Interleaving offset calibration	Table 43
D_SET2_GAIN_CAL	0x0728		D core Interleaving gain calibration	Table 41
D_SET2_PHASE_CAL	0x0729		D core Interleaving phase calibration	Table 42
D_SET2_OFFSET_CAL	0x072A		D core Interleaving offset calibration	Table 43
D_SET3_GAIN_CAL	0x072B		D core Interleaving gain calibration	Table 41
D_SET3_PHASE_CAL	0x072C		D core Interleaving phase calibration	Table 42
D_SET3_OFFSET_CAL	0x072D		D core Interleaving offset calibration	Table 43
D_SDA_CTRL	0x072F	1000	D core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)	Table 35
IN0_IN1_CMIREF	0x0905	14	Input common mode calibration for IN0 & IN1 analog inputs	Table 38
IN2_IN3_CMIREF	0x0906	14	Input common mode calibration for IN2 & IN3 analog inputs	Table 38
IN0_IN1_RIN	0x0907	10	Input impedance calibration for IN0 & IN1 analog inputs	Table 39
IN2_IN3_RIN	0x0908	10	Input impedance calibration for IN2 & IN3 analog inputs	Table 39
AB_ROUT_HSSL	0x0909	55	CALIBRATION R LOAD CML bit[1:0]= R_cml0 channel A (for link0) bit[3:2]= R_cml1 channel A (for link1) bit[5:4]= R_cml0 channel B (for link0) bit[7:6]= R_cml1 channel B (for link1)	Table 40
CD_ROUT_HSSL	0x090A	55	CALIBRATION R LOAD CML bit[1:0]= R_cml0 channel C (for link0) bit[3:2]= R_cml1 channel C (for link1) bit[5:4]= R_cml0 channel D (for link0) bit[7:6]= R_cml1 channel D (for link1)	Table 40
DATA_MODE_SEL	0x0B07	7	For all following bits : 0: disable 1: enable bit[0] = PRBS enable bit[1] = DATA enable (0 means DATA=0) bit[2] = DC-Balance enable	Table 30
TEST_MODE	0x0B0A	0	For all following bits : 0: disable 1: enable bit[0]= ramp mode bit[1]= force VOH bit[2]= force VOL bit[3]= force decimation (/4)	Table 30
A_CALC_OTP_CRC	0x0B0B		CRC calculated after a OTP loading	Table 31
B_CALC_OTP_CRC	0x0B0C		CRC calculated after a OTP loading	Table 31
C_CALC_OTP_CRC	0x0B0E		CRC calculated after a OTP loading	Table 31
D_CALC_OTP_CRC	0x0B0F		CRC calculated after a OTP loading	Table 31
E_CALC_OTP_CRC	0x0B29		CRC calculated after a OTP loading	Table 31
F_CALC_OTP_CRC	0x0B2A		CRC calculated after a OTP loading	Table 31
A_OTP_CRC	0x0B14		CRC OTP reading	Table 31

Registers Names	@ hex	Default value hex	COMMENT	Refer to Table
B_OTP_CRC	0x0B15		CRC OTP reading	Table 31
C_OTP_CRC	0x0B17		CRC OTP reading	Table 31
D_OTP_CRC	0x0B18		CRC OTP reading	Table 31
E_OTP_CRC	0x0B2B		CRC OTP reading	Table 31
F_OTP_CRC	0x0B2C		CRC OTP reading	Table 31
AB_POWER_ON_PACK	0x0B02	FF	Power ON for A,B cores	Table 45
CD_POWER_ON_PACK	0x0B03	FF	Power ON for A,B cores	Table 45
AB_HSSL_POWER_ON	0x0B00	3	A,B Serial links Power ON	Table 46
CD_HSSL_POWER_ON	0x0B01	3	C,D Serial links Power ON	Table 46
CPS_POWER_ON	0x0B04	1	CPS_POWER_ON	Table 47
AB_HSSL_IO_POWER_ON	0x0B05	F	A,B CML ouput Buffers_POWER_ON	Table 48
CD_HSSL_IO_POWER_ON	0x0B06	F	C,D CML ouput Buffers_POWER_ON	Table 48

6.4 Digital Reset and start up procedure

RSTN is an asynchronous active low global reset for the SPI and OTP (One Time Programmable registers). It is mandatory to put RSTN at low level during a minimum of 10 µs at power-up of the device. It sets all SPI registers to their default values. The SPI interface can be used or not; if it is not used, the OTP value and default SPI configurations will be automatically loaded.

Figure 13 presents the reset and synchronization to realize after power-up when the SPI is used (see section Serial Peripheral Interface (SPI) for more information on the SPI interface).

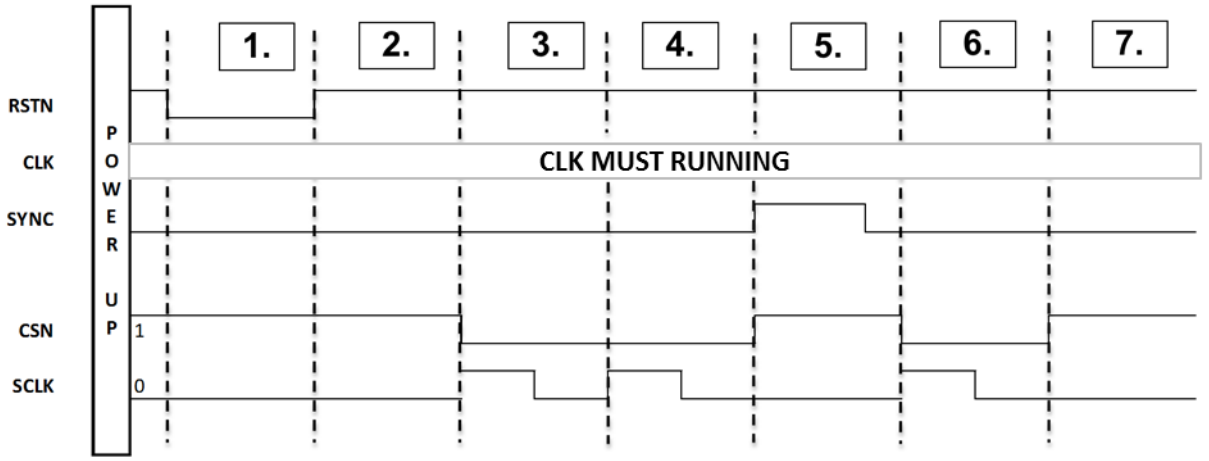


Figure 13 – Start-up sequence when using the SPI interface

- **1.** It is mandatory to reset the device at power-up through RSTN. It is active low and the pulse must be at least 10 µs. During the RSTN pulse, CSN must be held high and SCLK held low. The CLK must be provided before the RSTN pulse. The CLK can start before or after the power-up.
- **2.** The fuses need 1 ms to wake up.
- **3.** The SPI instruction WRITE @0x0001 =0b1 must be sent to the ADC. The OTP are loaded into the SPI registers at this point. There must be at least 1 ms between the RSTN pulse and this SPI instruction;
- **4.** The ADC is configured through the SPI interface.
- **5.** A pulse is applied onto the SYNCTRIG input to reset the internal clocks (SYNC signal in Figure 13). At this stage, the trigger mode is disabled.
- **6.** The ADC can be configured in trigger mode enable and the EXTRA_SEE_PROTECT register can be activated – see section 6.15.
- **7.** Normal operation of the ADC.

6.5 ADC Synchronization Signal (SYNCTRIGP, SYNCTRIGN)

The SYNCTRIGP, SYNCTRIGN LVDS inputs deliver SYNC signal for synchronization or TRIGGER signal for triggering data. This section focused on using the SYNC signals.

Since SYNC is multiplexed with TRIGGER, to perform synchronization, the ADC must be configured in synchronization mode. The SYNC function is enabled by default. Refer to AB_HSSL_CFG and CD_ HSSL_CFG registers in Table 28.

The SYNC signal is mandatory in order to have a deterministic timing for the 4 core synchronization (clock tree and digital reset) and for multiple ADCs time alignment.

It is asynchronous regarding the external clock. It is active high and should be compliant with the timing shown in the chronograms of Figure 13 and specified in Table 8 to work properly. It becomes effective on the rising edge of SYNCTRIGP, SYNCTRIGN.

6.6 Cross-point switch (CPS)

CPS functionality enables different input configurations by switching the signal to the dedicated core (A, B, C or D). IN0 and IN3 can address any core. IN1and IN2 must be connected to core B and C if used, as described on the Figure 14 below:

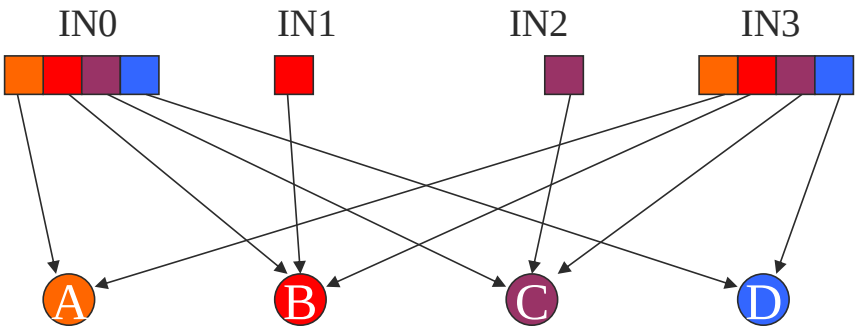


Figure 14 – CPS configurations

To interleave A to D cores, IN0 input can be used and register CPS_CTRL has to be set to 0. The right clock distribution has to be chosen (see section 6.7).
Different CPS capabilities are described in register CPS_CTRL.

.

Table 17. CPS_CTRL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
													CPS_CTRL		

Register Name	@	Type	Size	Default Value	Core	Comment
CPS_CTRL	0x000B	RW	3	0b0	All	1 channel mode 000 : input 0 to core A & B & C & D (default) 001 : input 3 to core A & B & C & D 2 channels mode 010 : input 0 to core A & B input 3 to core C & D 011 : input 0 to core C & D input 3 to core A & B 4 channels mode 100 : input 0 to core A input 1 to core B input 2 to core C input 3 to core D

6.7 Clock interleaving

Core A to D could be addressed one to one or interleaved two by two or all four together to reach 6.4GSps. A dedicated register (CLK_MODE_SEL) has to be used to provide the right clock behavior to each core.

Table 18. CLK_MODE_SEL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
														CLK_MODE_SEL	

Register Name	@	Type	Size	Default Value	Core	Comment
CLK_MODE_SEL	0x000A	RW	2	0b00	All	bit[1:0]= clock control 11: clock A=B=C=D , all clocks are in phase 10: clock A=C, clock B=D 01: clock A=B, clock C=D 00: all clocks are interleaved (default)

Detailed clocks chronograms for each configuration are given in Figure 15 to Figure 18.

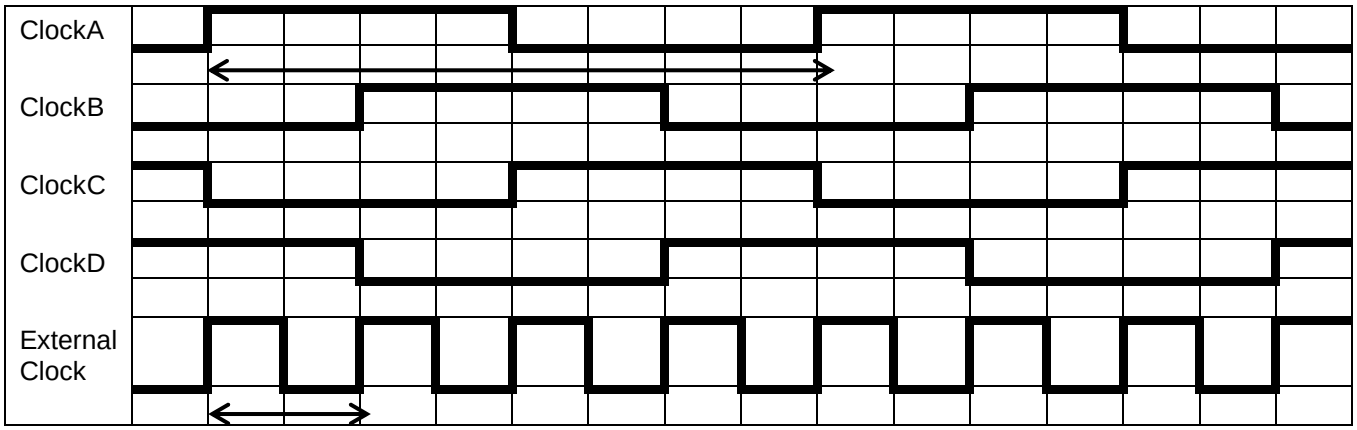


Figure 15 - Clocks for four cores interleaved
CLK_MODE_SEL = 0

Above clocks mode configuration has to be associated with the case one Input IN0 (or IN3) of the CPS.

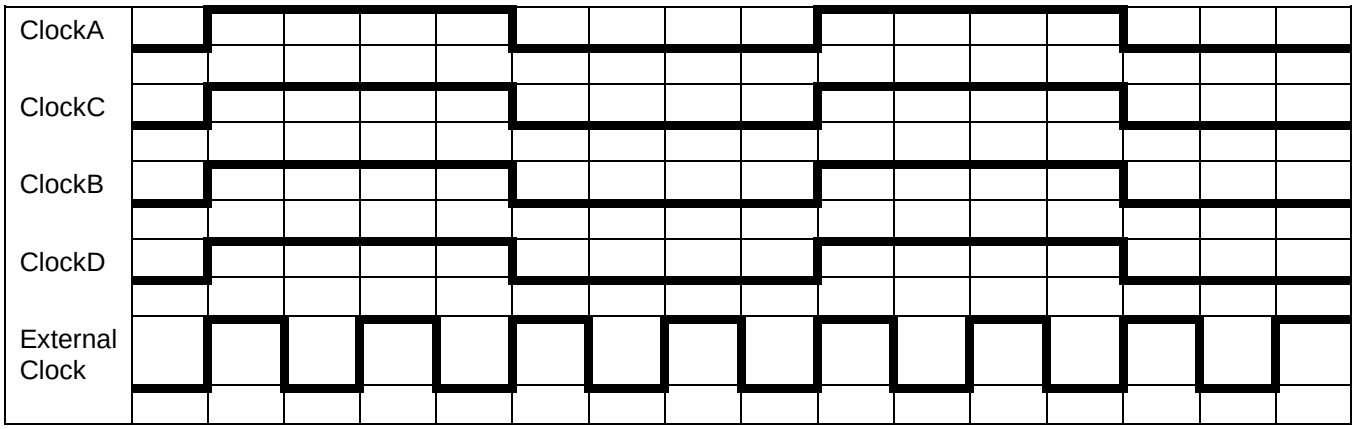


Figure 16 - Clocks for four cores aligned: averaging or four channels, CLK_MODE_SEL = 3

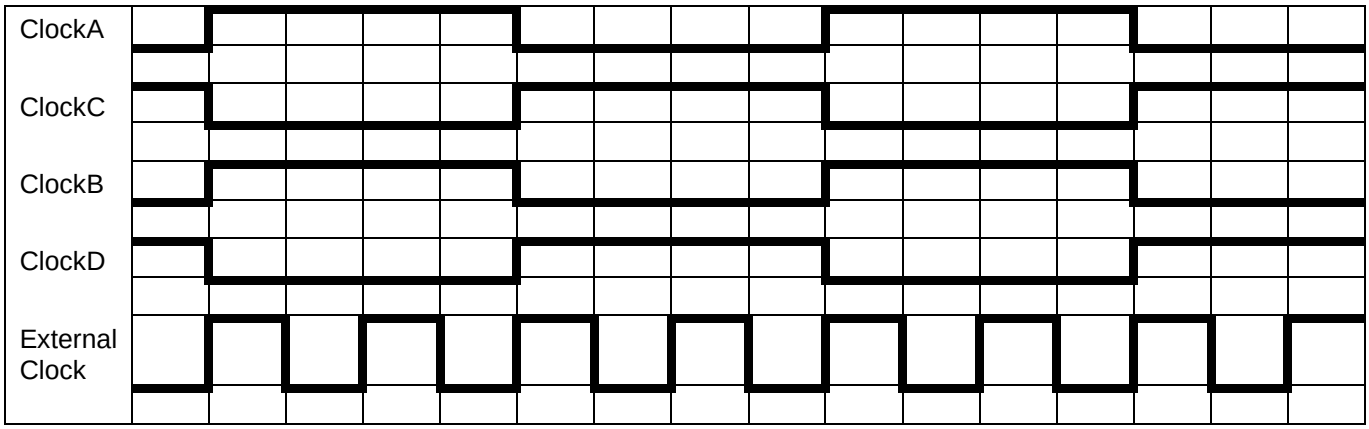


Figure 17 - Clocks for two cores interleaving – configuration 1: Interleaved of A and B, and interleaved of C and D CLK_MODE_SEL = 1

In this configuration, IN0 and IN3 inputs are used: IN0 provides signal to two cores while IN3 provides the two other cores input.

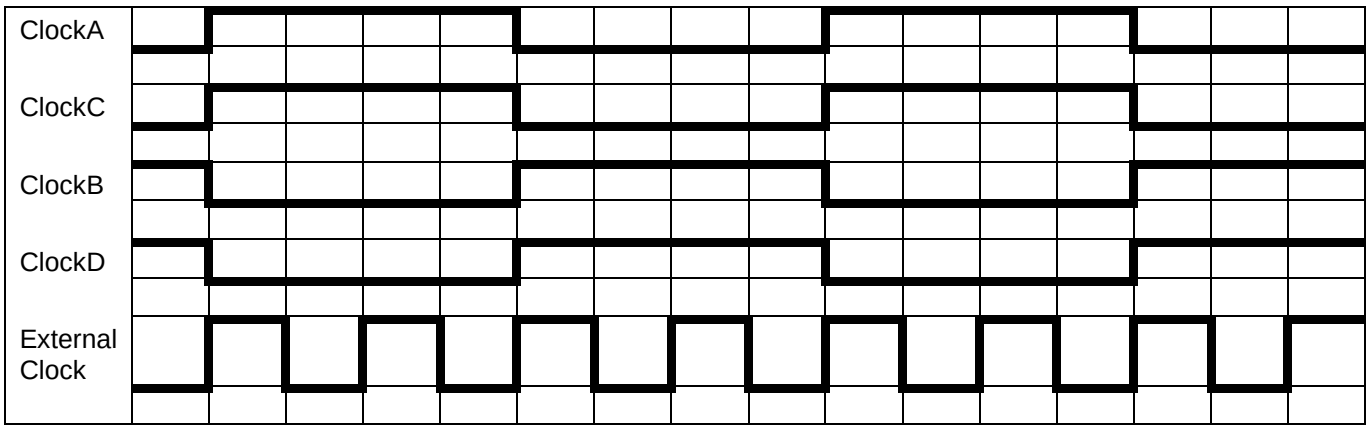


Figure 18 - Clocks for two cores interleaving – configuration 2: Interleaving of A and C, and interleaving of B and D CLK_MODE_SEL = 2

6.8 Calibration selection

The device contains 4 calibration sets (predefined manufacturing calibrations).
These sets address interleaving Gain, Phase and Offset registers. They ensure optimal interleaving performance depending on the condition of use (see section 8.3 for detailed specifications).

One set is selected thanks to CAL_SET_SEL register.

Table 19. CAL_SET_SEL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
													CAL_SET_SEL		Reserved

Register Name	@	Type	Size	Default Value	Core	Comment
CAL_SET_SEL	0x0009	RW	3	0b000	All	bit [0]= reserved bit[2:1]= phase/gain/offset calibration set selection 00: set 0 selected (2230MHz, 60°C) 01: set 1 selected (2230MHz, 100°C) 10: set 2 selected (100MHz, 60°C) 11: set 3 selected (100MHz, 100°C)

6.9 Analog bandwidth

The ADC core Analog Bandwidth can be selected thanks to EXT_BW_DISABLE register (refer to dynamic characteristic on Table 6).

Table 20. EXT_BW_DISABLE register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															EXT_BW_DISABLE

Register Name	@	Type	Size	Default Value	Core	Comment
EXT_BW_DISABLE	0x0008	W	1	0b0	All	bit[0]= 0: extended bandwidth (default) 1: nominal bandwidth

6.10 SYNC, slow and fast output clocks (SSO, CLKOUT)

To use the SYNC signal internally, it should first be sampled by the internal clock. Though, as the SYNC is asynchronous, it may lead to metastability when the internal sampling clock edge is simultaneous with the SYNC signal transition. To prevent this phenomenon, different SPI registers have to be used.

SYNC_FLAG indicates whether the SYNC has been correctly recovered by the system clock or not.

Table 21. SYNC_FLAG register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_FLAG	0x000D	R	1	0b0	All	bit [0] = Indicate timing violation on SYNC 0 : SYNC has been correctly recovered 1 :Timing violation on SYNC

The flag is reset by a reading of SYNC_FLAG_RST register:

Table 22. SYNC_FLAG_RST register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_FLAG_RST	0x000E	W	1	0b0	All	bit [0] = 0 : reset the flag

Two other SYNC_CTRL register's bits are used to configure the ADC. The first one, described in Table 23, is the sync_edge. It indicates to the ADC the system clock edge to use in order to recover it. The other one is the sync_shift, helpfull to add one to three external clock delays before resetting the ADC timing. Thanks to these registers, the ADC timing can be reset and multiple ADCs can be synchronized.

Table 23. SYNC_CTRL register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNC_CTRL	0x000C	W	3	0b00	All	bit[0] = **sync_edge**:Indicate system clock sampling edge for SYNC 0 : Positive edge 1 : Negative edge bit[2:1] = **sync_shift** : Add one(or more) system clock period on SYNC internal path 00 : No system clock period added 01 : One system clock period added 10 : two system clock periods added 11 : three system clock periods added

The slow output clock SSO (used in synchronization, frequency generation and as reference clock for serial link receiver) is not affected by SYNCTRIGP, SYNCTRIGN (not interrupted). It is an LVDS output generated by a 32 times division of the input clock.

The SYNC signal also starts the synchronization sequence of the serial interface.
CLKOUT is an output clock signal provided by the circuit as a clock reference to other ADCs. It has the same frequency as input clock CLKP, CLKN. The output signals SYNCOP, SYNCON result from the sampling of SYNCTRIGP, SYNCTRIGN signals by the system clock.

In order to reach deterministic resynchronization of several ADCs, it is recommended to chain the SYNC of ADC part N on the SYNCO of ADC part N-1. By this way, the delay between the different ADCs will be deterministic, and SYNC tree is still possible.

SYNCO, CLKOUT or SSO signals can be deactivated to save power when multiple ADC chaining is not used. The deactivation is done though OUTPUT_CLK_EN register:

Table 24. OUTPUT_CLK_EN register description

Register Name	@	Type	Size	Default Value	Core	Comment
OUTPUT_CLK_EN	@0x0017	W	3	0b010	All	For all following bit : 0: disable 1: enable bit[0]= CLKOUT enable (disable by default) bit[1]= SSO enable (enable by default) bit[2]= SYNCO enable (disable by default)

The signals swing can be reduced to save power though SYNCO_SSO_CLKOUT_FULL_SWING_EN register:

Table 25. SYNCO_SSO_CLKOUT_FULL_SWING_EN register description

Register Name	@	Type	Size	Default Value	Core	Comment
SYNCO_SSO_CLKOUT_FULL_SWING_EN	@0x0005	W	2	0b00	All	For all following bit : 0: reduced 1: full swing bit[1]= LVDS full swing on SSO and SYNCO bit[0]= CML CLKOUT full swing

6.11 Serial link output configuration

6.11.1 Serial link output swing and polarity configuration

IO‘s consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing capability, it is possible to reduce the output dynamic and so the consumption by using “swing adjust”. IO’s consumption can be reduced by 1/3.
Note: CLKOUT, SSO, SYNCO and serial link buffers (HSSL links) have independent dynamic settings. Refer to registers of Table 25 for CLKOUT, SSO and SYNCO swing setting.
The configuration is done via registers AB_HSSL_FULL_SWING_EN and CD_HSSL_FULL_SWING_EN.

Table 26. AB_HSSL_FULL_SWING_EN and CD_HSSL_FULL_SWING_EN registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															AB_HSSL_FULL_SWING_EN CD_HSSL_FULL_SWING_EN

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_FULL_SWING_EN	0x0006	W	1	0b0	A, B	bit[0]= 0: HSSL output swing is reduced (default) 1: full HSSL output swing
CD_HSSL_FULL_SWING_EN	0x0007	W	1	0b0	C, D	bit[0]= 0: HSSL output swing is reduced (default) 1: full HSSL output swing

It is also possible to invert the polarity of serial links outputs thanks to registers AB_HSSL_POL and CD_HSSL_POL.

Table 27. AB_HSSL_POL and CD_HSSL_POL registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
												AB_HSSL_POL CD_HSSL_POL			

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_POL	0x0015	W	4	0b110	A, B	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0]= Pin N/P configuration of serial output buffer 0 CHANNEL A bit[1]= Pin N/P configuration of serial output buffer 1 CHANNEL A bit[2]= Pin N/P configuration of serial output buffer 0 CHANNEL B bit[3]= Pin N/P configuration of serial output buffer 1 CHANNEL B
CD_HSSL_POL	0x0016	W	4	0b110	C, D	For all following bits : 0: Pin N/P default 1: Pin N and P reversed bit[0]= Pin N/P configuration of serial output buffer 0 CHANNEL C bit[1]= Pin N/P configuration of serial output buffer 1 CHANNEL C bit[2]= Pin N/P configuration of serial output buffer 0 CHANNEL D bit[3]= Pin N/P configuration of serial output buffer 1 CHANNEL D

When these options are set, samples are output on serial links in one channel interleaved mode according to the timing diagram on Figure 19:

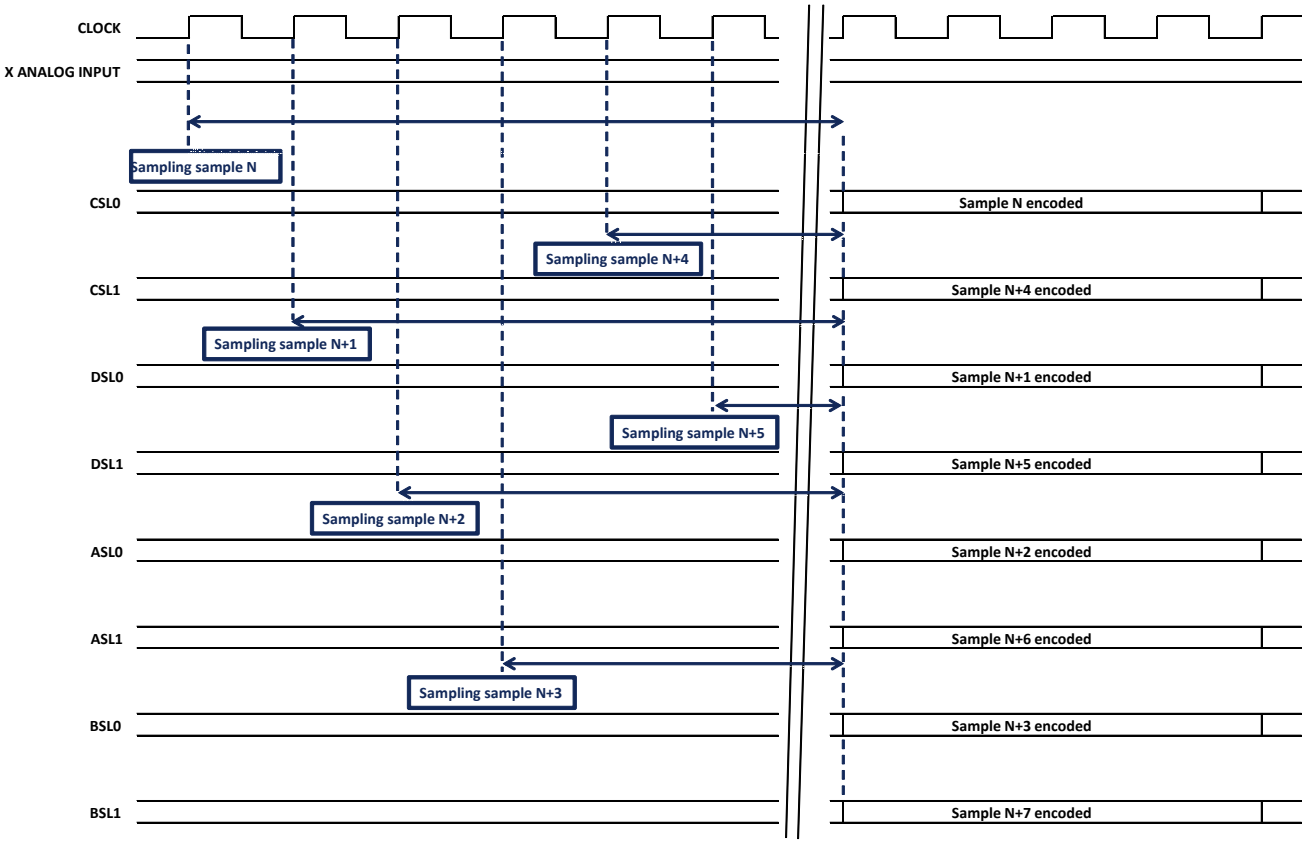


Figure 19 - Timing diagram in serial interface in 1-channel mode

In dual interleaved mode, to reconstruct the output signal, BA (or CD) samples have to be considered such as on Figure 20:

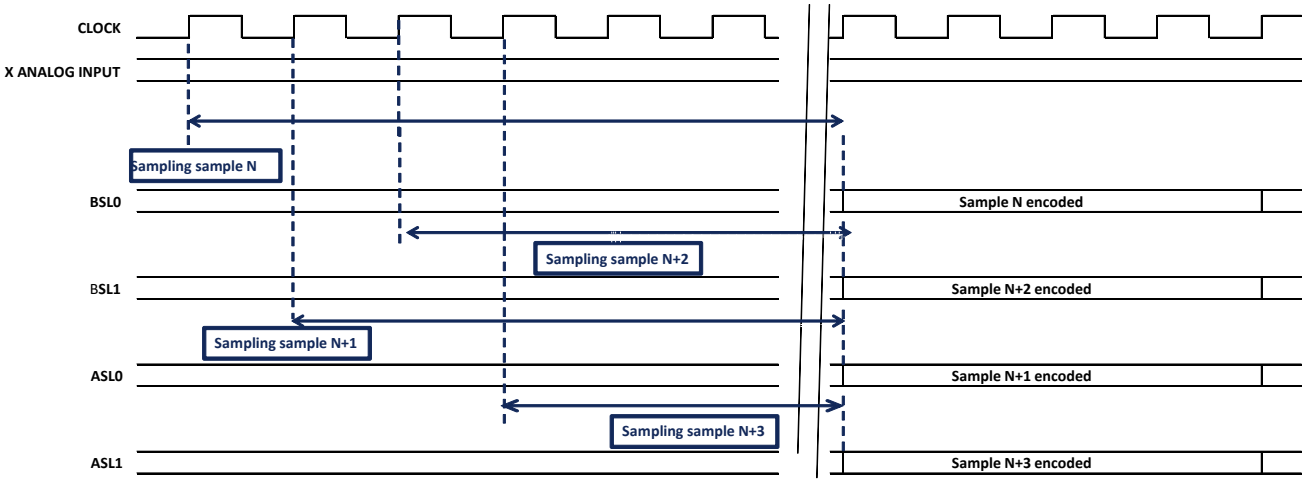


Figure 20 - Timing diagram in serial interface in 2-channel mode

6.11.2 Serial link In Range, Trigger, Timestamp, Parity and bit order configuration

It is possible to select the function of CB1 and CB2 (bit 12 and 13) of serial links among In Range, Trigger, Timestamp or parity bit. For more information on CB1 and CB2, see paragraph □.
The converted data (bit[11:0]) can be set either MSB first or LSB first by means of bit[4] of this register.

Table 28. AB_HSSL_CFG and CD_HSSL_CFG registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											AB_HSSL_CFG CD_HSSL_CFG				

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_CFG	0x0013	W	5	0b11000	A, B	bit[1:0]= DATA SELECTION FOR CB1 00: INRANGE selected (default) 01: TRIG selected (=> SYNC disabled) 10: TIMESTAMP selected 11: PARITY selected bit[3:2]= DATA SELECTION FOR CB2 00: INRANGE selected 01: TRIG selected (=> SYNC disabled) 10: TIMESTAMP selected (default) 11: PARITY selected bit[4]= LSB first enable 0: MSB first 1: LSB first (default)
CD_HSSL_CFG	0x0014	W	5	0b11000	C, D	bit[1:0]= DATA SELECTION FOR CB1 00: INRANGE selected (default) 01: TRIG selected (=> SYNC disabled) 10: TIMESTAMP selected 11: PARITY selected bit[3:2]= DATA SELECTION FOR CB2 00: INRANGE selected 01: TRIG selected (=> SYNC disabled) 10: TIMESTAMP selected (default) 11: PARITY selected bit[4]= LSB first enable 0: MSB first 1: LSB first (default)

6.11.3 Decimation

Figure 21 shows how the data is outputted on the 2 serial links of each ADC core, xSL0 & xSL1 where x can be A, B, C or D. Link0 outputs data N+2k while link1 outputs data N+(2k+1) (with k ∈|N).

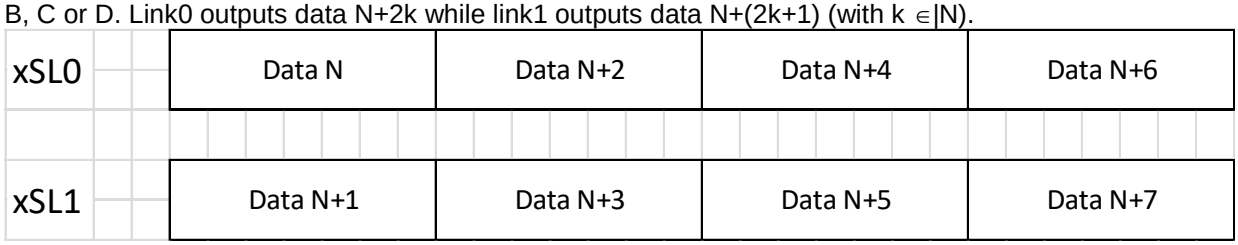


Figure 21: Output data on each serial link.

Powering down one of the links provides a simple way to decimate the output data flow by 2 while lowering power consumption.

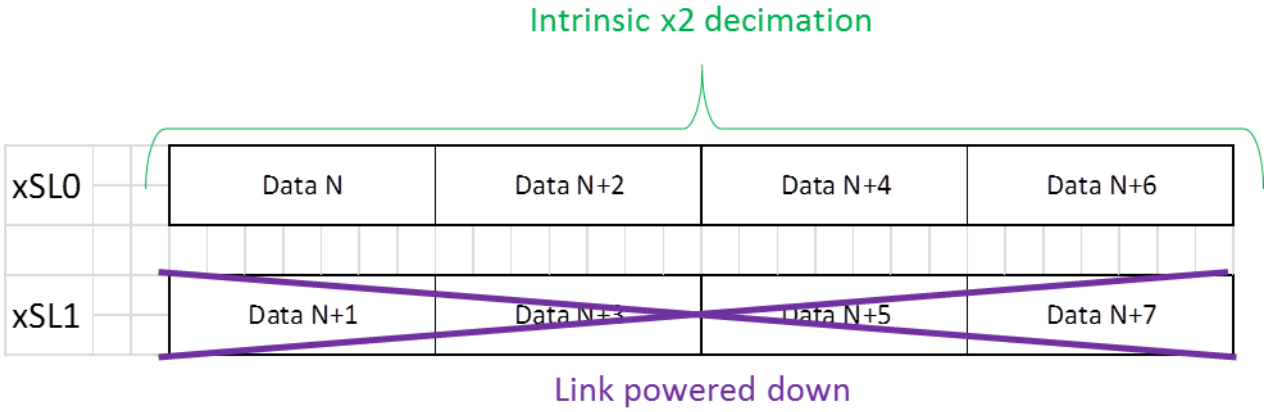


Figure 22: Powering down 1 link gives a x2 decimation.

Serial link can be powered down by using the registers described in Table 29

Table 29. AB_HSSL_IO_ POWER_ON and CD_HSSL_IO_ POWER_ON registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											AB_HSSL_IO_POWER_ON CD_HSSL_IO_POWER_ON				

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_IO_POWER_ON	0x0B05	RW	4	0b1111	A, B	0: power OFF 1: power ON CMLx : Serial link buffer bit[0] = power_on CML0 channel A bit[1] = power_on CML1 channel A bit[2] = power_on CML0 channel B bit[3] = power_on CML1 channel B
CD_HSSL_IO_POWER_ON	0x0B06	RW	4	0b1111	C, D	0: power OFF 1: power ON CMLx : Serial link buffer bit[0] = power_on CML0 channel C bit[1] = power_on CML1 channel C bit[2] = power_on CML0 channel D bit[3] = power_on CML1 channel D

6.11.4 Trigger mode

The SYNCTRIG input is an LVDS signal. It can be used in 2 different modes controlled through SPI: either in SYNC mode (refer to section 6.5) or in TRIGGER mode. To set it in TRIGGER mode, at least one of the control bit setting of register AB_HSSL_CFG and CD_HSSL_CFG must be set to TRIG (refer to Table 28). The trigger bit is a copy of the SYNCTRIG input with the same pipeline delay as the sampled data (refer to timing diagram in the figure below).

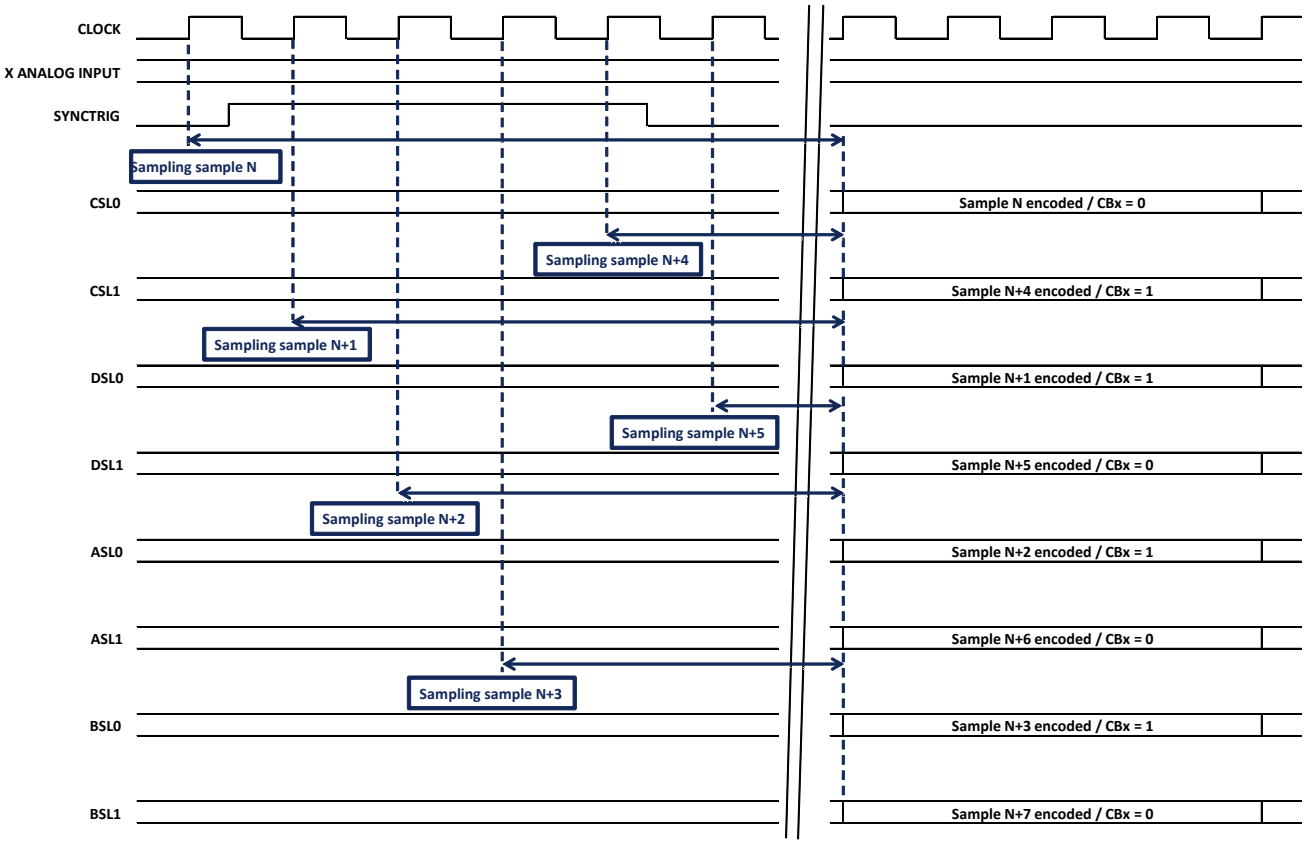


Figure 23 - Trigger mode timing diagram in serial interface

6.11.5 Parity bit

The parity of the 12 output bits of each data is calculated by performing an XOR combination between the 12 bits of output data. It is outputted at the same time than the 12-bits data. It is multiplexed with the in range and trigger bits. This function is selectable though AB_HSSL_CFG and CD_HSSL_CFG registers (refer to Table 28). By default, this function is not activated.

6.11.6 In-range bit

The “in-range” bit indicates whether the input signal is in the ADC dynamic range or not. When the ADC input signal is over the ADC dynamic range, the “in-range” bit is low. It is multiplexed with the parity and trigger bits.
This function is selectable AB_HSSL_CFG and CD_HSSL_CFG registers (refer to Table 28). By default, this function is activated.

6.11.7 TIMESTAMP

The timestamp control bit is a PRBS sequence that is updated with every frame. It is the same sequence for all links and is reset upon receiving a SYNCTRIG pulse. The PRBS sequence is based on an LFSR of Galois architecture with the polynomial X^7+X^6+1. It can be used to identify the samples order and/or check the synchronization of the serial interface.
This function is selectable AB_HSSL_CFG and CD_HSSL_CFG registers (refer to Table 28). By default, this function is activated.

6.12 Test modes and Data modes

Multiple test modes are available and can be generated by the ADC:
- PRBS : generates a pseudo-random binary sequence on the output
- Ramp : generates a ramp on the output

See below the registers used to enable or disable the different test modes:

Table 30. TEST_MODE & DATA_MODE_SEL registers description

Register Name	@	Type	Size	Default Value	Core	Comment
TEST_MODE	@0x0B0A	W	4	0b0000	All	For all following bits : 0: disable 1: enable bit[0]= ramp mode
DATA_MODE_SEL	@0x0B07	W	3	0b111	All	For all following bits : 0: disable 1: enable (default) bit[0] = PRBS enable bit[1] = DATA enable (0 means DATA=0) bit[2] = DC-Balance enable

6.12.1 PRBS

Pseudo Random Bit Sequence can be generated for output. It can be:
- Deactivated
- Added to data (PRBS+data)
- Outputted without data

This pseudo-random test mode is encoded with ESIstream protocol (see section 9).

6.12.2 Ramp mode

In ramp mode, the data encoded corresponds to a 12 bit ramp value with only the even values on lane 1 and the odd values on lane 2.

See below the chronogram of the ramp test mode. The data shown in the following figure 24 only presents the 14bit data from the ADC (12 bit sample values plus 2 control bits CB1 and CB2) and does not include the encoding of the ESIstream protocol which is used on the serial interface, in order to understand the ramp test mode (for more information on CB1 and CB2, see paragraph □).

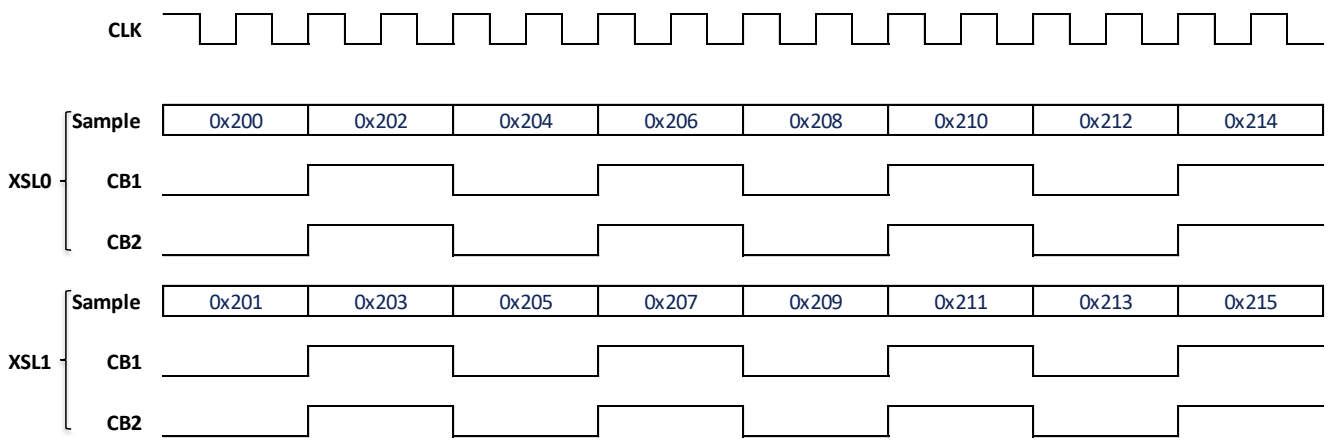


Figure 24 – Chronogram of the Ramp test mode

6.12.3 DC balance

There are two main issues in serial transmission. First, the transmission must be DC balanced to avoid voltage imbalance issues while allowing AC coupling between transmitter and receiver. The second issue is brought by the CDR in the receiver. This component uses the edges in the transmission to recover the clock. Thus, if there are long series of '1' or '0', the lock can be lost in the receiver.
To avoid this kind of problem, a DC balance can be added using the 15th bit of the ESIstream protocol: if bit[15] is set to 1; the bits parity is inverted. Otherwise, nothing is done.

6.13 CRC CHECKING

In order to prevent errors during the OTP (One Time Programmable) life time, a CRC (Cyclic Redundancy Check) is added into the OTP. The CRC reference value is stored in the OTP. During the operation of the ADC, the CRC value of the SPI register can be calculated and compared to the one stored in the OTP, to check if the configuration has been corrupted. A status equal to "1" means that CRC is OK. A status equal to "0" means the CRC is not OK.

Table 31. OTP and CRC registers description

Register Name	@	Type	Size	Default Value	Core	Comment
OTP_LOADING	@0x0001	W	1	NA	All	bit[0] = to load fuses (OTP) values into the SPI register. 0 or 1 : load OTP value into SPI This is a write only register
A_CALC_OTP_CRC	@0x0B0B	R	16	N/A	A	CRC calculated after a OTP loading
B_CALC_OTP_CRC	@0x0B0C	R	16	N/A	B	CRC calculated after a OTP loading
C_CALC_OTP_CRC	@0x0B0E	R	16	N/A	C	CRC calculated after a OTP loading
D_CALC_OTP_CRC	@0x0B0F	R	16	N/A	D	CRC calculated after a OTP loading
E_CALC_OTP_CRC	@0x0B29	R	16	N/A	A & B	CRC calculated after a OTP loading
F_CALC_OTP_CRC	@0x0B2A	R	16	N/A	C & D	CRC calculated after a OTP loading

Register Name	@	Type	Size	Default Value	Core	Comment
A_OTP_CRC	@0x0B14	R	16	N/A	A	CRC OTP reading
B_OTP_CRC	@0x0B15	R	16	N/A	B	CRC OTP reading
C_OTP_CRC	@0x0B17	R	16	N/A	C	CRC OTP reading
D_OTP_CRC	@0x0B18	R	16	N/A	D	CRC OTP reading
E_OTP_CRC	@0x0B2B	R	16	N/A	A & B	CRC OTP reading
F_OTP_CRC	@0x0B2C	R	16	N/A	C & D	CRC OTP reading

6.14 CHIP ID

Chip_ID can be read though dedicated register CHIP_ID described below:

Table 32. CHIP_ID register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHIP_ID															

Register Name	@	Type	Size	Default Value	Core	Comment
CHIP_ID	0x0011	R	16	0x914	-	Chip id value is 0x914

6.15 Single event protection

All sensitive areas of the device have been protected to increase robustness. This includes but is not limited to clock circuitry and SPI registers. To improve even more the robustness, an extra protection mode has been implemented. It can be activated through the EXTRA_SEE_PROTECT register.

Table 33. EXTRA_SEE_PROTECT register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															EXTRA_SEE_PROTECT

Register Name	@	Type	Size	Default Value	Core	Comment
EXTRA_SEE_PROTECT	0x0002	RW	1	0b0	All	Additional protection against Single Event 0: major protection is available (default) 1: additional protection is available _ All SPI registers can't be accessed, except this register _ SYNC is disabled _ The presence of the CLOCK SPI refreshes Triple Majority Redundancy registers

Enabling register EXTRA_SEE_PROTECT by writing '1' disables the SYNCTRIG input when in SYNC mode and thus prevents unwanted timing reset of the ADC (see section 6.5 for more information). It prevents as well any modification on the SPI registers. The SPI clock (SCLK) can be provided from time to time to refresh the SPI (and flush out any SE that would have impacted one branch of the TMR). When it is necessary to modify the configuration of the device or synchronize the ADC, this register needs to be set back to '0'.
The consequences of extra SEE protection activation are described in Table 34.

Table 34. Consequences of extra SEE protection activation

	PROTECTION OFF	PROTECTION ON
SYNC mode	SYNC possible	SYNC deactivated
Trigger mode	No SYNC possible, Trigger mode operating	
Registers	Registers can be modified by OTP or SPI	Registers cannot be modified

6.16 SDA operation

The effective sampling instant of each ADC core can be adjusted independently via registers x_SDA_CTRL (with x=A, B, C or D) thanks to two built in fine and coarse internal clock shifters (fine: 1023 steps of 30fs, coarse: addition of 0, 1, 2 or 3 delay of 30ps).
The total tuning range is 120ps. Delay is set only through SPI instructions. By default, SDA is disabled (by-passed). Activating the SDA has an impact on the jitter performance of the device.

Table 35. A_SDA_CTRL, B_SDA_CTRL, C_SDA_CTRL and D_SDA_CTRL registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			SDA disable	SDA value											

Register Name	@	Type	Size	Default Value	Core	Comment
A_SDA_CTRL	0x012F	W	13	0x1000	A	A core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)
B_SDA_CTRL	0x032F	W	13	0x1000	B	B core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)
C_SDA_CTRL	0x052F	W	13	0x1000	C	C core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit[9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)
D_SDA_CTRL	0x072F	W	13	0x1000	D	D core Sampling Delay Adjust (0 to 120 ps with a step of 30 fs) bit[11:0] = SDA value bit [9:0]: fine delay, step 30fs bit[11:10]: coarse delay, step 30ps bit[12] = SDA disable 0: enable 1: disable (default)

7 DIE JUNCTION TEMPERATURE MONITORING DIODE

Two pins are provided so that the diode can be probed using standard temperature sensors. Maximum current allowed on this pin is 1.2 mA.
The diode measures the junction temperature which is 7.5°C below the hot spot (but higher than die average temperature)

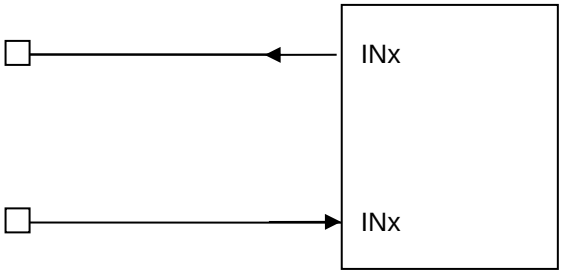


Figure 25 – Junction temperature monitoring diode system

Note: If the diode function is not used, the diode pins can be left unconnected (open). If diode is used it is mandatory to connect DiodeC to GND.

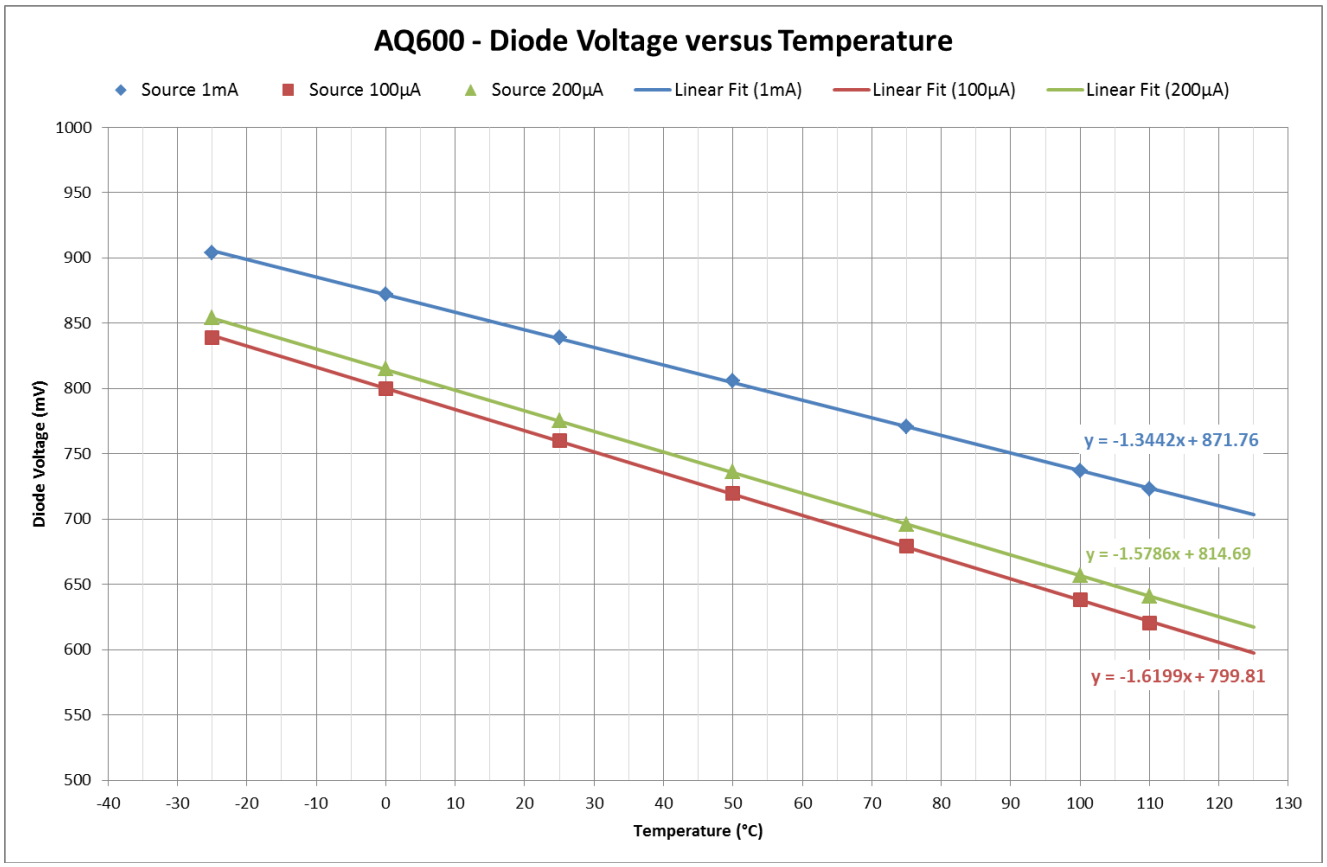


Figure 26: Diode voltage vs temperature for 3 different input currents (blue: 1mA, green: 200µA, red: 100µA)

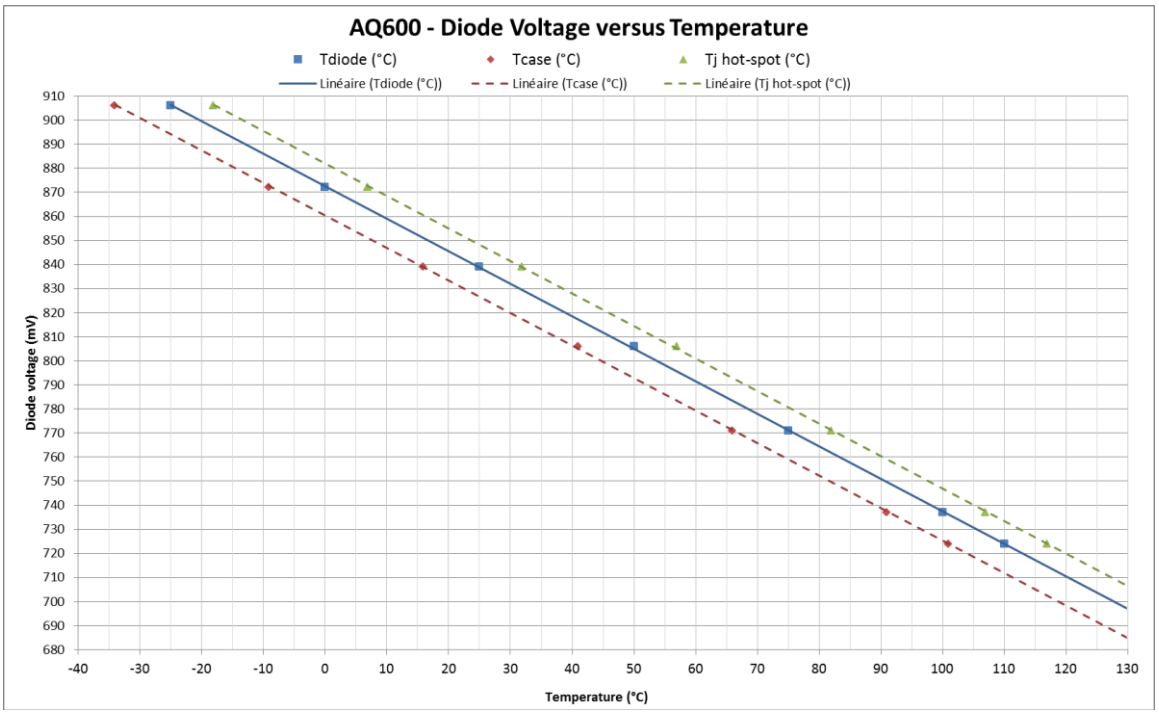


Figure 27: Voltage vs temperature. Blue=diode voltage - Green=hot-spot junction voltage- Red=case voltage.

8 FUNCTIONALITIES SUMMARY

Default mode is:

- ADC core calibrated through OTP values
- Serial buffer in reduced swing (low power) mode
- Extended analog bandwidth selected
- Synchronization mode enabled
- In range signal output
- 4 ADC Cores are interleaved.

Table 36. Functionalities summary

Functionality / mode	Default mode	description	control
Serial 8 lanes	ON	Available - data rate @2x Fclock (Max 12Gb/s)	SPI
Serial 4 lanes	OFF	Available data rate @2x Fclock (Max 12Gb/s)	SPI
Swing adjust	ON	ON (reduced swing) / OFF	SPI
Input common mode Adjust	Set by OTP	Available	OTP/SPI
Input impedance Adjust	Set by OTP	Available	OTP/SPI
CML impedance Adjust	Set by OTP	Available	OTP/SPI
Gain Adjust	Set by OTP	Available	OTP/SPI
Offset Adjust	Set by OTP	Available	OTP/SPI
Phase adjust	Set by OTP	Available	OTP/SPI
SDA	Disabled	Available	OTP/SPI
Power ON Mode	no standby	Available	SPI
InRange	output	Available	Selected by SPI
SYNC mode /Trigger Mode	SYNC MODE enable	SYNC MODE enable SYNC mode disable,trigger mode enable	Selected by SPI
Test Mode	Disabled	Enable / Disabled	Selected by SPI
Analog bandwidth	extended	Nominal or extended	Selected by SPI
SEE protection	OFF	OFF or ON	Selected by SPI
Junction temperature monitoring		Available	Refer to section 7

8.1 Calibrations summary

For details regarding calibration, see section 9.3.

Table 37. Calibrations summary

Calibration	Description	Set by OTP	Set by SPI
Core gain adjust	ADC gain adjust for interleaving operation	Yes	Yes
Core offset adjust	ADC DC offset adjust for interleaving operation	Yes	Yes
Core phase adjust	ADC sampling phase adjust for interleaving operation	Yes	Yes
Core input impedance	100 ohm differential impedance calibration	Yes	Yes
CML output impedance	100 ohm differential impedance calibration	Yes	Yes
CMiref	Input common mode calibration	Yes	Yes

8.1.1 Input common mode calibration

ADC analog input can operates in DC coupling or AC coupling mode. To cope with previous amplifier output stage, ADC input common mode (CMIREF) can be trimmed via IN0_IN1_CMIREF and IN2_IN3_CMIREF registers described below.
Adjustment of input common mode can also be used to optimize ADC linearity.

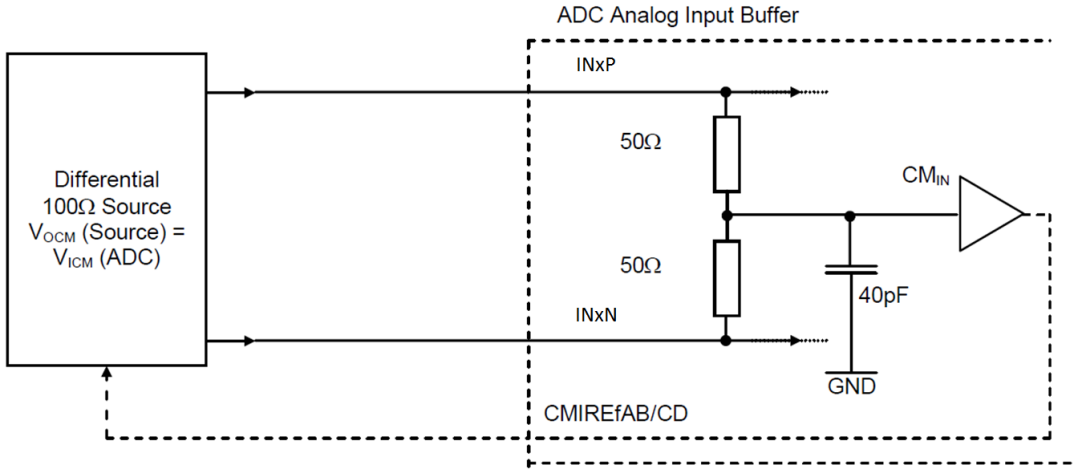


Figure 28 : Differential analog input implementation (DC coupled)

Table 38. IN0_IN1_CMIREF and IN2_IN3_CMIREF registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											IN0_IN1_CMIREF IN2_IN3_CMIREF				

Register Name	@	Type	Size	Default Value	Core	Comment
IN0_IN1_CMIREF	0x0905	R/W	5	0x14	A, B	Input common mode calibration for A & B cores
IN2_IN3_CMIREF	0x0906	R/W	5	0x14	C, D	Input common mode calibration for C &D cores

IN0_IN1_CMIREF IN2_IN3_CMIREF (hexa)	CMIREF (V)
1F	1.525
10	1.6
0	1.675
Excursion	0.15
Step	5.10^{-3}

8.1.2 Input impedance calibration

ADC impedance matching is important to maximize power transmission. DC impedance can be trimmed digitally to 100 (Ω) with IN0_IN1_RIN and IN2_IN3_RIN registers to compensate process variation or optimized power transmission, with 2% accuracy.

Table 39. IN0_IN1_RIN and IN2_IN3_RIN registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											IN0_IN1_RIN IN2_IN3_RIN				

Register Name	@	Type	Size	Default Value	Core	Comment
IN0_IN1_RIN	0x0907	R/W	5	0x10	A, B	
IN2_IN3_RIN	0x0908	R/W	5	0x10	C, D	

IN0_IN1_RIN IN2_IN3_RIN (hexa)	Rin (Ω)
0	142
10	90
1F	87
Excursion	55
Step	1.7

8.2 CML output impedance calibration

ADC impedance matching is important to maximize power transmission. DC impedance of CML output buffers can be trimmed digitally to 100 (Ω) with AB_ROUT_HSSL (or CD_ROUT_HSSL) register on both cores A and B (C and D respectively) to compensate process variation or to optimize power transmission, with 5% accuracy.
Note: CLKOUT CML output buffers impedance cannot be trimmed.

Table 40. AB_ROUT_HSSL and CD_ROUT_HSSL registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								AB_ROUT_HSSL CD_ROUT_HSSL							

Register Name	@	Type	Size	Default Value	Core	Comment
AB_ROUT_HSSL	0x909	R/W	8	0x55	A, B	CALIBRATION R LOAD CML bit[1:0]= R_cml0 channel A (for link0) bit[3:2]= R_cml1 channel A (for link1) bit[5:4]= R_cml0 channel B (for link0) bit[7:6]= R_cml1 channel B (for link1)
CD_ROUT_HSSL	0x90A	R/W	8	0x55	C, D	CALIBRATION R LOAD CML bit[1:0]= R_cml0 channel C (for link0) bit[3:2]= R_cml1 channel C (for link1) bit[5:4]= R_cml0 channel D (for link0) bit[7:6]= R_cml1 channel D (for link1)

AB_ROUT_HSSL CD_ROUT_HSSL (hexa)	ROUT (Ω)
0	83
1	100
3	125
Excursion	42
Step	14

8.3 Interleaving functions

To improve interleaving performances, gain, phase and offset of each ADC core can be corrected thanks to embedded DACs accessible via registers described in the following paragraphs. 4 factory calibration sets are available to improve performance depending on the condition of use.

Calibration set	Region of interest	Frequency of calibration	Calibration temperature (Td)
CalSet0	800MHz to 6GHz	2230MHz	60°C
CalSet1	800MHz to 6GHz	2230MHz	100°C
CalSet2	DC to 800MHz	100MHz	60°C
CalSet3	DC to 800MHz	100MHz	100°C

8.3.1 Gain Adjustment

The Gain of each ADC core is independently adjustable thanks to a built in 12 bit DACs controlled though the SPI.
Reminder: 4 calibration sets are stored in the product (accessible from the OTP).

Table 41. y_SETx_GAIN_CAL, registers description (x=0, 1, 2, 3 and y= A, B, C, D)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				A_SET0_GAIN_CAL B_SET0_GAIN_CAL C_SET0_GAIN_CAL D_SET0_GAIN_CAL											
				A_SET1_GAIN_CAL B_SET1_GAIN_CAL C_SET1_GAIN_CAL D_SET1_GAIN_CAL											
				A_SET2_GAIN_CAL B_SET2_GAIN_CAL C_SET2_GAIN_CAL D_SET2_GAIN_CAL											
				A_SET3_GAIN_CAL B_SET3_GAIN_CAL C_SET3_GAIN_CAL D_SET3_GAIN_CAL											

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_GAIN_CAL	0x0122	W	12	0x800	A	Interleaving gain calibration Fcal = 2230MHz, Tcal = 60°C
B_SET0_GAIN_CAL	0x0322	W	12	0x800	B	
C_SET0_GAIN_CAL	0x0522	W	12	0x800	C	
D_SET0_GAIN_CAL	0x0722	W	12	0x800	D	
A_SET1_GAIN_CAL	0x0125	W	12	0x800	A	Interleaving gain calibration Fcal = 2230MHz, Tcal =100°C
B_SET1_GAIN_CAL	0x0325	W	12	0x800	B	
C_SET1_GAIN_CAL	0x0525	W	12	0x800	C	
D_SET1_GAIN_CAL	0x0725	W	12	0x800	D	
A_SET2_GAIN_CAL	0x0128	W	12	0x800	A	Interleaving gain calibration Fcal = 100MHz, Tcal =60°C
B_SET2_GAIN_CAL	0x0328	W	12	0x800	B	
C_SET2_GAIN_CAL	0x0528	W	12	0x800	C	
D_SET2_GAIN_CAL	0x0728	W	12	0x800	D	
A_SET3_GAIN_CAL	0x012B	W	12	0x800	A	Interleaving gain calibration Fcal = 100MHz, Tcal =100°C
B_SET3_GAIN_CAL	0x032B	W	12	0x800	B	
C_SET3_GAIN_CAL	0x052B	W	12	0x800	C	
D_SET3_GAIN_CAL	0x072B	W	12	0x800	D	

The tuning range is equivalent to a 427LSB variation of full scale (step of 0.1 LSB).

y_SETx_GAIN_CAL (hexa)	Fullscale variation (LSB)
0	-213,5
800	0
FFF	213,5
Excursion	427
Step	0.1

8.3.2 Phase adjustment

The phase of each ADC core is independently adjustable thanks to a built in 9 bit DACs controlled though the SPI.
Reminder: 4 calibration sets are stored in the product (accessible from the OTP).

Table 42. y_SETx_PHASE_CAL registers description (x=0,1, 2, 3 and y= A, B, C, D)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							A_SET0_PHASE_CAL B_SET0_PHASE_CAL C_SET0_PHASE_CAL D_SET0_PHASE_CAL								
							A_SET1_PHASE_CAL B_SET1_PHASE_CAL C_SET1_PHASE_CAL D_SET1_PHASE_CAL								
							A_SET2_PHASE_CAL B_SET2_PHASE_CAL C_SET2_PHASE_CAL D_SET2_PHASE_CAL								
							A_SET3_PHASE_CAL B_SET3_PHASE_CAL C_SET3_PHASE_CAL D_SET3_PHASE_CAL								

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_PHASE_CAL	0x0123	W	9	0x0100	A	Interleaving phase calibration Fcal = 2230MHz, Tcal = 60°C
B_SET0_PHASE_CAL	0x0323	W	9	0x0100	B	
C_SET0_PHASE_CAL	0x0523	W	9	0x0100	C	
D_SET0_PHASE_CAL	0x0723	W	9	0x0100	D	
A_SET1_PHASE_CAL	0x0126	W	9	0x0100	A	Interleaving phase calibration Fcal = 2230MHz, Tcal = 100°C
B_SET1_PHASE_CAL	0x0326	W	9	0x0100	B	
C_SET1_PHASE_CAL	0x0526	W	9	0x0100	C	
D_SET1_PHASE_CAL	0x0726	W	9	0x0100	D	
A_SET2_PHASE_CAL	0x0129	W	9	0x0100	A	Interleaving phase calibration Fcal = 100MHz, Tcal = 60°C
B_SET2_PHASE_CAL	0x0329	W	9	0x0100	B	
C_SET2_PHASE_CAL	0x0529	W	9	0x0100	C	
D_SET2_PHASE_CAL	0x0729	W	9	0x0100	D	
A_SET3_PHASE_CAL	0x012C	W	9	0x0100	A	Interleaving phase calibration Fcal = 100MHz, Tcal = 100°C
B_SET3_PHASE_CAL	0x032C	W	9	0x0100	B	
C_SET3_PHASE_CAL	0x052C	W	9	0x0100	C	
D_SET3_PHASE_CAL	0x072C	W	9	0x0100	D	

The tuning range is equivalent to ± 0.9ps (step of 3.5 fs).
For wider range, SDA operation described hereafter could also be used.

y_SETx_PHASE_CAL (hexa)	phase variation (fs)
0	-900
100	0
1FF	900
Excursion	1800
Step	3.5

8.3.3 Offset adjustment

The Offset of each ADC core is independently adjustable thanks to a built in 9 bit DACs controlled though the SPI.
Reminder: 4 calibration sets are stored in the product (accessible from the OTP)

Table 43. y_SETx_OFFSET_CAL registers description (x=0,1, 2, 3 and y= A, B, C, D)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							A_SET0_OFFSET_CAL B_SET0_OFFSET_CAL C_SET0_OFFSET_CAL D_SET0_OFFSET_CAL								
							A_SET1_OFFSET_CAL B_SET1_OFFSET_CAL C_SET1_OFFSET_CAL D_SET1_OFFSET_CAL								
							A_SET2_OFFSET_CAL B_SET2_OFFSET_CAL C_SET2_OFFSET_CAL D_SET2_OFFSET_CAL								
							A_SET3_OFFSET_CAL B_SET3_OFFSET_CAL C_SET3_OFFSET_CAL D_SET3_OFFSET_CAL								

Register Name	@	Type	Size	Default Value	Core	Comment
A_SET0_OFFSET_CAL	0x0124	W	9	0x0100	A	Interleaving offset calibration Fcal = 2230MHz, Tcal = 60°C
B_SET0_OFFSET_CAL	0x0324	W	9	0x0100	B	
C_SET0_OFFSET_CAL	0x0524	W	9	0x0100	C	
D_SET0_OFFSET_CAL	0x0724	W	9	0x0100	D	
A_SET1_OFFSET_CAL	0x0127	W	9	0x0100	A	Interleaving offset calibration Fcal = 2230MHz, Tcal = 100°C
B_SET1_OFFSET_CAL	0x0327	W	9	0x0100	B	
C_SET1_OFFSET_CAL	0x0527	W	9	0x0100	C	
D_SET1_OFFSET_CAL	0x0727	W	9	0x0100	D	
A_SET2_OFFSET_CAL	0x012A	W	9	0x0100	A	Interleaving offset calibration Fcal =100MHz, Tcal = 60°C
B_SET2_OFFSET_CAL	0x032A	W	9	0x0100	B	
C_SET2_OFFSET_CAL	0x052A	W	9	0x0100	C	
D_SET2_OFFSET_CAL	0x072A	W	9	0x0100	D	
A_SET3_OFFSET_CAL	0x012D	W	9	0x0100	A	Interleaving offset calibration Fcal = 100MHz, Tcal = 100°C
B_SET3_OFFSET_CAL	0x032D	W	9	0x0100	B	
C_SET3_OFFSET_CAL	0x052D	W	9	0x0100	C	
D_SET3_OFFSET_CAL	0x072D	W	9	0x0100	D	

The tuning range is equivalent to +/- 27.4 LSB (step of 0.11 LSB)

y_SETx_OFFSET_CAL (hexa)	offset variation (LSB)
0	-27.4
100	0
1FF	27.4
Excursion	55
Step	0.11

8.3.4 Interpolation with temperature

To further enhance performance and compensate the roll-off effect with temperature, the user can interpolate the Gain, Phase and Offset registers according to the 2 temperature given calibration sets (CalSet0/CalSet1 or CalSet2/CalSet3). A simple linear interpolation will lead to new registers values that will improve performance.
The following equation applies:

$$Reg\ value(T) = \frac{Reg\ value(100°C) - Reg\ value(60°C)}{100°C - 60°C} \times T + Reg\ value\ (60°C) - \frac{Reg\ value(100°C) - Reg\ value(60°C)}{100°C - 60°C} \times 60°C$$

The original register values (@60°C and @100°C respectively) are to be read in the appropriate SPI addresses (see Table 41 to Table 43). Once the derived register value is found, the user shall write it (through SPI) in place of the previous calibration set used.
Example: the user is working at 3GHz with CalSet1 (Fcal=2230MHz, Tcal=100°C) loaded into SPI, the current device temperature drops to 40°C and the system can adjust the registers to match this new temperature.

Table 44. Example of Interleaving registers interpolation

Register type	ADC Core	Value @60°C	Value @100°C	Interpolated value @40°C	Target address (SPI)
Gain	A	76D	774	76A	0x0125
	B	714	719	712	0x0325
	C	88B	886	88E	0x0525
	D	8E3	8DE	8E6	0x0725
Phase	A	0E5	0F3	DE	0x0126
	B	12D	125	131	0x0326
	C	0DE	0E3	DC	0x0526
	D	0E4	0ED	E0	0x0726
Offset	A	0DE	0E3	DC	0x0127
	B	124	121	126	0x0327
	C	120	11B	123	0x0527
	D	125	11E	129	0x0727

8.4 POWER ON mode

All internal blocks can be powered ON or OFF : CPS, anacore circuitry, digital circuitry, TH circuitry, latch circuitry, High Speed serial links (HSSL) and CML buffers (HSSL_IO).
Figure 29 details the layout of these different internal blocks and their respective power_on registers.

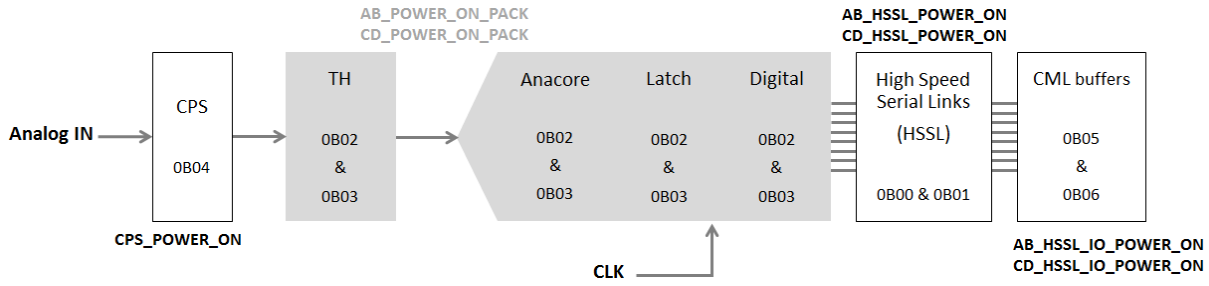


Figure 29 : Internal blocks that can be powered ON or OFF and their respective register addresses.

Power-on mode for TH, anacore, latch and digital circuitry can be controlled via AB_POWER_ON_PACK and CD_POWER_ON_PACK registers, described in Table 45.
CML buffers, HSSL and CPS blocks own dedicated registers described in Table 46 to Table 48.

Table 45. AB_POWER_ON_PACK and CD_POWER_ON_PACK registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								AB_POWER_ON_PACK CD_POWER_ON_PACK							

Register Name	@	Type	Size	Default Value	Core	Comment
AB_POWER_ON_PACK	0x0B02	RW	8	0b1111111	A, B	bit[0] = power_on Latch A bit[1] = power_on Latch B bit[2] = power_on Digital A bit[3] = power_on Digital B bit[4] = power_on Anacore A bit[5] = power_on Anacore B bit[6] = power_on TH A bit[7] = power_on TH B 0 : power OFF 1 : power ON
CD_POWER_ON_PACK	0x0B03	RW	8	0b1111111	C, D	bit[0] = power_on Latch C bit[1] = power_on Latch D bit[2] = power_on Digital C bit[3] = power_on Digital D bit[4] = power_on Anacore C bit[5] = power_on Anacore D bit[6] = power_on TH C bit[7] = power_on TH D 0 : power OFF 1 : power ON

Other blocks such as HSSL, CPS and HSSL_IO are adressed through dedicated SPI registers as described below.

Table 46. AB_HSSL_POWER_ON and CD_HSSL_POWER_ON registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
														AB_HSSL_POWER_ON CD_HSSL_POWER_ON	

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_POWER_ON	0x0B00	RW	2	0b11	A, B	bit[0] = power_on CHANNEL A serial link bit[1] = power_on CHANNEL B serial link 0 : power OFF 1 : power ON
CD_HSSL_POWER_ON	0x0B01	RW	2	0b11	C, D	bit[0] = power_on CHANNEL C serial link bit[1] = power_on CHANNEL D serial link 0 : power OFF 1 : power ON

Table 47. CPS_ POWER_ON register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															CPS_POWER_ON

Register Name	@	Type	Size	Default Value	Core	Comment
CPS_ POWER_ON	0x0B04	RW	1	0b1	-	bit[0] = power_on CPS 0 : power OFF 1 : power ON

Table 48. AB_HSSL_IO_POWER_ON and CD_HSSL_IO_POWER_ON registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
												AB_HSSL_IO_POWER_ON CD_HSSL_IO_POWER_ON			

Register Name	@	Type	Size	Default Value	Core	Comment
AB_HSSL_IO_POWER_ON	0x0B05	RW	4	0b1111	A, B	CMLx : Serial link x buffer bit[0] = power_on CML1 channel A bit[1] = power_on CML2 channel A bit[2] = power_on CML1 channel B bit[3] = power_on CML2 channel B 0 : power OFF 1 : power ON
CD_HSSL_IO_POWER_ON	0x0B06	RW	4	0b1111	C, D	CMLx : Serial link x buffer bit[0] = power_on CML1 channel C bit[1] = power_on CML2 channel C bit[2] = power_on CML1 channel D bit[3] = power_on CML2 channel D 0 : power OFF 1 : power ON

In order to switch a core in its stand-by mode : latch, digital, anacore and TH circuitry, HSSL and CML buffers of the considered core are required to be powered-OFF.
A SYNC will be sufficient to apply the modifications done in the registers concerning blocks of the power-on mode.
To switch back a core in its power-on mode: all these registers are required to be powered-ON. A SYNC, and eventually a FPGA-RESET, has to follow the registers' switches.

9 APPLICATION INFORMATION

9.1 Power supplies

9.1.1 Power supply ramp-up

Supplies settling time should be faster than 10ms. No specific power sequencing is required. However, in order to avoid possible current peak at start up, it is recommended to use the following sequence: Vccd/Vcco/Vcca (Vcc_spi can be powered up at any time).

9.1.2 Bypassing, decoupling and grounding

Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 22 nF capacitors (value depending of DC/DC regulators).

All grounds pins have to be connected on PCB but locally under the component, a slit between AGND+DGND (analog and digital ground) and GNDO (IO ground) has to be respected.

The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins as described in Figure 30 and Table 49.

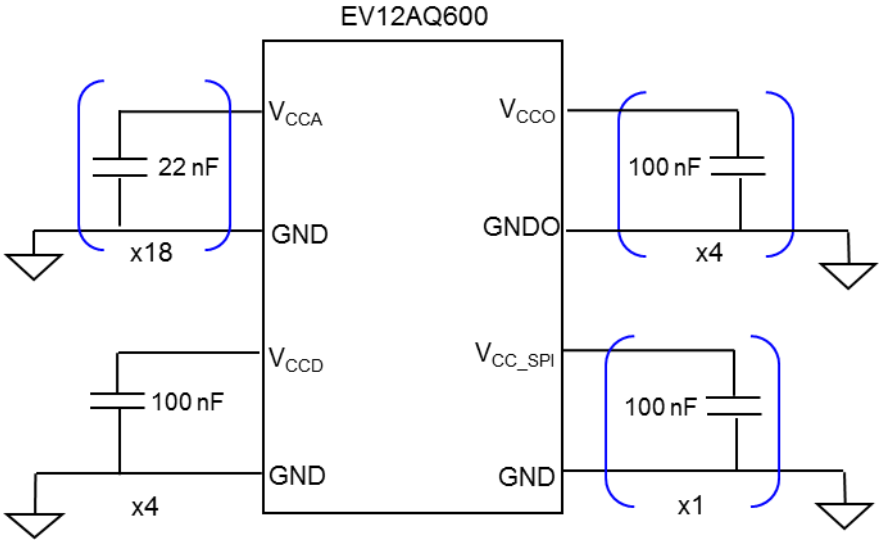


Figure 30 - Power Supplies decoupling scheme

Table 49. List of recommended neighboring pins for V_{CCA} decoupling

(VCCA, AGND)
Pins (E9-D9) (E10-D10) (G9-F9) (G10-F10) (G11-F11) (G8-F8) (J8-H8) (J11-H11) (H9-J9) (H10-J10) Pins (K8-K7) (K11-K12) (K9-L9) (K10-L10) (L8-M8) (L11-M11) (M9-N9) (M10-N10)

Table 50. List of recommended neighboring pins for V_{CCD} decoupling

(VCCD, DGND)
Pins (G6-G7) (H6-J6) (K6-L6) (M6-N6) Pins (G13-G12) (H13-J13) (K13-L13) (M13-N13) (F14-F13)

Table 51. List of recommended neighboring pins for V_{CCO} decoupling

VCCO- GNDO
Pins (H4-J4) (M4-L4) (K4-K3) (H5-J5) (M5-L5) Pins (H14-J14) (M14-L14) (K15-K16) (H15-J15) (M15-L15)

Table 52. List of recommended neighboring pins for V_{CC_SPI} decoupling

VCC_SPI- DGND

Pins (F5-F6)

9.2 High Speed Serial Interface

More information on the ESIstream protocol can be found on www.esistream.com.

The ESIstream protocol is a 14b/16b encoding based on 14 scrambled bits along with 2 overhead bits: clock bit and disparity bit. Applied onto the EV12AQ600, the 16 bits frames are as follows:

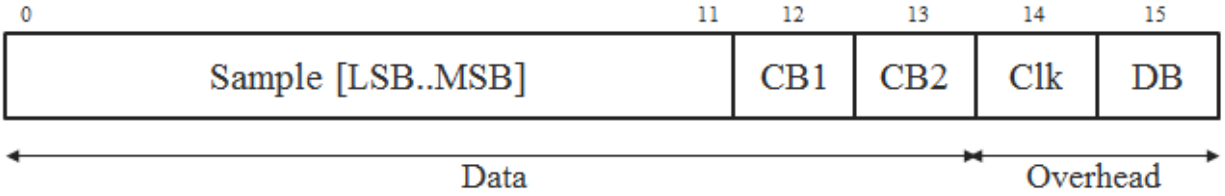


Figure 31 - ESIstream frame with EV12AQ600

DB being the disparity bit, CLK the clock bit, CB1 and CB2 the control bit of the ADC (Refer to Table 28) and bit 11 to 0 contains the ADC sample. Bit 13 to 0 are scrambled using an LSFR (Linear Feedback Shift Register) that generate the PRBS (Pseudo-Random Binary Sequence). The frames are transmitted LSB first.

9.2.1 ESIstream protocol

9.2.1.1 Scrambling

Applying scrambling ensures a statistical DC balanced transmission. It also statistically ensures that there are transitions in the transmission. It is necessary to comply with these constraints otherwise the CDR (Clock and Data Recovery) may lose its lock and the data would be corrupted.

The scrambling technique used in ESIstream is an additive scrambling to avoid error propagation in case of a single bit error. It is based on Fibonacci architecture using the following polynomial: $X^{17}+X^3+1$. It has a run length of $2^{17}-1$. Instead of using a shift of one bit per operation, it uses shifts of 14 bits per operation to adapt to the size of the data being scrambled.
The equations to use to generate this PRBS are as follow:

$$LFSR_{n+1}(0) = LFSR_n(14)$$
$$LFSR_{n+1}(1) = LFSR_n(15)$$
$$LFSR_{n+1}(2) = LFSR_n(16)$$
$$LFSR_{n+1}(3) = LFSR_n(0) \text{ xor } LFSR_n(3)$$
$$LFSR_{n+1}(4) = LFSR_n(1) \text{ xor } LFSR_n(4)$$
$$LFSR_{n+1}(5) = LFSR_n(2) \text{ xor } LFSR_n(5)$$
$$LFSR_{n+1}(6) = LFSR_n(3) \text{ xor } LFSR_n(6)$$
$$LFSR_{n+1}(7) = LFSR_n(4) \text{ xor } LFSR_n(7)$$
$$LFSR_{n+1}(8) = LFSR_n(5) \text{ xor } LFSR_n(8)$$
$$LFSR_{n+1}(9) = LFSR_n(6) \text{ xor } LFSR_n(9)$$
$$LFSR_{n+1}(10) = LFSR_n(7) \text{ xor } LFSR_n(10)$$
$$LFSR_{n+1}(11) = LFSR_n(8) \text{ xor } LFSR_n(11)$$
$$LFSR_{n+1}(12) = LFSR_n(9) \text{ xor } LFSR_n(12)$$
$$LFSR_{n+1}(13) = LFSR_n(10) \text{ xor } LFSR_n(13)$$
$$LFSR_{n+1}(14) = LFSR_n(11) \text{ xor } LFSR_n(14)$$
$$LFSR_{n+1}(15) = LFSR_n(12) \text{ xor } LFSR_n(15)$$
$$LFSR_{n+1}(16) = LFSR_n(13) \text{ xor } LFSR_n(16)$$

The PRBS is applied to the data as follow; the 14 LSB of the PRBS are the bits used to scramble the data.

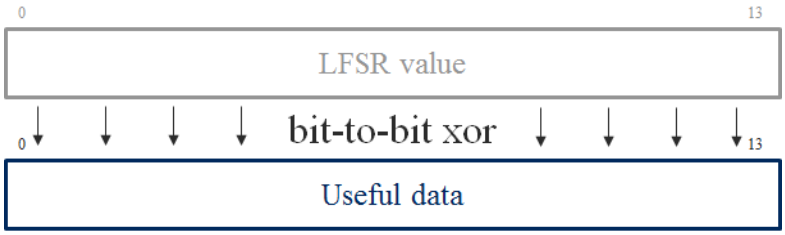


Figure 32 - LFSR operation

This particular LFSR was chosen because it reduces the number of necessary gates to be implemented.

9.2.1.2 Encoding

After scrambling, the 14 bits of data are encoded into a 16 bits frame. One of the added bits is the clk bit; it toggles at every frame. The last bit encoding these 15 bits is the disparity bit. Its objective is to ensure deterministically the advantages brought statistically by the scrambling process.

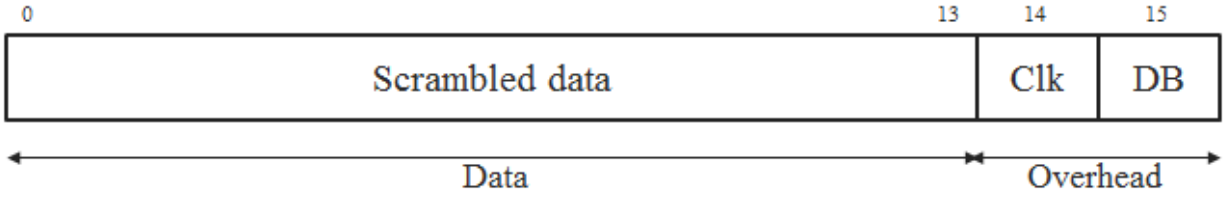


Figure 33 - Frame format after encoding

Even with scrambling, large running disparity can still occur with very low probability and could produce excessive eye shifts. These eye shifts could be balanced by a more complicated equalization stage in the receiver if the running disparity was still limited. However, a PRBS does not bind the running disparity deterministically, thus the data could be corrupted on the reception end and it could eventually cause the CDR to lose its lock. To prevent this, the disparity bit is implemented.

The running disparity of the transmission is constantly monitored by the transmitter on each link.
For each frame, its disparity is calculated, 2 cases can occur on the running disparity:

a. The running disparity of the transmission **does not** increase above +/- 15 (+15 and -15 included). In this case, the disparity bit is set to '0' and the 15 bits of data (scrambled data + clk bit) are transmitted as such.
b. The running disparity of the transmission **does** increase above +/-15 (+15 and -15 excluded). In this case, the 15 bits of data (scrambled data + clk bit) are inverted and the disparity bit is set to '1'.

The running disparity is updated with the disparity of the frame.

This disparity bit ensures that the longest possible series of '1' or '0' transmitted is of 48 bits (the clk bit reduces this value effectively to 32). It also ensures that the running disparity does not exceed +/- 15 (included) which satisfies the DC balance condition.

In normal operating mode, the receiver will check the disparity bit first. If it is high then it will invert the received data and descramble them. Otherwise it will directly descramble them.

9.2.1.3 Synchronization

The link must be synchronized to align the frames between the transmitter and the receiver and to synchronize the reception scrambler with the transmission scrambler. The synchronization is controlled through the SYNC signal sent by the receiver (FPGA/ASIC) to the transmitter (EV12AQ600).

The synchronization works in 2 steps and starts when the ADC receives a SYNCTRIG pulse in SYNC mode (refer to section 6.5).

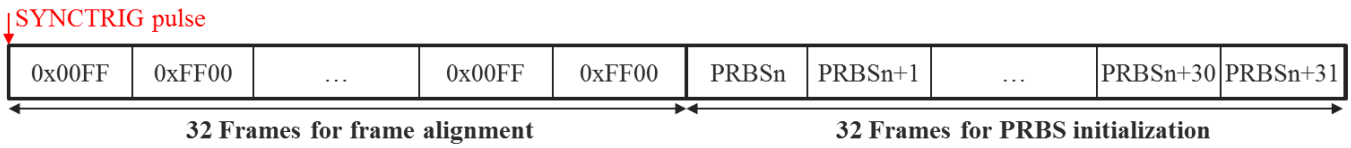


Figure 34 - Synchronization sequence

When the ADC sees the SYNCTRIG pulse, it will send an alignment pattern which is 32 frames alternating between 0xFF00 and 0x00FF. The sequence bypasses the scrambling and disparity processing (the sequence is DC balanced). This alignment pattern should be used by the receiver to align its data on the transmitter output data.
After these 32 frames, the transmitter starts sending 32 additional frames containing the scrambling PRBS alone. These frames contain 14 bits of the PRBS plus the clk bit and the disparity bit. They go through the disparity processing, as the PRBS value will start to impact the running disparity of the transmission.

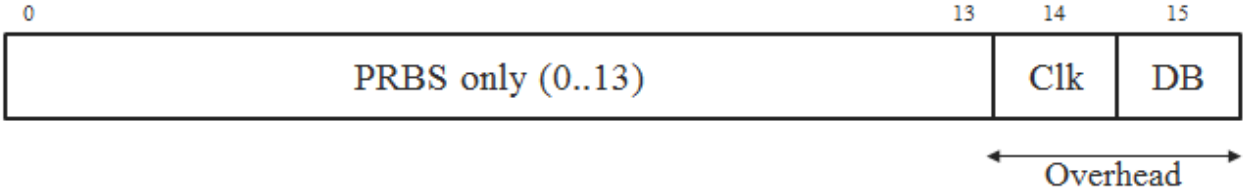


Figure 35 - Frame sent for PRBS initialization

The receiver will detect the transition from the alignment pattern to the PRBS alone (passive detection). It will determine the initial value it has to start its PRBS with after receiving 2 frames of the PRBS. These 2 frames contain 28 bits of the PRBS sequence; the receiver needs 17 bits to determine its initial value. The transmitter (EV12AQ600) PRBS sequence is reset upon reception of a SYNCTRIG pulse in SYNC mode.

The PRBS used is based on the polynomial sequence $X^7 + X^6 + 1$.

After these 2 steps, the synchronization of the link is complete.

During normal operation, the synchronization of the serial links can be monitored through the clk bit. If the receiver does not detect that the clk bit is toggling properly, then it can state that the link is not synchronous or has lost its synchronization and restart the synchronization process. Another option is to use the timestamp control bit of the ADC to monitor the interface synchronization.

9.3 Interleaving Calibration protocol

To reduce interleaving spurs level, phase, offset and gain of each core, SPI can be adjusted.
Refer to Table 41 to Table 43.

9.3.1 Offset interleaving calibration

To set offset, DC value should be extracted with high precision to quantify offset unbalance between cores. Offset adjust 9 bits DAC should be set at the right value to decrease DC offset mismatch.

Protocol:
- Use single core output data with or without input signal
- Calculate output data average for each core DCcoreX (X= A, B, C, D)
- Apply DC correction equal to:

$$DC_{correction}X = \frac{DC_{core}X - DC_{ref}}{DAC\_LSB_{DCcorex}}$$

With:
- $DC_{correction}X$ = DAC code to compensate corex DC offset (X = A, B, C, D)
- $DC_{core}X$ = DC offset at coreX output (X = A, B, C, D)
- DC_{ref}= reference value to align cores DC offset. It can be set to 2048 or to one core offset value
- $DAC\_LSB_{DCcorex}$= core X DC offset DAC calibration LSB (X = A, B, C, D)

CoreX DC offset DAC calibration LSB is determined by measuring corex DC offset at maximum and minimum correction.

$$LSB_{DCcorex} = \frac{DC_{core}X@maxcode - DC_{core}X@mincode}{maxcode - mincode - 1}$$

With:
- $DC_{core}X@maxcode$ = core X DC offset at maximum DC offset correction code
- $DC_{core}X@mincode$ = core X DC offset at minimum DC offset correction code
- $maxcode = 511$
- $mincode = 0$

9.3.2 Gain and phase interleaving calibration

By using FFT on each core output, gain and phase of each core can be estimated at input frequency Fin of interest. Correction is calculated as follow:

$$Gain_{correction}X = \frac{Gain_X - Gain_{ref}}{LSB_{Gain\ X}}$$

$$Phase_{correction}X = \frac{Phase_X - Phase_{ref}}{LSB_{Phase\ X} * (360.F_{in})}$$

With:

$Core\ X$Corex: core to be calibrated (X = A, B, C, D)
$Gain_X$Gainx: corex gain in dB
$Gain_{ref}$Gainref: core gain reference in dB
$Phase_X$Phasex: corex phase in degree
$Phase_{ref}$Phaseref: core phase reference in degree
F_{in}Fin: frequency of interest

Gain and phase measurement accuracy should be negligible regarding ADC LSB.

10 ORDERING INFORMATIONS

Table 53. Prototypes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EVP12AQ600SH	Ambient	Prototype	RoHS	Beta sampling
EVX12AQ600AGH	Ambient	Prototype	Non RoHS	General samples
EVX12AQ600ASH	Ambient	Prototype	RoHS	General samples

Table 54. Evaluation kit

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600-ADX4-EVM	Ambient	Prototype		

Table 55. Ordering codes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600ACSH	Tc 0°C, Tj +90°C	Standard	RoHS	Pending qualification
EV12AQ600AVSH	Tc -40°C, Tj +110°C	Standard	RoHS	Pending qualification
EV12AQ600AMSH	Tc -55°C, Tj +125°C	Standard	RoHS	Pending qualification
EV12AQ600AMGH	Tc -55°C, Tj +125°C	Standard	Non RoHS	Pending qualification

Table 56. Engineering, Engineering Qualification and Flight Models ordering codes

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EV12AQ600AMGHD/T	Tc -55°C, Tj +125°C	Standard +168h burn-in	Non RoHS	Pending qualification
EV12AQ600AMGH-Y	Tc -55°C, Tj +125°C	QML-Y compliant	Non RoHS	Pending qualification
EV12AQ600AMGH9NB1	Tc -55°C, Tj +125°C	ESCC9000 compliant	Non RoHS	Pending qualification

11 REVISION HISTORY

Issue	Date	Comments
A	22/03/2018	Creation
B	27/04/2018	Main page: bring some clarification on performance in the different Nyquist zones Figure 1 modified for clarification Table 3: clock output level is referenced to V_{CCA} and not V_{CCO} Table 12: CLKOUT is an output and not an input
C	12/11/2018	All document : FClock Max = 6.4 GHz §1 New CPS scheme with serial link ESIstream up to 12.8 Gsps §1 Functionalities though SPI updated §1 and §6.4.1: step for Gain adjustment is 0.1 LSB. §6.2.2 : maximum input impedance is 1F and not 3F §2.1 Absolute Maximum ratings table update §2.5 Low frequency an dynamic characteristics table update §3.1 Package outline for SAC305 added §3.3 Relative skew for serial links view §5.3, §7.3.1, §7.3.2, §7.3.3 Calibration set2 and set3 added §5.8 Calibration selection description §5.11.3 Decimation section added §7.3 Interleaving functions §7.4 Power ON mode section added §9 P/Ns added §2.6 Switching characteristics table updated External Clock low frequency range 800 MHz up to 2000 MHz External Clock high frequency range 4500 MHz up to 6400 MGHz
D	08/03/2019	Min and Max values added in performance tables FClock @ 6.4 GHz added in performance tables SFDR, THD, SNR, SINAD & ENOB nominal values Power on chapter modified §3.5 VccA range modified and table 4 values accordingly §4.3 Relative skew for serial links view modified