e2v
Avenue de Rochepleine, BP 123, 38521 Saint Egrève Cedex, France

Tel. +33 (0)4 76 58 30 00 - Fax +33 (0)4 76 58 34 80

www.e2v.com

Comparison between EV10AQ190 and EV10AQ190A

The new version of EV10AQ190 was to resolve a number of issues.

- Dependance on SYNC to internal clock state giving bistable outputs.
- Correction of flashing problem
- MISO signal problem.
- Potential for glitches at codes 250 / 750

These issues were reported in Errata sheets reference 1050, 1053 and 1060

All other functions of the device will remain as for the old version.

Table 1. Summary of Changes

EV10AQ190	**EV10AQ190A**	**Comments**
Chip ID 0x0418	Chip ID 0x41C	
Flashing	Flashing mode will now operate as per datasheet.	
MISO	Pull-up on MISO can still be employed; however no need now to buffer individual MISO signals in multi ADC applications.	
Sync	Sync will operate in two modes. 1. In mode described in previous datasheet. 2. In new mode described below.	Existing mode default New mode active on programming Control Register bit 10 '1'

SYNC Function

Existing SYNC Function

The existing SYNC timing is dependant on the rising edge of the SYNC signal and also on the falling edge. Where this falling edge occurs in relation to the internal ADC clock can cause an indeterminate timing of the start point of Data Ready (by 1 internal ADC clock cycle). This is outlined on the timing diagram below.
In addition the Data Ready signal will go permanently low while SYNC is active, this can cause problems if a PLL is used in the interface FPGA since this may lose lock.

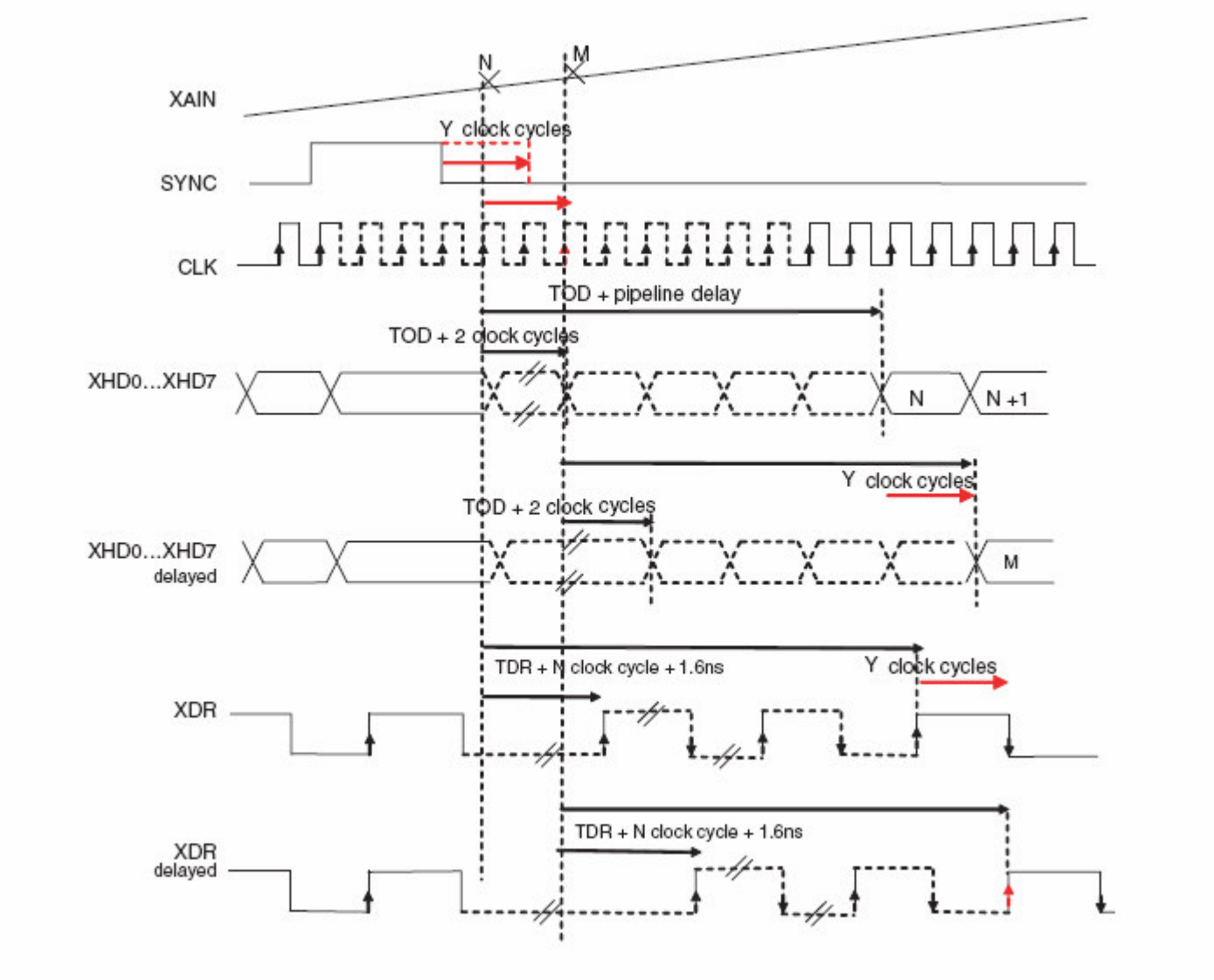


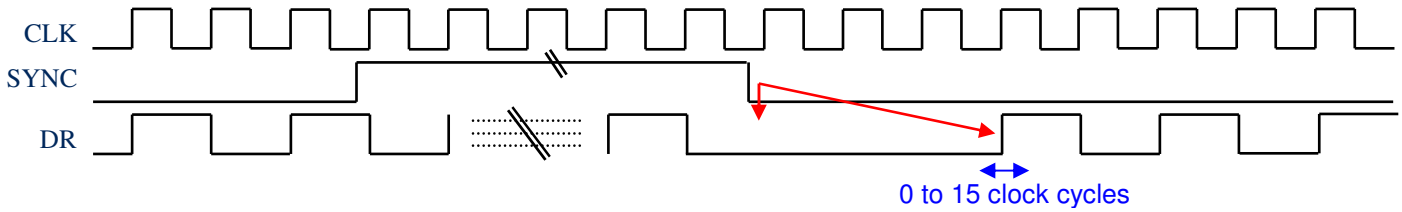
Fig. 1 Existing Sync Timing Function

EV10AQ190A will incorporate this functionality as default but the timing is now only dependant on the falling edge of the SYNC signal (this will avoid the potential bi-stable output of Data Ready). So in existing silicon N is 1 or 2 depending on length of SYNC pulse, in the new version N will not depend on SYNC pulse length.

SYNC alternative operation

A new functionality which can be selected using the Control register address 0x01 bit 10,available using SPI, will enable a SYNC mode that will not lock the Data Ready signal while SYNC is active.
The Data Ready signal will remain low for only a small (and fixed) number of clock cycles and then restart to toggle.

The timing diagram for this mode is shown below.



Note: timing values will be confirmed after characterisation.

Fig. 2 New SYNC timing Function

Ordering Code - Prototypes EVX10AQ190ATPY