Features

- **Operating Voltage: 3.3V**
- **Access Time: 40 ns**
- **Very Low Power Consumption**
  - **Active: 160 mW (Max)**
  - **Standby: 70 µW (Typ)**
- **Wide Temperature Range: -55·°C to +125·°C**
- **MFP 32 leads 400 Mils Width Package**
- **TTL Compatible Inputs and Outputs**
- **Asynchronous**
- **Designed on 0.35µm Process**
- **No Single Event Latch-up below a LET threshold of 80 MeV/mg/cm^2@125 °C**
- **Radiation Tolerance(1)**
  - **Tested up to a Total Dose of 300 krad (Si)**
  - **RHA capability of 100 krad (Si) according to MIL STD 883 Method 1019**
- **Quality grades: QML Q or V with SMD 5962-02501**

Notes: 1. tolerance to MBU's may need to be enhanced by the application

Description

The M65609E is a very low power CMOS static RAM organized as 131,072 x 8 bits.

Utilizing an array of six transistors (6T) memory cells, the M65609E combines an extremely low standby supply current with a fast access time at 40 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The M65609E is processed according to the methods of the latest revision of the MIL PRF 38535 and ESCC 9000.

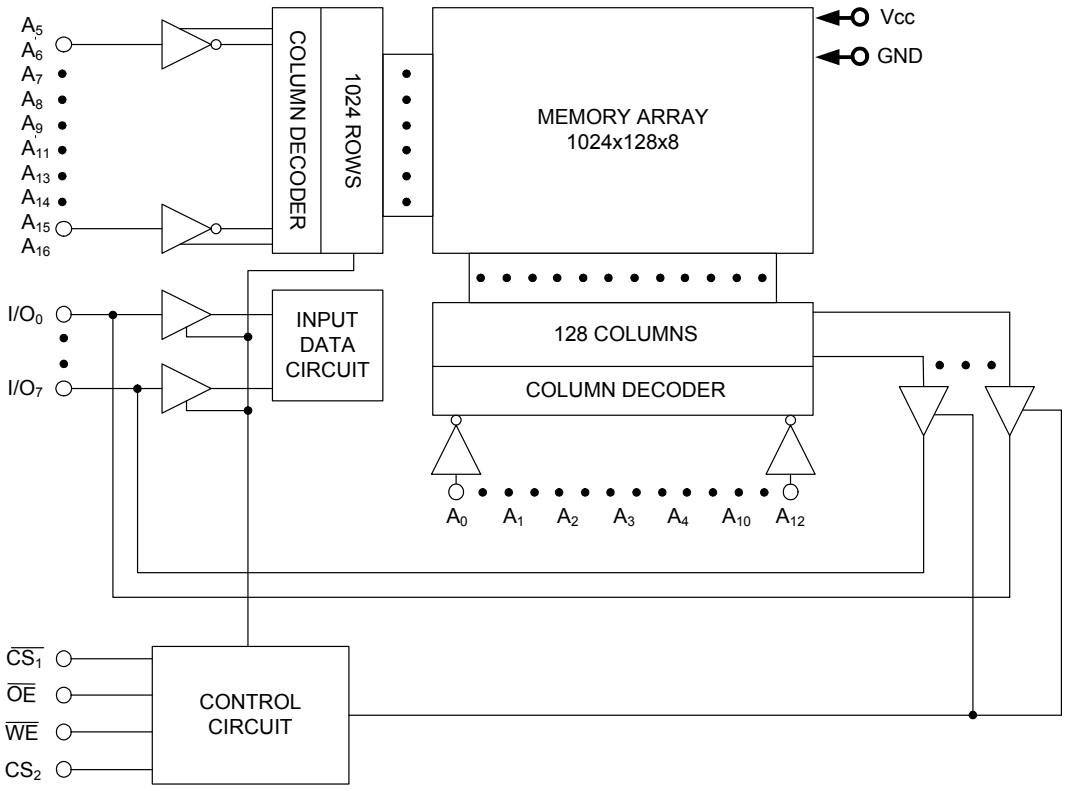
It is produced on the same process as the MH1RT sea of gates series.

Rad Hard 128K x 8 3.3-volt Very Low Power CMOS SRAM

M65609E

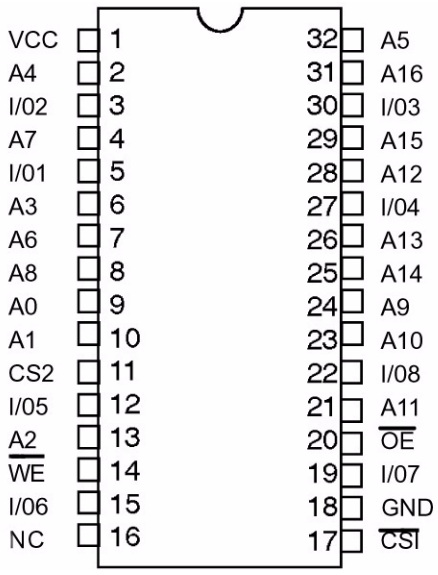
4158J–AERO–11/13

Block Diagram



Pin Assignment

Figure 1. 32 pins Flatpack 400 MILS



Pin Description

Name	Description
A0 - A16	Address Inputs
I/O1 - I/O8	Data Input/Output
$\overline{CS_1}$	Chip Select 1
CS_2	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

Table 1. Truth Table

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect/ Power-down
X	L	X	X	Z	Deselect/ Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage to GND Potential	-0.5V + 5V
DC Input Voltage	GND - 0.3V to V_{CC} + 0.3V
DC Output Voltage High Z State	GND - 0.3V to V_{CC} + 0.3V
Storage Temperature	-65·C to + 150·C
Output Current Into Outputs (Low)	20 mA
Electro Statics Discharge Voltage	> 500V
(MIL STD 883D Method 3015.3)	

*NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Military Operating Range

Operating Voltage	Operating Temperature
3.3V ± 0.3V	-55·C to + 125·C

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	V_{CC} + 0.3	V

Capacitance

Parameter	Description	Min	Typ	Max	Unit
C_{IN}[1]	Input low voltage	–	–	8	pF
C_{OUT}[1]	Output high voltage	–	–	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
IIX (1)	Input leakage current	-1	–	1	µA
IOZ (1)	Output leakage current	-1	–	1	µA
VOL (2)	Output low voltage	-	–	0.4	V
VOH (3)	Output high voltage	2.4	–	–	V

1. Gnd < Vin < V_{CC}, Gnd < Vout < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 4 mA.
3. V_{CC} min. IOH = -2 mA.

Consumption

Symbol	Description	65609E-40	Unit	Value
ICCSB (1)	Standby supply current	1.5	mA	max
$ICCSB_1$ (2)	Standby supply current	1	mA	max
ICCOP (3)	Dynamic operating current	45	mA	max

1. $\overline{CS_1} \geq$ VIH or $CS_2 \leq$ VIL and $\overline{CS_1} \leq$ VIL.
2. $\overline{CS_1} \geq V_{CC}$ - 0.3V or, $CS_2 <$ Gnd + 0.3V and $\overline{CS_1} \leq$ 0.2V
3. $F = 1/T_{AVAV}$, I_{OUT} = 0 mA, $\overline{W} = \overline{OE}$ = VIH, Vin = Gnd or V_{CC}, V_{CC} max.

AC Parameters

Test Conditions

Temperature Range ..... -55 +125 °C

Supply Voltage: ..... 3.3 ±0.3V

Input and Output Timing Reference Levels 1.5V

Test Loads and Waveforms

Figure 2. Test Loads

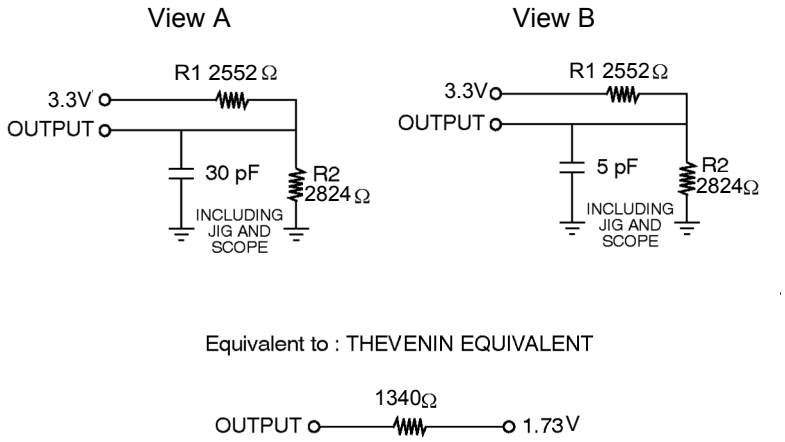
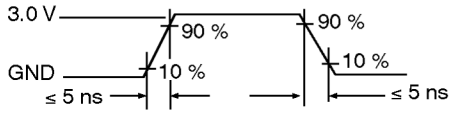


Figure 3. CMOS Input Pulses

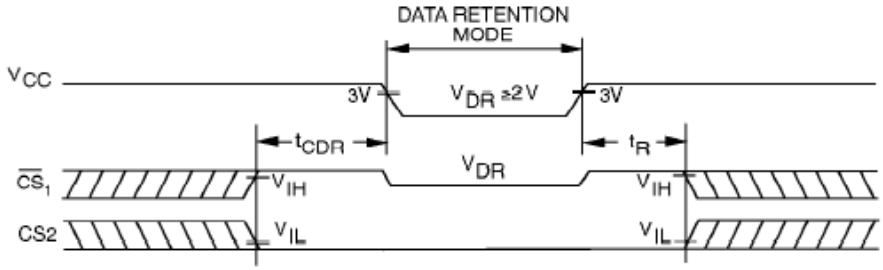


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention $\overline{CS1}$ must be held high within V_{CC} to V_{CC} - 0.2V or chip select $\overline{CS2}$ must be held down within GND to GND +0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions $\overline{CS1}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}, or with BS between GND and GND -0.3V.
4. The RAM can begin operation > t_R ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 4. Data Retention Timing



Data Retention Characteristics

Parameter	Description	Min	Typical T_A = 25·C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
T_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV} (1)	–	–	ns
I_{CCDR1} (2)	Data retention current at 2.0V	–	0.010	1.0	mA

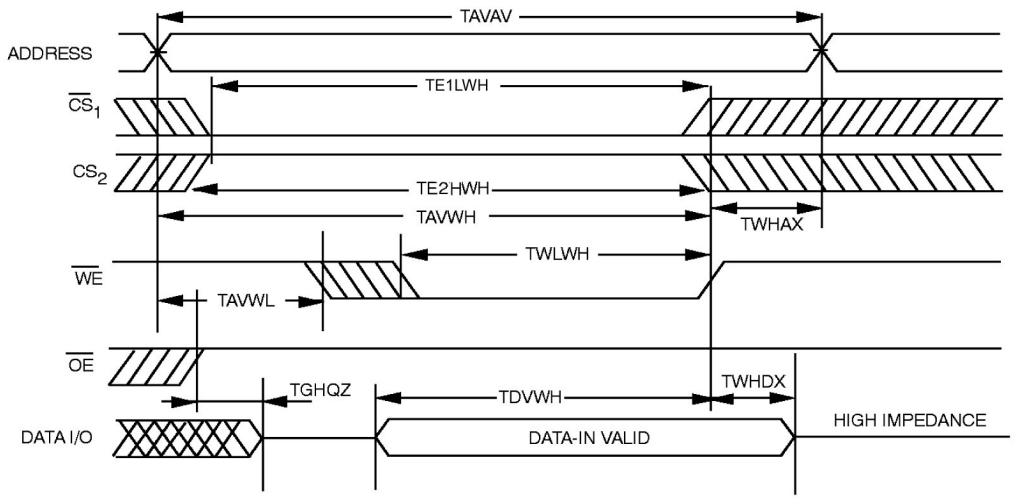
Notes: 1. TAVAV = Read Cycle Time
2. $\overline{CS1}$ = V_{CC} or CS2 = $\overline{CS1}$ = GND, V_{IN} = GND/V_{CC}.

Write Cycle

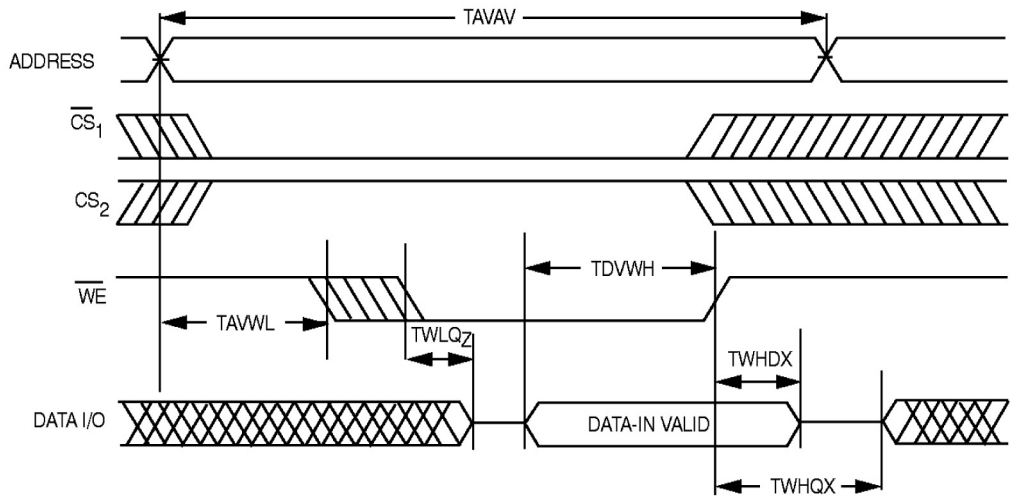
Symbol	Parameter	65609E-40	Unit	Value
t_{AVAW}	Write cycle time	35	ns	min
t_{AVWL}	Address set-up time	0	ns	min
t_{AVWH}	Address valid to end of write	28	ns	min
t_{DVWH}	Data set-up time	18	ns	min
t_{E1LWH}	$\overline{CS}_1$ low to write end	28	ns	min
t_{E2HWH}	CS_2 high to write end	28	ns	min
t_{WLQZ}	Write low to high Z (1)	15	ns	max
t_{WLWH}	Write pulse width	28	ns	min
t_{WHAX}	Address hold from to end of write	3	ns	min
t_{WHDX}	Data hold time	0	ns	min
t_{WHQX}	Write high to low Z (1)	0	ns	min

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see view B on Figure 2 on page 6).

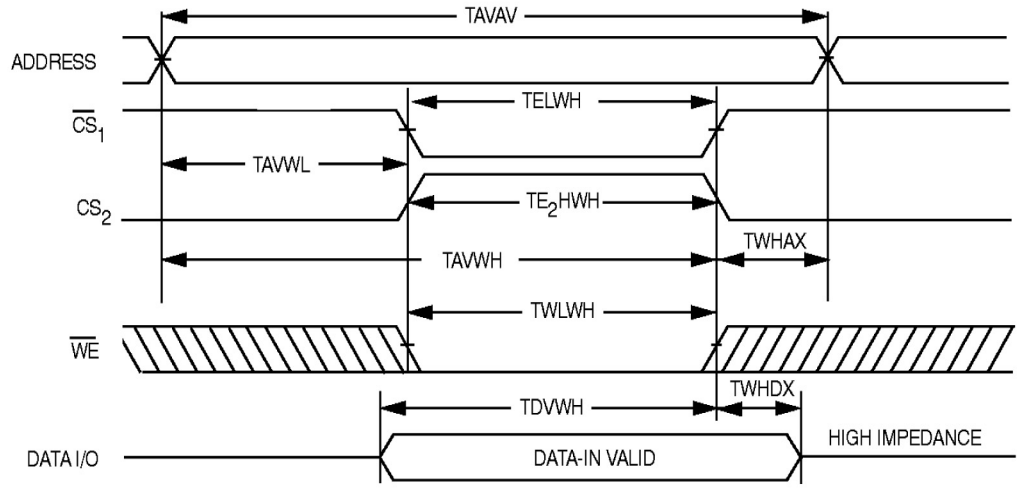
Write Cycle 1 — $\overline{WE}$ Controlled. $\overline{OE}$ High During Write



Write Cycle 2 **$\overline{WE}$ Controlled. $\overline{OE}$ Low**



Write Cycle 3. **$\overline{CS1}$ or CS2 Controlled[1]**



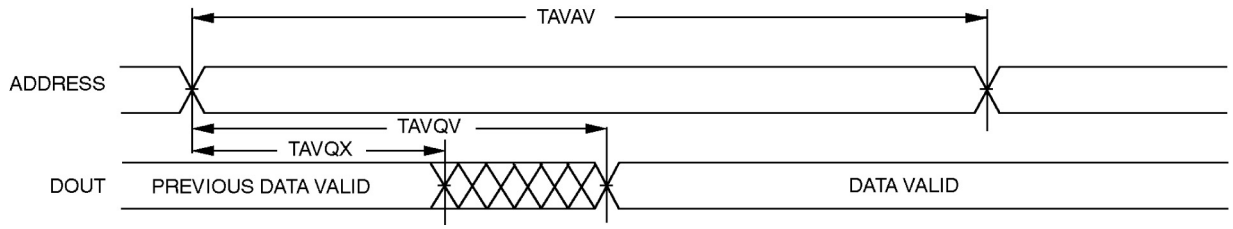
Note: 1. The internal write time of the memory is defined by the overlap of $\overline{CS1}$ LOW and CS2 HIGH and $\overline{W}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

Read Cycle

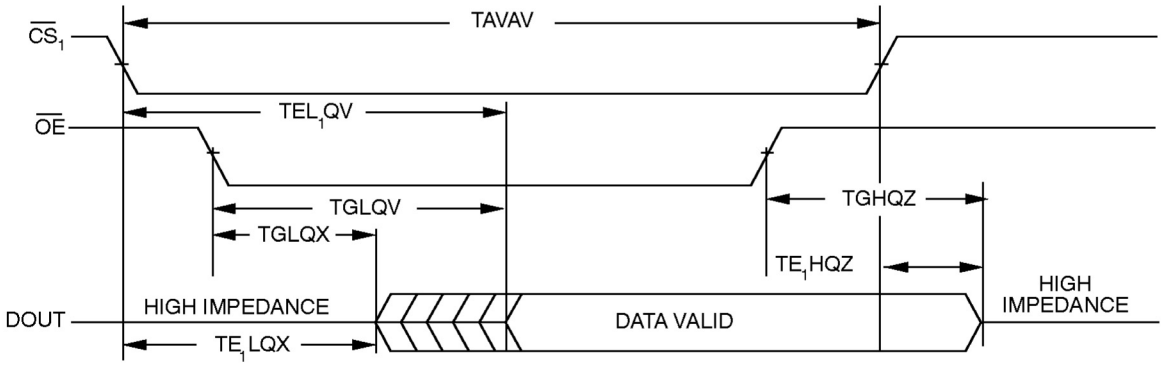
Symbol	Parameter	65609E-40	Unit	Value
t_{AVAV}	Read cycle time	40	ns	min
t_{AVQV}	Address access time	40	ns	max
t_{AVQX}	Address valid to low Z	3	ns	min
t_{E1LQV}	Chip-select$_1$ access time	40	ns	max
t_{E1LQX}	$\overline{CS}_1$ low to low Z (1)	3	ns	min
t_{E1HQZ}	$\overline{CS}_1$ high to high Z (1)	15	ns	max
t_{E2HQV}	Chip-select$_2$ access time	40	ns	max
t_{E2HQX}	CS_2 high to low Z (1)	3	ns	min
t_{E2LQZ}	CS_2 low to high Z (1)	15	ns	max
t_{GLQV}	Output Enable access time	12	ns	max
t_{GLQX}	$\overline{OE}$ low to low Z (1)	0	ns	min
t_{GHQZ}	$\overline{OE}$ high to high Z (1)	10	ns	max

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see view B on Figure 2 on page 6).

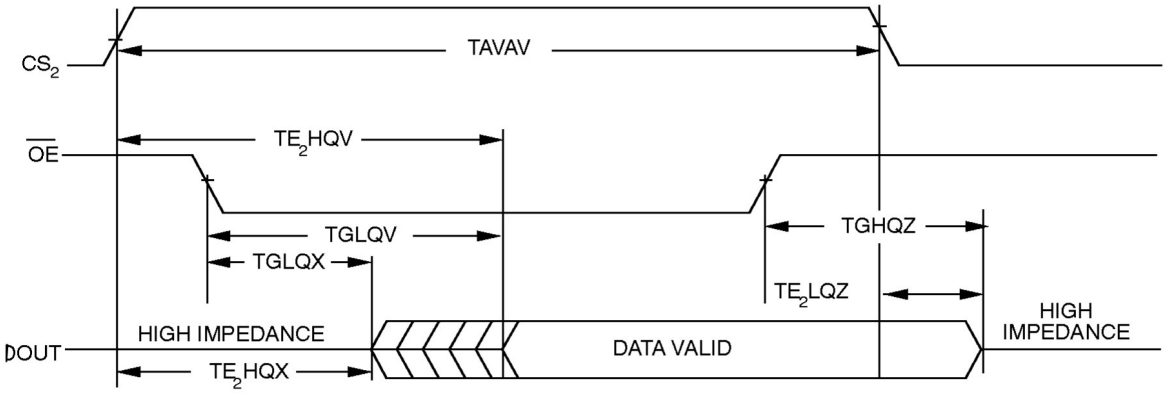
Read Cycle 1



Read Cycle 2



Read Cycle 3



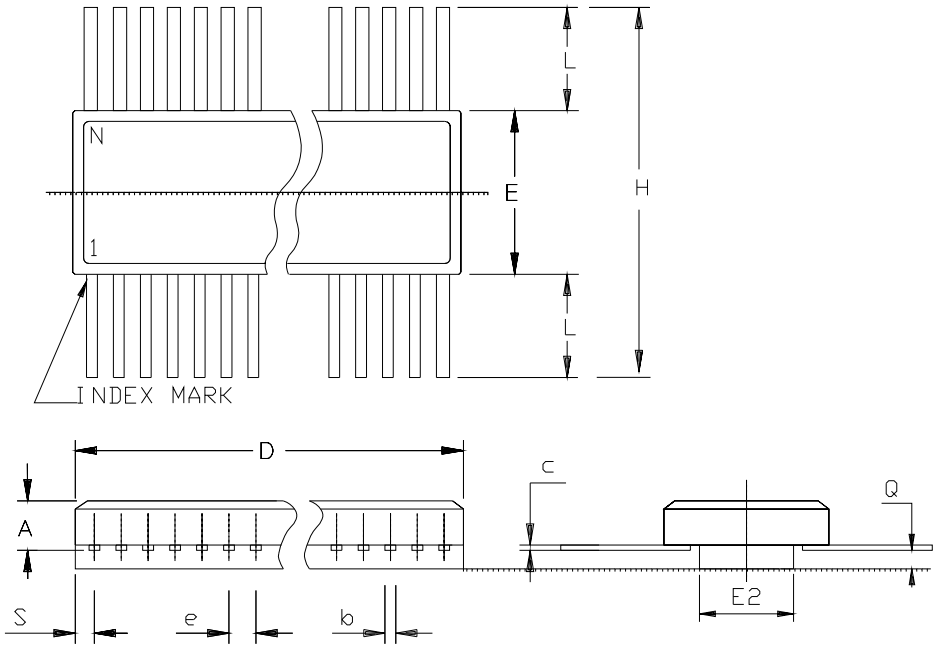
Ordering Information

Part Number	Temperature Range	Speed	Package	Flow
MMDJ-65609EV-40-E	25 °C	40 ns	FP32.4	Engineering Samples
5962-0250101QXC	-55 to +125 °C	40 ns	FP32.4	QML Q
5962-0250101VXC	-55 to +125 °C	40 ns	FP32.4	QML V
5962R0250101VXC	-55 to +125 °C	40 ns	FP32.4	QML V RHA
SMDJ-65609EV-40SCC	-55 to +125° C	40 ns	FP32.4	ESCC
MM0 -65609EV-40-E(1)	25 °C	40 ns	Die	Engineering Samples
MM0 -65609EV-40SV(1)	-55 to +125 °C	40 ns	Die	QML V

Note: 1. Contact Atmel for availability.

Package Drawing

32-pin Flat Pack (400 Mils)



	MM		INCH	
	Min	Max	Min	Max
A	1.78	2.72	.070	.107
b	0.38	0.48	.015	.019
c	0.076	0.18	.003	.007
D	20.62	21.03	.812	.828
E	10.26	10.57	.404	.416
E2	6.96	7.26	.274	.286
e	1.27 BSC		.050 BSC	
L	7.00	8.50	.276	.335
H	25.6	26.2	1.008	1.031
Q	0.51	0.76	.020	.030
S	---	1.14	---	.045
N	32		32	

Document Revision History

Changes from Rev. I to Rev. J

Add-on: MBU’s note in features section

Update: radiation tolerance specification in features section

Update: block diagram

Update: AC test conditions section

Update: package drawing

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature