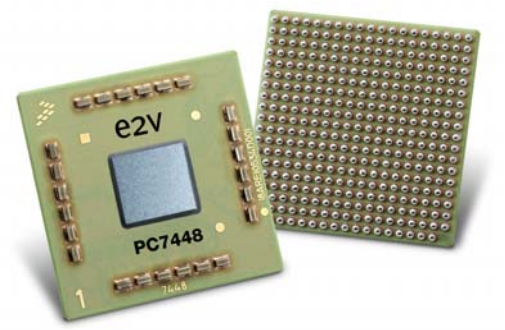
PC7448
PowerPC 7448 RISC Microprocessor

Datasheet

Features



- 3000 Dhrystone 2.1 MIPS at 1.3 GHz
- Selectable Bus Clock (30 CPU Bus Dividers up to 28x)
- Selectable MPx/60x Interface Voltage (1.5V; 1,8V; 2.5V)
- P_D Typically 10W at 1.25 GHz at V_{DD} = 1.1V Full Operating Conditions
- Nap, Doze and Sleep Power Saving Modes
- Superscalar (Four Instructions Fetched Per Clock Cycle)
- 4 GB Direct Addressing Range
- Virtual Memory: 4 Hexabytes (2^{52})
- 64-bit Data and 36-bit Address Bus Interface
- Integrated L1: 32 KB Instruction and 32 KB Data Cache
- Integrated L2: 1 MB with ECC
- 11 Independent Execution Units and 3 Register Files
- Write-back and Write-through Operations
- f_{INT} Max = 1267 MHz
- f_{BUS} Max = 133 MHz/166 MHz and 200 MHz

Description

This document is primarily concerned with the PowerPC® PC7448. The PC7448 is an implementation of the PowerPC microprocessor family of Reduced Instruction Set Computer (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the PC7448. For information regarding specific PC7448 part numbers covered by this document and part numbers covered by other documents, See “Ordering Information” on page 49. For functional characteristics of the processor, refer to the *PC7450 RISC Microprocessor Family Reference Manual*.

Screening

- Full Military Temperature Range (T_C = -55° C, T_J = +125° C)
- Industrial Temperature Range (T_C = -40° C, T_J = +110° C)

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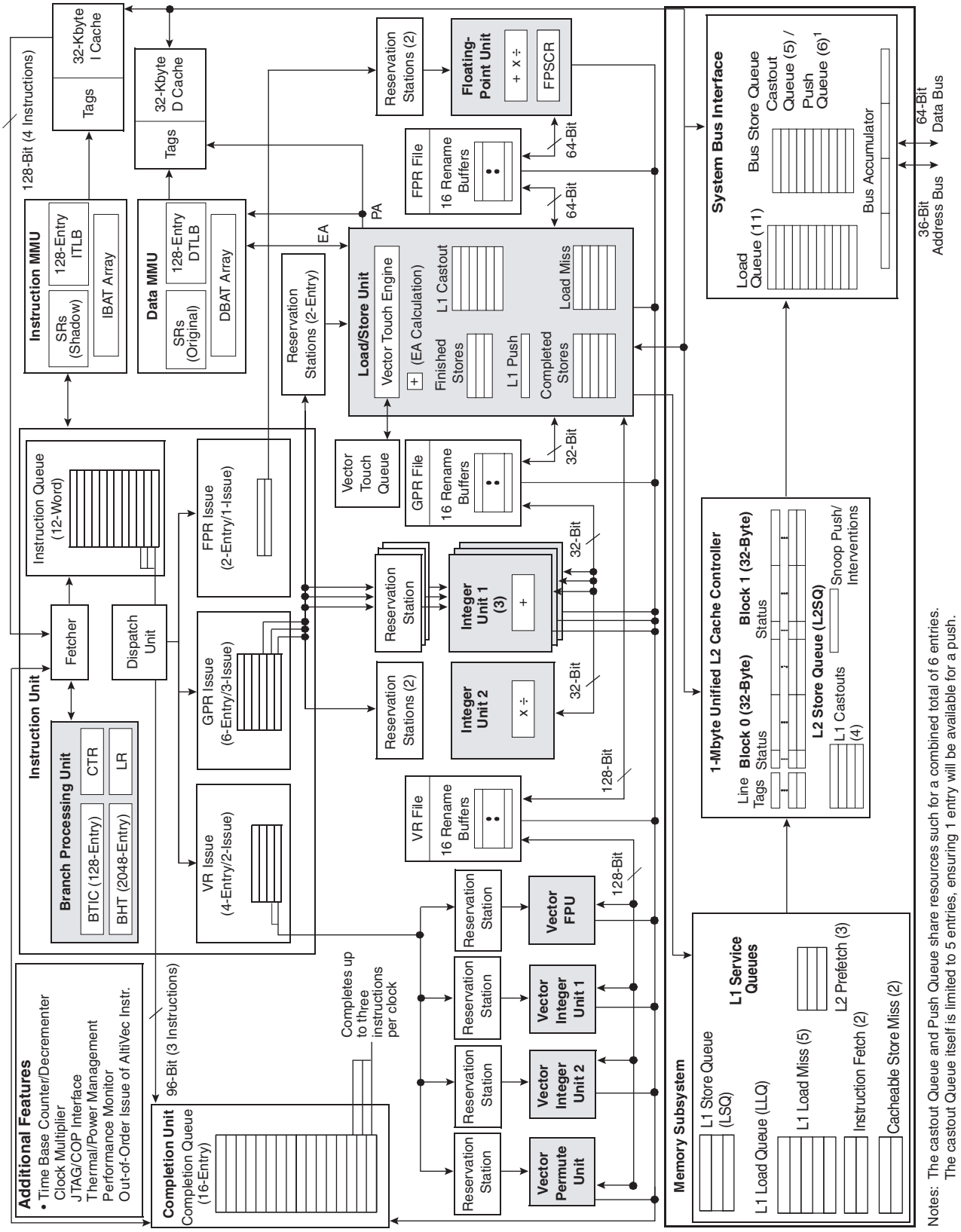
1. Overview

The PC7448 is the sixth implementation of fourth-generation (G4) microprocessors from Freescale™. The PC7448 implements the full PowerPC 32 bits architecture and is targeted at networking and computing systems applications. The PC7448 consists of a processor core and a 1 Mbyte L2.

Figure 1-1 on page 3 shows a block diagram of the PC7448. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit.

The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to main memory and other system resources.

Figure 1-1. PC7448 Block Diagram



Notes: The castout Queue and Push Queue share resources such for a combined total of 6 entries.
The castout Queue itself is limited to 5 entries, ensuring 1 entry will be available for a push.

Note that the PC7448 is a footprint-compatible, drop-in replacement in an PC7447A application if the core voltages are identical.

2. Features

This section summarizes features of the PC7448 implementation of the PowerPC architecture.

Major features of the PC7448 are as follows:

- High-performance, superscalar microprocessor

  Up to four instructions can be fetched from the instruction cache at a time

  Up to three instructions plus a branch instruction can be dispatched to the issue queues at a time

  Up to 12 instructions can be in the Instruction Queue (IQ)

  Up to 16 instructions can be at some stage of execution simultaneously

  Single-cycle execution for most instructions

  One instruction per clock cycle throughput for most instructions

  Seven-stage pipeline control

- Eleven independent execution units and three register files

  Branch Processing Unit (BPU) features static and dynamic branch prediction

  – 128-entry (32-set, four-way set-associative) Branch Target Instruction Cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream

  – 2048-entry Branch History Table (BHT) with 2 bits per entry for four levels of prediction: not taken, strongly not taken, taken, and strongly taken

  – Up to three outstanding speculative branches

  – Branch instructions that do not update the count register (CTR) or Link Register (LR) are often removed from the instruction stream

  – Eight-entry link register stack to predict the target address of branch conditional to link register (**bclr**) instructions

  Four Integer Units (IUs) that share 32 GPRs for integer operands

  – Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions

  – IU2 executes miscellaneous instructions, including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions

  Five-stage FPU and 32-entry FPR file

  – Fully IEEE® 754-1985 – compliant FPU for both single- and double-precision operations

  – Supports non-IEEE mode for time-critical operations

  – Hardware support for denormalized numbers

  – Thirty-two 64 bits FPRs for single or double-precision operands

  Four vector units and 32-entry Vector Register file (VRs).

  - Vector Permute Unit (VPU)
  - Vector Integer Unit 1 (VIU1) handles short-latency AltiVec® integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**)
  - Vector Integer Unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**)
  - Vector Floating-point Unit (VFPU)

  Three-stage Load/Store Unit (LSU)

  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry Vector Touch Queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - A dedicated adder calculates Effective Addresses (EAs)
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big and little-endian modes, including misaligned little-endian accesses

- Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:

  Instructions can only be dispatched from the three lowest IQ entries, IQ0, IQ1, and IQ2

  A maximum of three instructions can be dispatched to the issue queues per clock cycle

  Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)

- Rename buffers

  16 GPR rename buffers

  16 FPR rename buffers

  16 VR rename buffers

- Dispatch unit

  Decode/dispatch stage fully decodes each instruction

- Completion unit

  Retires an instruction from the 16-entry Completion Queue (CQ) when all instructions ahead of it have been completed, the instruction has finished executing, and no exceptions are pending

  Guarantees sequential programming model (precise exception model)

  Monitors all dispatched instructions and retires them in order

  Tracks unresolved branches and flushes instructions after a mispredicted branch

Retires as many as three instructions per clock cycle

- Separate on-chip L1 instruction and data caches (Harvard architecture)

  32-Kbyte, eight-way set-associative instruction and data caches

  Pseudo Least-Recently-Used (PLRU) replacement algorithm

  32-byte (eight-word) L1 cache block

  Physically indexed/physical tags

  Cache write-back or write-through operation programmable on a per-page or per-block basis

  Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle

  Caches can be disabled in software

  Caches can be locked in software

  MESI data cache coherency maintained in hardware

  Separate copy of data cache tags for efficient snooping

  Parity support on L1 and L2 cache and L2 tags

  No snooping of instruction cache except for **icbi** instruction

  Data cache supports AltiVec LRU and transient instructions

  Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding

- Level 2 (L2) cache interface

  On-chip, 1-Mbyte, eight-way set-associative unified instruction and data cache

  Cache write-back or write-through operation programmable on a per-page or per-block basis

  Parity support on cache tags

  ECC or parity support on data

  Error injection allows testing of error recovery software

- Separate Memory Management Units (MMUs) for instructions and data

  52-bit virtual address, 32- or 36-bit physical address

  Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments

  Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis

  Separate IBATs and DBATs (eight each) also defined as SPRs

  Separate instruction and data Translation Lookaside Buffers (TLBs)

  – Both TLBs are 128-entry, two-way set-associative and use an LRU replacement algorithm
  – TLBs are hardware- or software-reloadable (that is, a page table search is performed in hardware or by system software on a TLB miss)

- Efficient data flow

  Although the VR/LSU interface is 128 bits, the L1/L2 bus interface allows up to 256 bits

The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs

The L2 cache is fully pipelined to provide 32 bytes per clock every other cycle to the L1 caches

As many as 16 out-of-order transactions can be present on the MPX bus

Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)

Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache

Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache

- Multiprocessing support features include the following:

  Hardware-enforced, MESI cache coherency protocols for data cache

  Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations

- Power and thermal management

  Dynamic Frequency Switching (DFS) feature allows processor core frequency to be halved or quartered through software to reduce power consumption

  The following three power-saving modes are available to the system:

  – Nap: Instruction fetching is halted. Only the clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol
  – Sleep, Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled
  – Deep sleep: When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed upon exiting the deep sleep state

  Instruction cache throttling provides control of instruction fetching to limit device temperature

  A new temperature diode that can determine the temperature of the microprocessor

  Support for core voltage derating to further reduce power consumption

- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability

  LSSD scan design

  IEEE 1149.1 JTAG interface

- Reliability and serviceability

  Parity checking on system bus

  Parity checking on the L1 caches and L2 data tags

  ECC or parity checking on L2 data

3. Comparison with the PC7447A and PC7447

Table 3-1 compares the key features of the PC7448 with the key features of the earlier PC7447A and PC7447. All are based on the PC7450 RISC microprocessor and are architecturally very similar. The PC7448 is identical to the PC7447A, but the PC7448 supports 1 Mbyte of L2 cache with ECC and the use of Dynamic Frequency Switching (DFS) with more bus-to-core ratios.

Table 3-1. Microarchitecture Comparison

Microarchitectural Specs	PC7448	PC7447A	PC7447
Basic Pipeline Functions			
Logic inversions per cycle	18		
Pipeline stages up to execute	5		
Total pipeline stages (minimum)	7		
Pipeline maximum instruction throughput	3 + branch		
Pipeline Resources			
Instruction buffer size	12		
Completion buffer size	16		
Renames (integer, float, vector)	16, 16, 16		
Maximum Execution Throughput			
SFX	3		
Vector	2 (any 2 of 4 units)		
Scalar floating-point	1		
Out-of-Order Window Size in Execution Queues			
SFX integer units	1 entry × 3 queues		
Vector units	In order, 4 queues		
Scalar floating-point unit	In order		
Branch Processing Resources			
Prediction structures	BTIC, BHT, link stack		
BTIC size, associativity	128-entry, 4-way		
BHT size	2K-entry		
Link stack depth	8		
Unresolved branches supported	3		
Branch taken penalty (BTIC hit)	1		
Minimum misprediction penalty	6		
Execution Unit Timings (Latency-Throughput)			
Aligned load (integer, float, vector)	3-1, 4-1, 3-1		
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2		
L1 miss, L2 hit latency with ECC (data/instruction)	12/16	–	
L1 miss, L2 hit latency without ECC (data/instruction)	11/15	9/13	
SFX (add, sub, shift, rot, cmp, logicals)	1-1		

Table 3-1. Microarchitecture Comparison (Continued)

Microarchitectural Specs	PC7448	PC7447A	PC7447
Integer multiply (32 ×8, 32 ×16, 32 ×32)	4-1, 4-1, 5-2		
Scalar float	5-1		
VSFX (vector simple)	1-1		
VCFX (vector complex)	4-1		
VFPU (vector float)	4-1		
VPER (vector permute)	2-1		
MMUs			
TLBs (instruction and data)	128-entry, 2-way		
Tablewalk mechanism	Hardware + software		
Instruction BATs/data BATs	8/8		
L1 I Cache/D Cache Features			
Size	32K/32K		
Associativity	8-way		
Locking granularity	Way		
Parity on I cache	Word		
Parity on D cache	Byte		
Number of D cache misses (load/store)	5/2	5/1	
Data stream touch engines	4 streams		
On-Chip Cache Features			
Cache level	L2		
Size/associativity	1-Mbyte/ 8-way	512-Kbyte/8-way	
Access width	256 bits		
Number of 32-byte sectors/line	2	2	
Parity tag	Byte	Byte	
Parity data	Byte	Byte	
Data ECC	64 bits	–	
Thermal Control			
Dynamic frequency switching divide-by-two mode	Yes	Yes	No
Dynamic frequency switching divide-by-four mode	Yes	No	No
Thermal diode	Yes	Yes	No

4. General Parameters

The following list summarizes the general parameters of the PC7448:

Table 4-1. Device Parameters

Parameter	Description
Technology	90 nm CMOS SOI, nine-layer metal
Die size	8 mm × 7.3 mm
Transistor count	90 million
Logic design	Mixed static and dynamic
Packages	Surface mount 360 ceramic ball grid array (HiTCE) Surface mount 360 ceramic land grid array (HiTCE) RoHS HiTCE LGA Surface mount 360 ceramic ball grid array with lead-free spheres (HiTCE) = RoHS
Core power supply	1.1V ± 50 mV (1250 MHz) 1.05V ± 50 mV (1267 MHz) 1.0V ± 50 mV (1000 MHz)
I/O power supply	1.5V ± 5% DC, or 1.8V ± 5% DC, or 2.5V ± 5% DC

5. Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PC7448.

5.1 Detailed Specification

This specification describes the specific requirements for the microprocessor PC7448 in compliance with e2v standard screening.

5.2 Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.3 DC Electrical Characteristics

The tables in this section describe the PC7448 DC electrical characteristics. Table 5-1 provides the absolute maximum ratings.

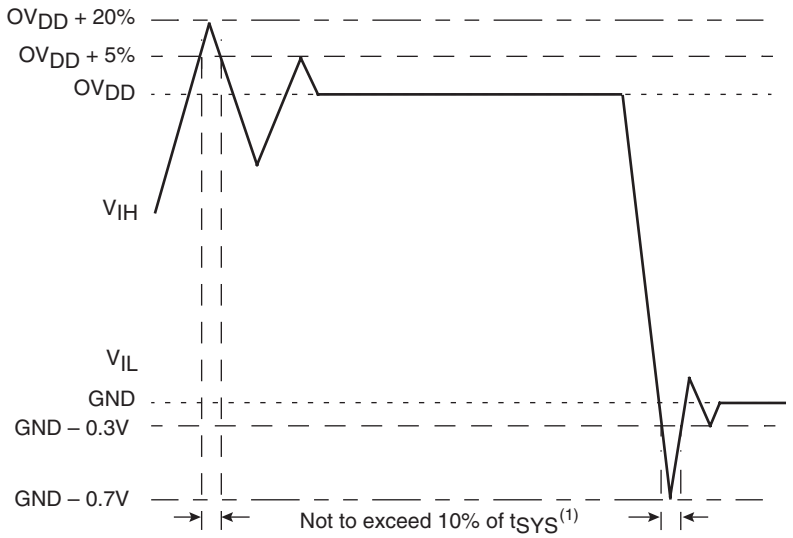
Table 5-1. Absolute Maximum Ratings(1)

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.4	V	(2)
PLL supply voltage		AV_{DD}	-0.3 to 1.4	V	(2)
Processor bus supply voltage	I/O Voltage Mode = 1.5V	OV_{DD}	-0.3 to 1.8	V	(3)
	I/O Voltage Mode = 1.8V		-0.3 to 2.2		(3)
	I/O Voltage Mode = 2.5V		-0.3 to 3.0		(3)
Input voltage	Processor bus	V_{IN}	-0.3 to OV_{DD} + 0.3	V	(4)
	JTAG signals	V_{IN}	-0.3 to OV_{DD} + 0.3	V	
Storage temperature range		Tstg	-65 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Table 5-3 on page 12. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. See Section 9.2 "Power Supply Design and Sequencing" on page 33 for power sequencing requirements.
3. Bus must be configured in the corresponding I/O voltage mode; see Table 5-2 on page 12.
4. **Caution**: V_{IN} must not V_{IN} OV_{DD} by more than 0.3V at any time including during power-on reset except as allowed by the overshoot specifications. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5-1.

Figure 5-1 shows the undershoot and overshoot voltage on the PC7448.

Figure 5-1. Overshoot/Undershoot Voltage



The PC7448 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7448 core voltage must always be provided at the nominal voltage (see Table 5-3 on page 12) or at the supported derated voltage (see Section 5.5 "Voltage and Frequency Derating" on page 22).

The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$.

The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 5-2 on page 12 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future, if necessary.

Table 5-2. Input Threshold Voltage Setting

BVSEL0	BVSEL1	I/O Voltage Mode(1)	Notes
0	0	1.8V	(2)(3)
0	1	2.5V	(2)(4)
1	0	1.5V	(2)
1	1	2.5V	(4)

Notes:
1. **Caution:** The I/O voltage mode selected must agree with the OV_{DD} voltages supplied. See Table 5-3.
2. If used, pull-down resistors should be less than 250Ω
3. The pin configuration used to select 1.8V mode on the PC7448 is not compatible with the pin configuration used to select 1.8V mode on the PC7447A and earlier devices.
4. The pin configuration used to select 2.5V mode on the PC7448 is fully compatible with the pin configuration used to select 2.5V mode on the PC7447A and earlier devices.

Table 5-3 provides the recommended operating conditions for the PC7448 part numbers described by this document.

Note: Table 5-3 describes the nominal operating conditions of the device. For information regarding the operation of the device at supported derated core voltage conditions, see Section 5.5 "Voltage and Frequency Derating" on page 22.

Table 5-3. Recommended Operating Conditions(1)

Characteristic		Symbol	Recommended Value						Unit	Notes
			1000 MHz		1250 MHz		1267 MHz			
			Min	Max	Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.0V ± 50 mV		1.1V ± 50 mV		1.05V ± 50 mV		V	(3)
PLL supply voltage		AV_{DD}	1.0V ± 50 mV		1.1V ± 50 mV		1.05V ± 50 mV		V	(2)(3)
Processor bus supply voltage	I/O Voltage mode = 1.5V	OV_{DD}	1.5V ± 5%						V	(4)
	I/O Voltage mode = 1.8V		1.8V ± 5%							(4)
	I/O Voltage mode = 2.5V		2.5V ± 5%							(4)
Input voltage	Processor bus	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}	V	
	JTAG signals	V_{IN}	GND	OV_{DD}	GND	OV_{DD}	GND	OV_{DD}		
Operating temperature		T_J	T_C = -55	T_J = +125	T_C = -55	T_J = +125	T_C = -55	T_J = +125	°C	

Notes:
1. These are the recommended and tested operating conditions. In addition, these devices also support voltage derating; see Section 5.5 ”Voltage and Frequency Derating” on page 22. Proper device operation outside of these conditions and those specified in Section 5.5 on page 22 is not guaranteed.
2. This voltage is the input to the filter discussed in Section 9.2.2 ”PLL Power Supply Filtering” on page 35 and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. V_{DD} and AV_{DD} may be reduced in order to reduce power consumption if further maximum core frequency constraints are observed. See Section 5.5 ”Voltage and Frequency Derating” on page 22, for specific information.
4. **Caution:** Power sequencing requirements must be met; see Section 9.2 ”Power Supply Design and Sequencing” on page 33.
5. See Section 9.2.3 ”Transient Specifications” on page 35 for information regarding transients on this power supply.

Table 5-4 provides the package thermal characteristics for the PC7448. For more information regarding thermal management, see Section 9.8, “Thermal Management Information.”

Table 5-4. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	26	°C/W	(2)(3)
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	19	°C/W	(2)(4)
Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	$R_{\theta JMA}$	22	°C/W	(2)(4)
Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	$R_{\theta JMA}$	16	°C/W	(2)(4)
Junction-to-board thermal resistance	$R_{\theta JB}$	11	°C/W	(5)
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	°C/W	(6)

Notes:
1. Refer to Section 9.8, “Thermal Management Information,” for details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 5-5 provides the DC electrical characteristics for the PC7448.

Table 5-5. DC Electrical Specifications (At Recommended Operating Conditions, see Table 5-3 on page 12)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs)	1.5	V_{IH}	$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$	V	(2)
	1.8		$OV_{DD} \times 0.65$	$OV_{DD} + 0.3$		
	2.5		1.7	$OV_{DD} + 0.3$		
Input low voltage (all inputs)	1.5	V_{IL}	-0.3	$OV_{DD} \times 0.35$	V	(2)
	1.8		-0.3	$OV_{DD} \times 0.35$		
	2.5		-0.3	0.7		

Table 5-5. DC Electrical Specifications (At Recommended Operating Conditions, see Table 5-3 on page 12)

Characteristic		Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input leakage current, V_{IN} = GV_{DD}/O_{DD} V_{IN} = GND		–	I_{IN}	–	50 -50	µA	(2)(3)
High-impedance (off-state) leakage current, V_{IN} = GV_{DD}/O_{DD} V_{IN} = GND		–	I_{TSI}	–	50 -50	µA	(2)(3)(4)
Output high voltage at I_{OH} = -5 mA		1.5	V_{OH}	OV_{DD} - 0.45	–	V	
		1.8		OV_{DD} - 0.45	–		
		2.5		1.8	–		
Output low voltage at I_{OL} = 5 mA		1.5	V_{OL}	–	0.45	V	
		1.8		–	0.45		
		2.5		–	0.6		
Capacitance, V_{IN} = 0V, f = 1 MHz	All inputs		C_{IN}	–	8	pF	(5)

Notes:
1. Nominal voltages; see Table 5-3 for recommended operating conditions.
2. All I/O signals are referenced to OV_{DD}.
3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals.
4. The leakage is measured for nominal OV_{DD}/GV_{DD} and V_{DD}, or both OV_{DD}/GV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).
5. Capacitance is periodically sampled rather than 100% tested.

Table 5-6 provides the power consumption for the PC7448 part numbers described by this document; see Section 10. "Ordering Information" on page 49, for more information. For information regarding power consumption when dynamic frequency switching is enabled, see Section 9.7.5 "Dynamic Frequency Switching (DFS)" on page 47.

Note: The power consumption information in this table applies when the device is operated at the nominal core voltage indicated in Table 5-6. For power consumption at derated core voltage conditions, see Section 5.5 "Voltage and Frequency Derating" on page 22..

Table 5-6. Power Consumption for PC7448

	Processor (CPU) Frequency			Unit	Notes
	1000 MHz	1250 MHz	1267 MHz[7]		
Full-Power Mode					
Typical	9.5	10	8.4	W	(1)(2)
Typical Thermal	12	12.6	10.3	W	(1)(5)
Maximum	13.9	14.6	12.0	W	(1)(3)
Nap Mode					
Typical	6.5	8.3	6.5	W	(1)(6)
Sleep Mode					

Table 5-6. Power Consumption for PC7448 (Continued)

	Processor (CPU) Frequency			Unit	Notes
	1000 MHz	1250 MHz	1267 MHz[7]		
Typical	6.3	8	6.3	W	(1)(6)
Deep Sleep Mode (PLL Disabled)					
Typical	6	7.7	6.0	W	(1)(6)

Notes:
1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 13 mW.
2. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 5-3 on page 12) and 65° C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Maximum power is the average measured at nominal V_{DD} and 125° C junction temperature while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.
5. Typical thermal power consumption is an average value measured at the nominal recommended V_{DD} (see Table 5-3 on page 12) and 105° C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz. This parameter is not 100% tested but periodically sampled.
6. Typical power consumption for these modes is measured at the nominal recommended V_{DD} (see Table 5-3 on page 12) and 105° C in the mode described. This parameter is not 100% tested but is periodically sampled.
7. Power consumption for the 1267 MHz device is intentionally constrained via testing and sorting to assure low power consumption for this device.

5.4 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PC7448. After fabrication, functional parts are sorted by maximum processor core frequency as shown in "Clock AC Specifications" , and tested for conformance to the AC specifications for that frequency. The processor core frequency, determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:5] signals, can be dynamically modified using Dynamic Frequency Switching (DFS). Parts are sold by maximum processor core frequency.See Section 9.7.5 "Dynamic Frequency Switching (DFS)" on page 47.

5.4.1 Clock AC Specifications

Table 5-7 on page 16 provides the clock AC timing specifications for the PC7448 part numbers described herein.

Note: The core frequency information in this table applies when the device is operated at the nominal core voltage indicated in Table 5-3 on page 12. For core frequency specifications at derated core voltage conditions, see Section 5.5 "Voltage and Frequency Derating" on page 22.

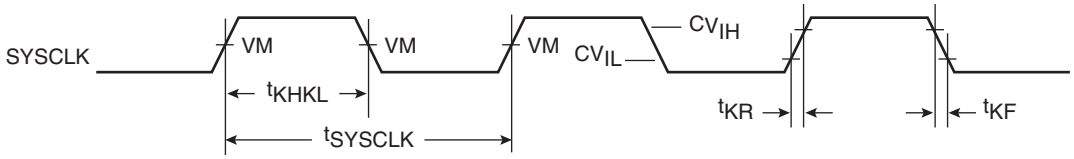
Table 5-7. Clock AC Timing Specifications (At Recommended Operating Conditions, see Table 5-3 on page 12)

Characteristic		Symbol	Maximum Processor Core Frequency						Unit	Notes
			1000 MHz		1250 MHz		1267 MHz			
			Min	Max	Min	Max	Min	Max		
Processor frequency	DFS mode disabled	f_{CORE}	500	1000	500	1250	500	1267	MHz	(1)(8)(9)
	DFS mode enabled	$f_{CORE-DFS}$	250	500	250	625	250	633		(10)
VCO frequency		f_{VCO}	500	1000	500	1250	500	1267	MHz	(1)(9)
SYSCLK frequency		f_{SYSCLK}	33	200	33	200	33	200	MHz	(1)(2)(8)
SYSCK cycle time		t_{SYSCLK}	5	30	5	30	5	30	ns	(2)
SYSCLK rise and fall time		t_{KR}, t_{KF}	–	0.5	–	0.5	–	0.5	ns	(3)
SYSCLK duty cycle measured at $OV_{DD}/2$		t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	(4)
SYSCLK cycle-to-cycle jitter			–	150	–	150	–	150	ps	(5)(6)

Notes:
1. **Caution:** The SYSCLK frequency and PLL_CFG[0:5] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:5] signal description in Section 9.1.1 "PLL Configuration" on page 31, for valid PLL_CFG[0:5] settings.
2. Actual maximum system bus frequency is system-dependent. See Section 5.4.1 "Clock AC Specifications" on page 15.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
8. This reflects the maximum and minimum core frequencies when the Dynamic Frequency Switching feature (DFS) is disabled. f_{CORE_DFS} provides the maximum and minimum core frequencies when operating in a DFS mode.
9. **Caution**: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced. See Section 5.5 "Voltage and Frequency Derating" on page 22, for more information.
10. This specification is provided to support use of the Dynamic Frequency Switching (DFS) feature and is applicable only when one of the DFS modes (divide-by-2 or divide-by-4) has been enabled. When DFS is disabled, the core frequency must conform to the maximum and minimum frequencies stated for f_{CORE}.
11. Use of the DFS feature does not affect VCO frequency.

Figure 5-2 provides the SYSCLK input timing diagram.

Figure 5-2. SYSCLK Input Timing Diagram



Note: V_M = Midpoint Voltage ($OV_{DD}/2$)

5.4.2 Processor Bus AC Specifications

Table 5-8 provides the processor bus AC timing specifications for the PC7448 as defined in Figure 5-3 on page 18 and Figure 5-4 on page 18..

Table 5-8. Processor Bus AC Timing Specifications[1] (At Recommended Operating Conditions, see Table 5-3 on page 12)

Parameter	Symbol[2]	All Speed Grades		Unit	Notes
		Min	Max		
Input setup times:					
A[0:35], AP[0:4]	t_{AVKH}	1.5	–		–
D[0:63], DP[0:7]	t_{DVKH}	1.5	–		–
AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:3], QACK, TA, TBEN, TEA, TS,EXT_QUAL, PMON_IN, SHD[0:1], BMODE[0:1], BVSEL[0:1]	t_{IVKH}	1.5	–	ns	–
	t_{MVKH}	1.5	–		[8]
Input hold times:					
A[0:35], AP[0:4]	t_{AXKH}	0	–		–
D[0:63], DP[0:7]	t_{DXKH}	0	–		–
AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:3], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1]	t_{IXKH}	0	–	ns	–
BMODE[0:1], BVSEL[0:1]	t_{MXKH}	0	–		[8]
Output valid times:					
A[0:35], AP[0:4]	t_{KHAV}	–	1.8		
D[0:63], DP[0:7]	t_{KHDV}	–	1.8		
AACK, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], WT	t_{KHOV}	–	1.8	ns	
TS	t_{KHTSV}	–	1.8		
ARTRY, SHD[0:1]	t_{KHARV}	–	1.8		
Output hold times:					
A[0:35], AP[0:4]	t_{KHAX}	0.5	–		
D[0:63], DP[0:7]	t_{KHDX}	0.5	–		
AACK, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], WT	t_{KHOX}	0.5	–	ns	
TS, ARTRY, SHD[0:1]	t_{KHTSX}	0.5	–		
	t_{KHARX}	0.5	–		
SYSCLK to output enable	t_{KHOE}	0.5	–	ns	[5]
SYSCLK to output high impedance (all except TS, ARTRY, SHD0, SHD1)	t_{KHOZ}	–	1.8	ns	[5]
SYSCLK to TS high impedance after precharge	t_{KHTSPZ}	–	1	t_{SYSCLK}	[3][4][5]
Maximum delay to ARTRY/SHD0/SHD1 precharge	t_{KHARP}	–	1	t_{SYSCLK}	[3][5][6][7]
SYSCLK to ARTRY/SHD0/SHD1 high impedance after precharge	t_{KHARPZ}	–	2	t_{SYSCLK}	[3][5][6][7]

Notes: 1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 5-3 on page 18). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{TS}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 5-5 on page 19. The nominal precharge width for $\overline{TS}$ is t_{SYSCLK}, that is, one clock period. Since no master can assert $\overline{TS}$ on the following clock edge, there is no concern regarding contention with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue because any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 5-5 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{SHD0}$ and $\overline{SHD1}$ can be driven by multiple bus masters beginning two cycles after $\overline{TS}$. Timing is the same as $\overline{ARTRY}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{SHD0}$ and $\overline{SHD1}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{BMODE}$[0:1] and BVSEL[0:1] are mode-select inputs. $\overline{BMODE}$[0:1] are sampled before and after $\overline{HRESET}$ negation. BVSEL[0:1] are sampled before $\overline{HRESET}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. $\overline{BMODE}$[0:1] must remain stable after the second sample; BVSEL[0:1] must remain stable after the first (and only) sample. See Figure 5-4 on page 18 for sample timing.

Figure 5-6 provides the AC test load for PC7448.

Figure 5-3. AC Test Load

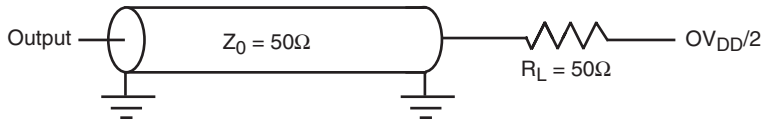
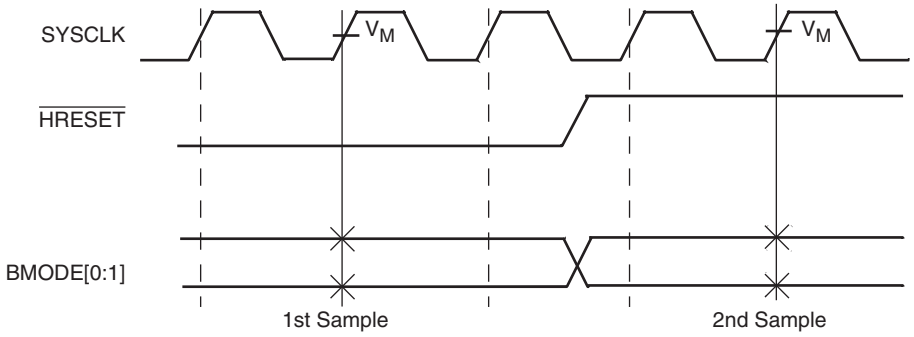


Figure 5-4 provides the $\overline{BMODE}$[0:1] input timing diagram for the PC7448. These mode select inputs are sampled once before and once after $\overline{HRESET}$ negation.

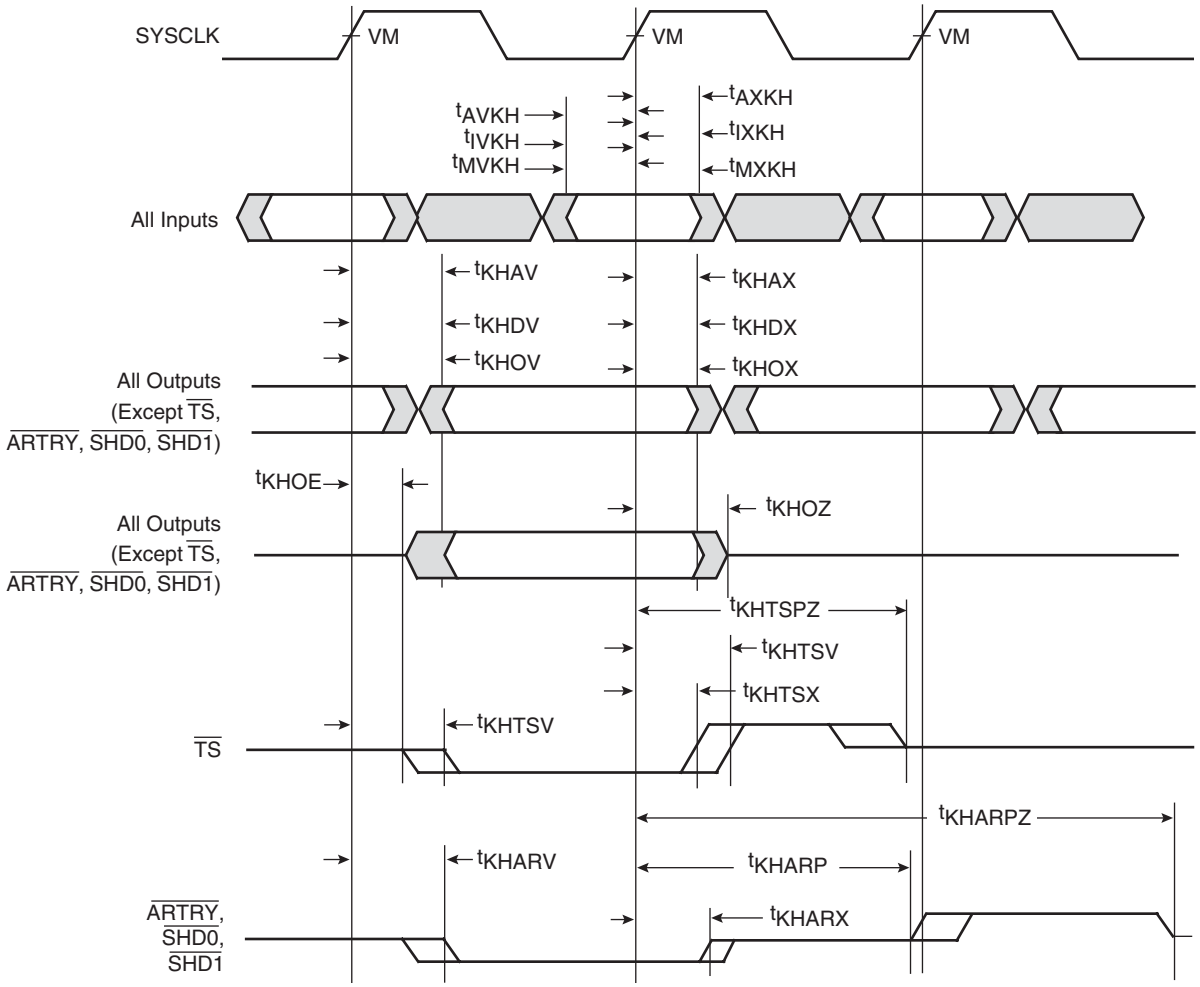
Figure 5-4. $\overline{BMODE}$[0:1] Input Sample Timing Diagram



Note: V_M = Midpoint Voltage (OV_{DD}/2)

Figure 5-5 provides the input/output timing diagram for the PC7448.

Figure 5-5. Input/Output Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

5.4.3 IEEE 1149.1 AC Timing Specifications

Table 5-9 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 5-7 on page 21 through Figure 5-10 on page 22.

Table 5-9. JTAG AC Timing Specifications (Independent of SYSCLK)(1)
(At Recommended Operating Conditions, see Table 5-3 on page 12)

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	–	ns	
TCK clock pulse width measured at 1.4V	t_{JHJL}	15	–	ns	
TCK rise and fall times	t_{JR} and t_{JF}	–	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	–	ns	(2)
Input Setup Times: - Boundary-scan data - TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 – –	ns	(3)
Input Hold Times: - Boundary-scan data - TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 – –	ns	(3)
Valid Times: - Boundary-scan data - TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	(4)
Output hold times: - Boundary-scan data - TDO	 t_{JLDX} t_{JLOX}	 30 30	 – –	ns	(4)
TCK to output high impedance: - Boundary-scan data - TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	(4)(5)

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 5-6). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 5-6 provides the AC test load for TDO and the boundary-scan outputs of the PC7448.

Figure 5-6. Alternate AC Test Load for the JTAG Interface

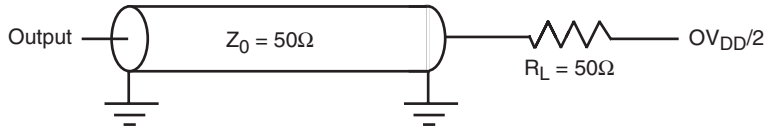
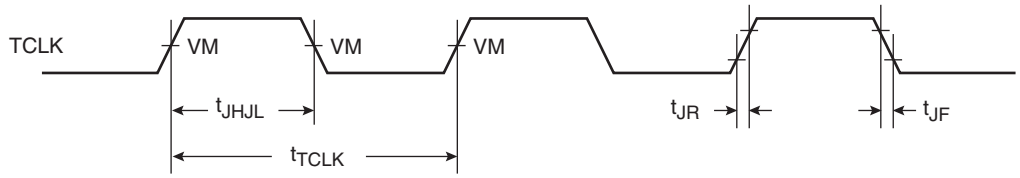


Figure 5-7 provides the JTAG clock input timing diagram.

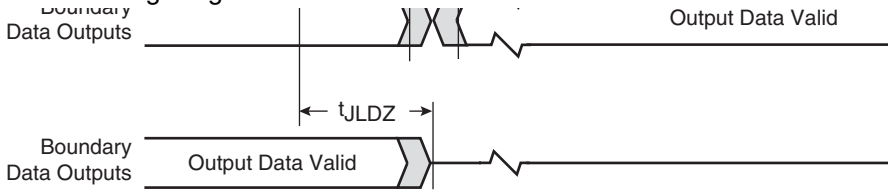
Figure 5-7. JTAG Clock Input Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 5-8 provides the $\overline{TRST}$ timing diagram.

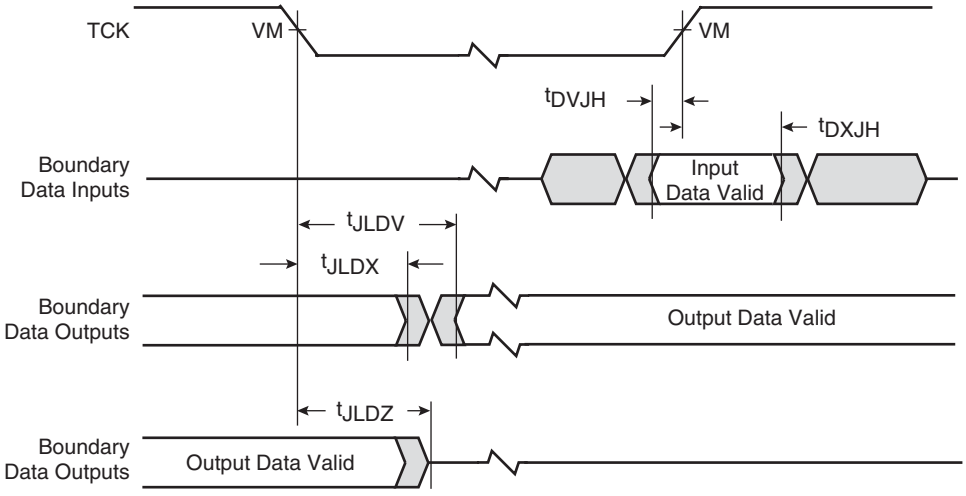
Figure 5-8. $\overline{TRST}$ Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 5-9 provides the boundary-scan timing diagram.

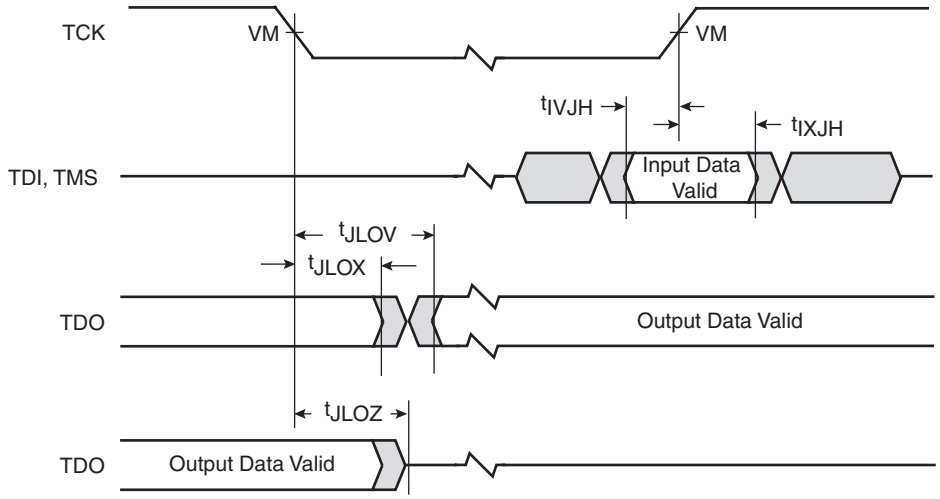
Figure 5-9. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 5-10 provides the test access port timing diagram.

Figure 5-10. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

5.5 Voltage and Frequency Derating

To reduce the power consumption of the device, these devices support voltage and frequency derating whereby the core voltage (V_{DD}) may be reduced if the reduced maximum processor core frequency requirements are observed. The supported derated core voltage, resulting maximum processor core frequency (f_{core}), and power consumption are provided in Table 5-10. Only those parameters in Table 5-10 are affected; all other parameter specifications are unaffected.

Table 5-10. Supported Voltage, Core Frequency, and Power Consumption Derating

Maximum Rated Core Frequency (Device Marking)	Supported Derated Core Voltage (V_{DD})	Maximum Derated Core Frequency (f_{core})	Full-Power Mode Power Consumption		
			Typical	Thermal	Maximum
1000	NA				
1250	NA				
1267	1.0V ± 50 mV	1000 MHz	6.0W	7.3W	8.5W

6. Pin Assignments

Figure 6-1 shows the pinout of the PC7448, 360 high coefficient of the thermal expansion ceramic ball grid array (HiTCE) package as viewed from the top surface. Figure 6-2 shows the side profile of the HiTCE package to indicate the direction of the top surface view.

Figure 6-1. Pinout of the PC7448, 360 HITCE Package as Viewed from the Top Surface

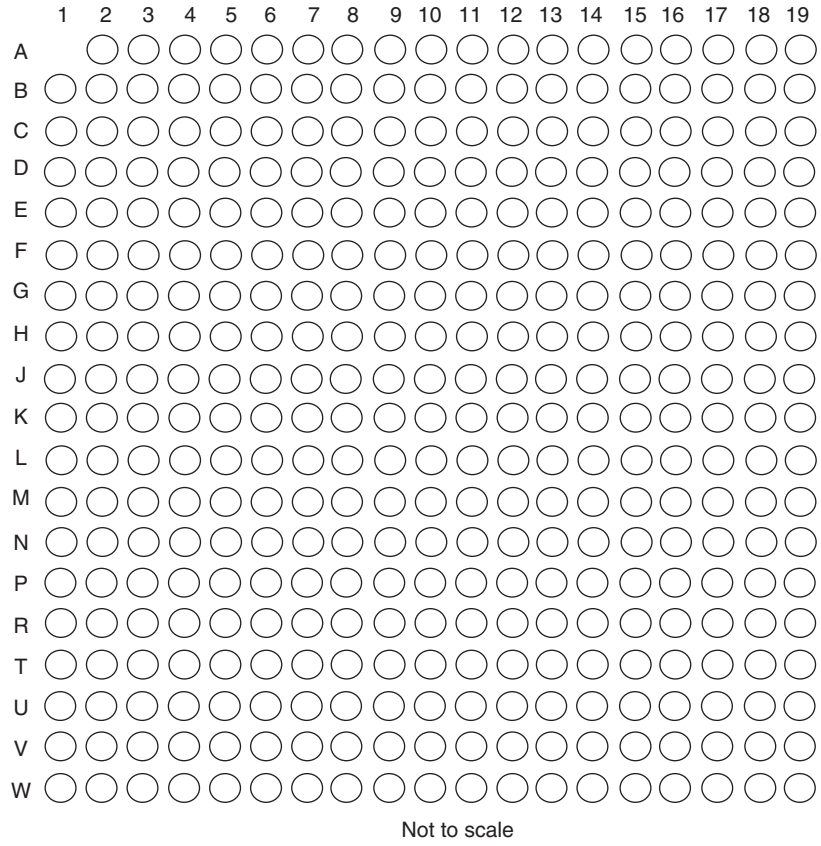
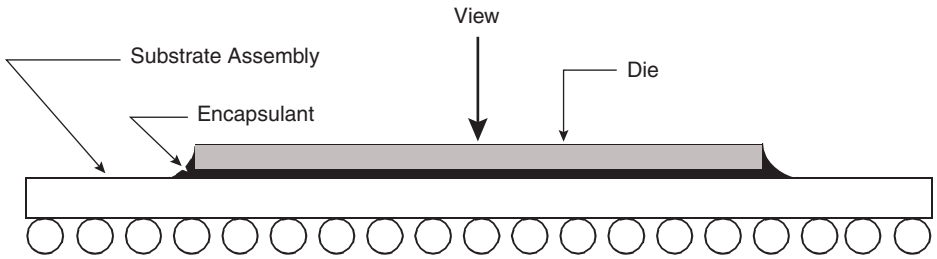


Figure 6-2. Pinout of the PC7448, 360 HiTCE Package as Viewed from the Top Surface



7. Pinout Listings

Table 7-1 provides the pinout listing for the PC7448, 360 HiTCE package. The pinouts of the PC7448 and PC7447A are pin compatible, but the requirements regarding the use of the additional power and ground pins may change. The PC7448 may require these pins be connected to the appropriate power or ground plane to achieve the full rated core frequency. As a result, these pins should be connected in all new designs.

Additionally, the PC7448 may be populated on a board designed for a PC7447 (or PC7445 or PC7441), provided the core voltage can be made to match the requirements in Table 5-3 and all pins defined as 'no connect' for the PC7447 are unterminated, as required by the PC7457 RISC Microprocessor Hardware Specifications. The PC7448 uses pins previously marked 'no connect' for the temperature diode pins and for additional power and ground connections. The additional power and ground pins are required to achieve high core frequencies; see Section 9.3 "Connection Recommendations" on page 37, for additional information. Because these 'no connect' pins in the PC7447 360 pin package are not driven in functional mode, an PC7447 can be populated in an PC7448 board.

Note: Caution must be exercised when performing boundary scan test operations on a board designed for an PC7448, but populated with an PC7447 or earlier device. This is because in the PC7447 it is possible to drive the latches associated with the former 'no connect' pins in the PC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal PC7447 latches do not cause these pins to be driven during board testing.

For the PC7448, pins that were defined as the TEST[0:4] factory test signal group on the PC7447A and earlier devices have been assigned new functions. For most of these, the termination recommendations for the TEST[0:4] pins of the PC7447A are compatible with the PC7448 and will allow correct operation with no performance loss. The exception is BVSEL1 (TEST3 on the PC7447A and earlier devices), which may require a different termination depending which I/O voltage mode is desired; see Table 5-2 on page 12 for more information.

Note: This pinout is not compatible with the PC750, PC7400, or PC7410 360 BGA package

Table 7-1. Pinout Listing for the PC7448, 360 HiTCE Package

Signal Name	Pin Number	Active	I/O	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	(2)
$\overline{\text{AACK}}$	R1	Low	Input	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	(2)
$\overline{\text{ARTRY}}$	N2	Low	I/O	(3)
AV_{DD}	A8	–	Input	
$\overline{\text{BG}}$	M1	Low	Input	
$\overline{\text{BMODE0}}$	G9	Low	Input	(4)
$\overline{\text{BMODE1}}$	F8	Low	Input	(5)
$\overline{\text{BR}}$	D2	Low	Output	
BVSEL0	B7	High	Input	(1)(6)
BVSEL1	E10	High	Input	(1)(20)
$\overline{\text{CI}}$	J1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	

Table 7-1. Pinout Listing for the PC7448, 360 HiTCE Package (Continued)

Signal Name	Pin Number	Active	I/O	Notes
CLK_OUT	H2	High	Output	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	
$\overline{\text{DBG}}$	M2	Low	Input	
$\overline{\text{DFS2}}$	A12	Low	Input	(20)(21)
$\overline{\text{DFS4}}$	B6	Low	Input	(12)(20)(21)
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	
$\overline{\text{DRDY}}$	R3	Low	Output	(7)
DTI[0:3]	G1, K1, P1, N1	High	Input	(8)
EXT_QUAL	A11	High	Input	(9)
$\overline{\text{GBL}}$	E2	Low	I/O	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	–	–	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	–	–	(15)
GND_SENSE	G12, N13	–	–	(19)
$\overline{\text{HIT}}$	B2	Low	Output	(7)
$\overline{\text{HRESET}}$	D8	Low	Input	
$\overline{\text{INT}}$	D4	Low	Input	
L1_TSTCLK	G8	High	Input	(9)
L2_TSTCLK	B3	High	Input	(10)
$\overline{\text{LVRAM}}$	B10	–	–	(12)(20)(22)
NC (No Connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	–	–	(11)
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	(6)(12)
$\overline{\text{MCP}}$	C9	Low	Input	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	–	–	
OV_{DD}_SENSE	E18, G18	–	–	(16)
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	
PLL_CFG[5]	D10	High	Input	(9)(20)
$\overline{\text{PMON\_IN}}$	D9	Low	Input	(13)
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	
$\overline{\text{QACK}}$	G5	Low	Input	
$\overline{\text{QREQ}}$	P4	Low	Output	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	(3)
$\overline{\text{SMI}}$	F9	Low	Input	

Table 7-1. Pinout Listing for the PC7448, 360 HiTCE Package (Continued)

Signal Name	Pin Number	Active	I/O	Notes
$\overline{\text{SRESET}}$	A2	Low	Input	
SYSCLK	A10	–	Input	
$\overline{\text{TA}}$	K6	Low	Input	
TBEN	E1	High	Input	
$\overline{\text{TBST}}$	F11	Low	Output	
TCK	C6	High	Input	
TDI	B9	High	Input	(6)
TDO	A4	High	Output	
$\overline{\text{TEA}}$	L1	Low	Input	
TEMP_ANODE	N18	–	–	(17)
TEMP_CATHODE	N19	–	–	(17)
TMS	F1	High	Input	(6)
$\overline{\text{TRST}}$	A5	Low	Input	(6)(14)
$\overline{\text{TS}}$	L4	Low	I/O	(3)
TSIZ[0:2]	G6, F7, E7	High	Output	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	
$\overline{\text{WT}}$	D3	Low	Output	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	–	–	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	–	–	(15)
V_{DD}_SENSE	G13, N12	–	–	(18)

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, see Table 5-2 on page 12. If used, the pull-down resistor should be less than 250Ω because these settings may change in future products, it is recommended BVSEL[0:1] be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{IN} or supply voltages see Table 5-3 on page 12.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the PC7448 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the PC7448 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the PC7447 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.

14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the PC7447. See Section 9.3 "Connection Recommendations" on page 37, for more information.
16. These pins were OV_{DD} pins on the PC7447. These pins are internally connected to OV_{DD} and are intended to allow an external device to detect the I/O voltage level present inside the device package. If unused, they must be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.
20. These pins were in the TEST[0:4] factory test pin group on the PC7447A and PC7447. They have been assigned new functions on the PC7448.
21. These pins can be used to enable the supported dynamic frequency switching (DFS) modes via hardware. If both are pulled down, DFS mode is disabled completely and cannot be enabled via software. If unused, they should be pulled up to OV_{DD} to allow software control of DFS. See the PC7450 RISC Microprocessor Family Reference Manual for more information.
22. This pin is provided to allow operation of the L2 cache at low core voltages and is for factory use only. See the PC7450 RISC Microprocessor Family Reference Manual for more information.

8. Package Description

The following sections provide the package parameters and mechanical dimensions for the HiTCE package.

8.1 Package Parameters for the PC7448, 360 HiTCE BGA

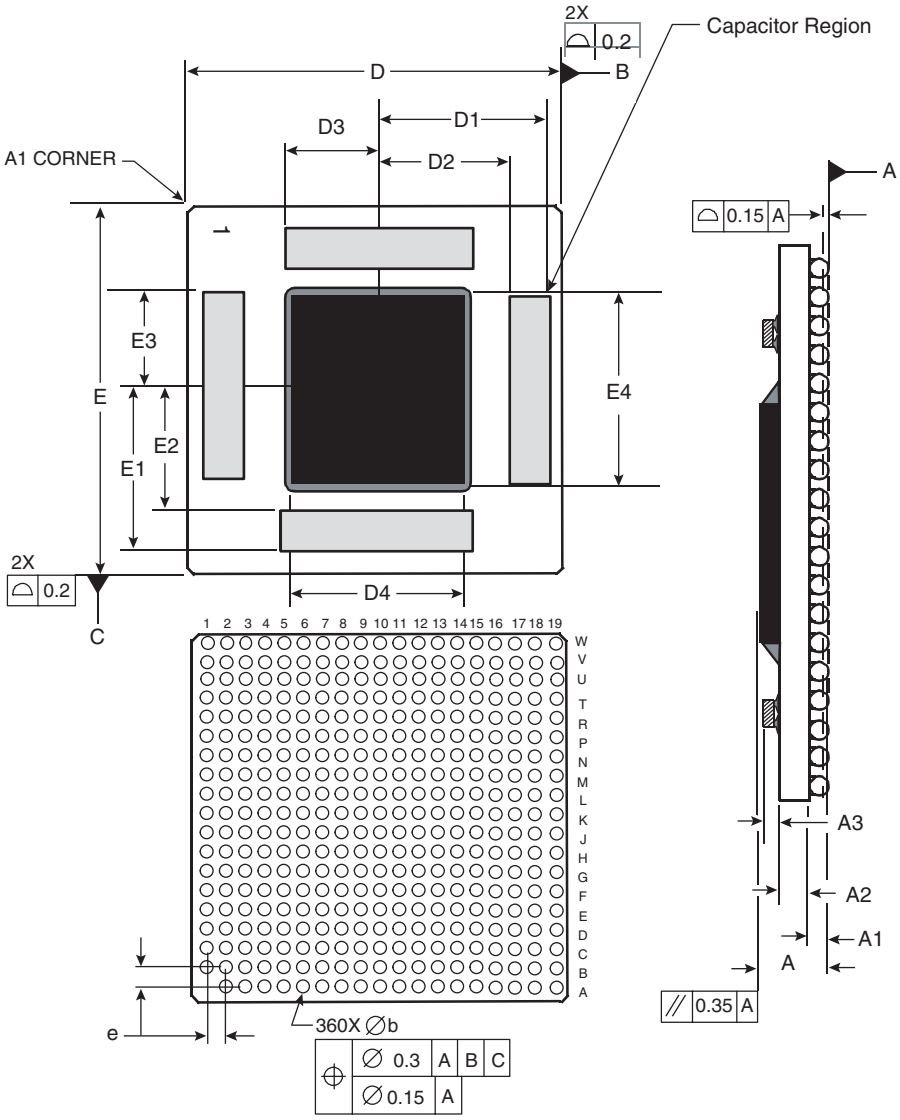
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HiTCE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/° C

8.2 Mechanical Dimensions for the PC7448, 360 HiTCE BGA

Figure 8-1 on page 28 provides the mechanical dimensions and bottom surface nomenclature for the PC7448, 360 HiTCE BGA package.

Figure 8-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7448, 360 HiTCE BGA Package



Notes:
1. Dimensioning and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.

	Millimeters	
Dim	Min	Max
A	2.32	2.80
A1	0.80	1
A2	0.70	0.90
A3	–	0.6
b	0.82	0.93
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	7.9	8.1

8.3 Package Parameters for the PC7448, 360 HiTCE LGA

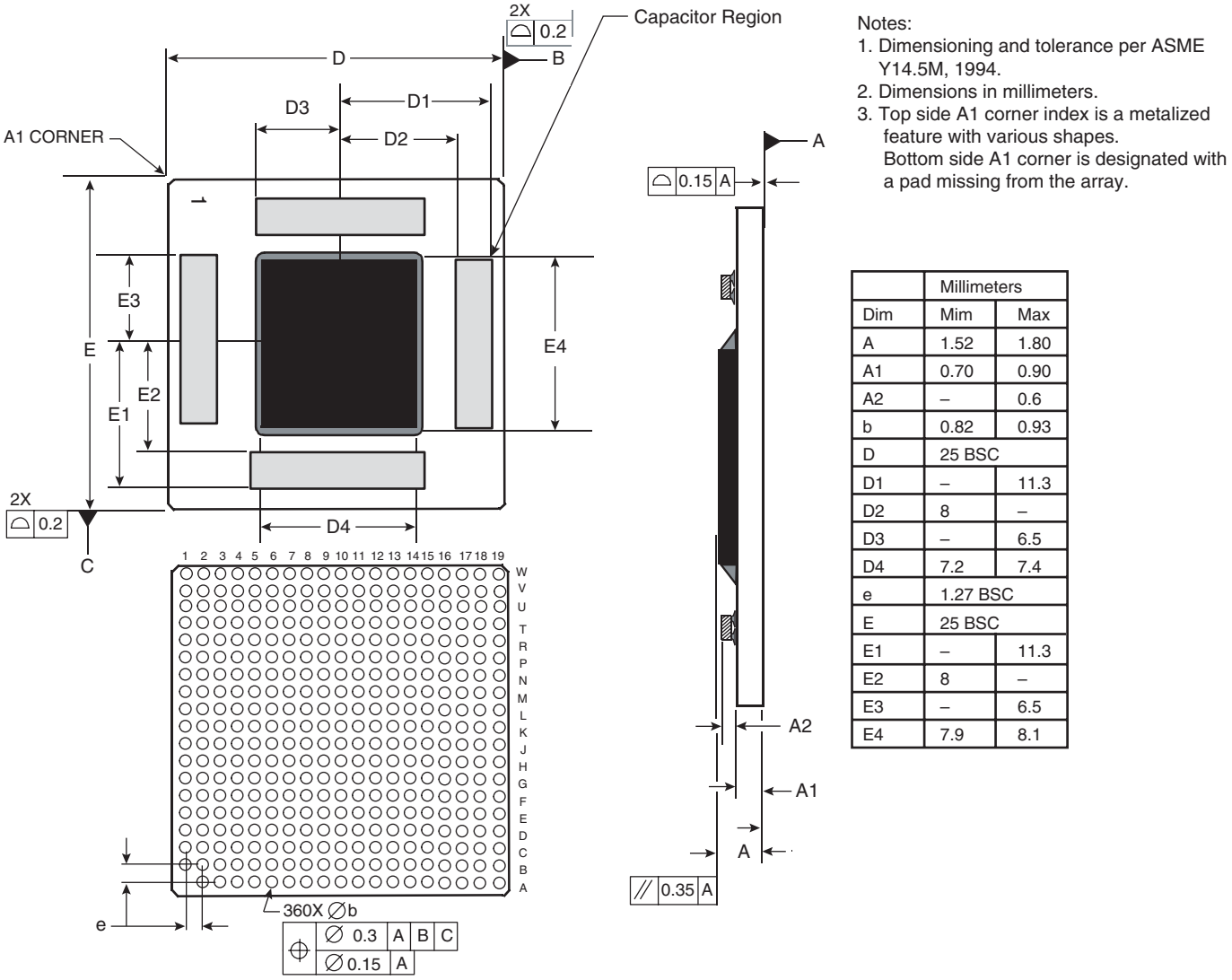
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 pin high coefficient of thermal expansion ceramic land grid array (HiTCE).

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.52 mm
Maximum module height	1.80 mm
Pad diameter	0.89 mm (35 mil)
Coefficient of thermal expansion	12.3 ppm/° C

8.4 Mechanical Dimensions for the PC7448, 360 HiTCE LGA

Figure 8-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7448, 360 HiTCE LGA package.

Figure 8-2. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7448, 360 HiTCE LGA Package



Notes:
1. Dimensioning and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a pad missing from the array.

	Millimeters	
Dim	Mim	Max
A	1.52	1.80
A1	0.70	0.90
A2	–	0.6
b	0.82	0.93
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	7.9	8.1

8.5 Package Parameters for the PC7448, 360 HiTCE RoHS-Compliant BGA

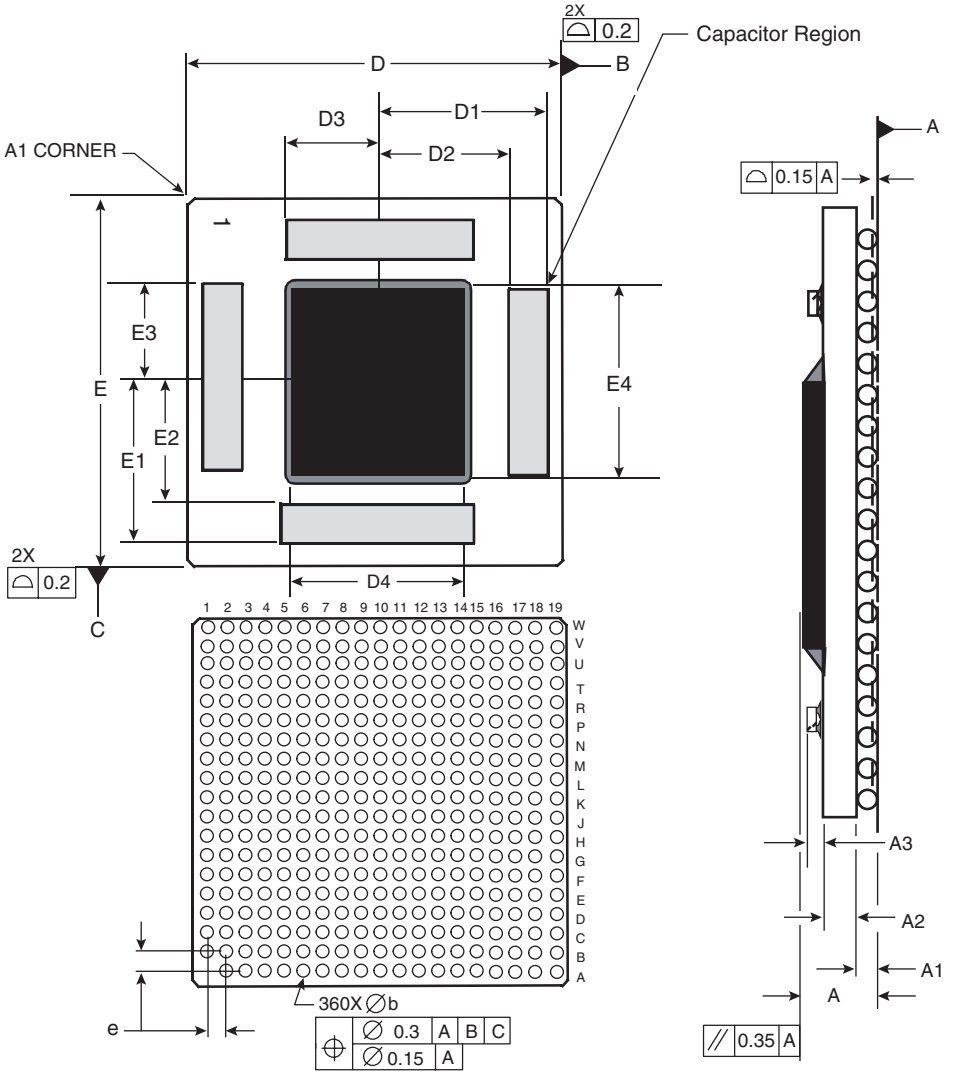
The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead high coefficient of thermal expansion ceramic ball grid array (HiTCE) with RoHS-compliant lead-free spheres.

Package outline	25 mm × 25 mm
Interconnects	360 (19 × 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.40 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/° C

8.6 Mechanical Dimensions for the PC7448, 360 HiTCE RoHS-Compliant BGA

Figure 8-1 on page 28 provides the mechanical dimensions and bottom surface nomenclature for the PC7448, 360 HiTCE BGA package with RoHS-compliant lead-free spheres.

Figure 8-3. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7448, 360 HiTCE RoHS-Compliant BGA Package



Notes:
1. Dimensioning and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
4. Dimension A1 represents the collapsed sphere diameter.

	Millimeters	
DIM	MIN	MAX
A	1.92	2.40
A1[4]	0.40	0.60
A2	0.70	0.90
A3	–	0.6
b	0.60	0.90
D	25 BSC	
D1	–	11.3
D2	8	–
D3	–	6.5
D4	7.2	7.4
e	1.27 BSC	
E	25 BSC	
E1	–	11.3
E2	8	–
E3	–	6.5
E4	7.9	8.1

9. System Design Information

This section provides system and thermal design requirements and recommendations for successful application of the PC7448.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the PC7448.

9.1.1 PLL Configuration

The PC7448 PLL is configured by the PLL_CFG[0:5] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC7448 is shown in Table 9-1. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with Table 5-7 on page 16. When enabled, Dynamic Frequency Switching (DFS) also affects the core frequency by halving or quartering the bus-to-core multiplier; see Section 9.7.5 ”Dynamic Frequency Switching (DFS)” on page 47, for more information. Note that when DFS is enabled the resulting core frequency must meet the adjusted minimum core frequency requirements (f_{core_DFS}) described in Table 5-7 on page 16. Note that the PLL_CFG[5] is currently used for factory test only and should be tied low, and that the PC7448 PLL configuration settings are compatible with the PC7447A PLL configuration settings when PLL_CFG[5] = 0.

Table 9-1. PC7448 Microprocessor PLL Configuration Example

	Example Core and VCO Frequency in MHz										
			Bus (SYSCLK) Frequency								
PLL_CFG[0:5]	Bus-to-Core Multiplier[5]	Core-to-VCO Multiplier[5]	33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
010000	2x	1x									
100000	3x	1x									600
101000	4x	1x								667	800
101100	5x	1x							667	835	1000
100100	5.5x	1x							733	919	1100
110100	6x	1x						600	800	1002	1200
010100	6.5x	1x						650	866	1086	1300
001000	7x	1x						700	931	1169	1400
000100	7.5x	1x					623	750	1000	1253	1500
110000	8x	1x				600	664	800	1064	1336	1600
011000	8.5x	1x				638	706	850	1131	1417	1700
011110	9x	1x			600	675	747	900	1197	1500	
011100	9.5x	1x			633	712	789	950	1264	1583	
101010	10x	1x			667	750	830	1000	1333	1667	
100010	10.5x	1x			700	938	872	1050	1397		
100110	11x	1x			733	825	913	1100	1467		
000000	11.5x	1x			766	863	955	1150	1533		

Table 9-1. PC7448 Microprocessor PLL Configuration Example (Continued)

PLL_CFG[0:5]	Example Core and VCO Frequency in MHz										
			Bus (SYSCLK) Frequency								
	Bus-to-Core Multiplier[5]	Core-to-VCO Multiplier[5]	33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz	200 MHz
101110	12x	1x		600	800	900	996	1200	1600		
111110	12.5x	1x		625	833	938	1038	1250	1667		
010110	13x	1x		650	865	975	1079	1300			
111000	13.5x	1x		675	900	1013	1121	1350			
110010	14x	1x		700	933	1050	1162	1400			
000110	15x	1x		750	1000	1125	1245	1500			
110110	16x	1x		800	1066	1200	1328	1600			
000010	17x	1x		850	1132	1275	1417	1700			
001010	18x	1x	600	900	1200	1350	1500				
001110	20x	1x	667	1000	1332	1500	1666				
010010	21x	1x	700	1050	1399	1575					
011010	24x	1x	800	1200	1600						
111010	28x	1x	933	1400							
001100	PLL bypass		PLL off, SYSCLK clocks core circuitry directly								
111100	PLL off		PLL off, no core clocking occurs								

Notes:
1. PLL_CFG[0:5] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC7448; see Section 5.4.1 ”Clock AC Specifications” on page 15, for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 5-8 on page 17). The result will be that the processor bus frequency will be one-half SYSCLK, while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7448 regardless of the SYSCLK input.
5. Applicable when DFS modes are disabled. These multipliers change when operating in a DFS mode.

9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5-7 on page 16 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the PC7448 input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns, and the PC7448 is compatible with spread spectrum sources if the recommendations listed in Table 9-2 are observed.

Table 9-2. Spread Spectrum Clock Source Recommendations

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	50	kHz	(1)
Frequency spread	–	1	%	(1)(2)

Notes: 1. Guaranteed by design

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5-7 on page 16.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 Power Supply Design and Sequencing

The following sections provide detailed information regarding power supply design for the PC7448.

9.2.1 Power Supply Sequencing

The PC7448 requires its power rails and clock to be applied in a specific sequence to ensure proper device operation and to prevent device damage. The power sequencing requirements are as follows:

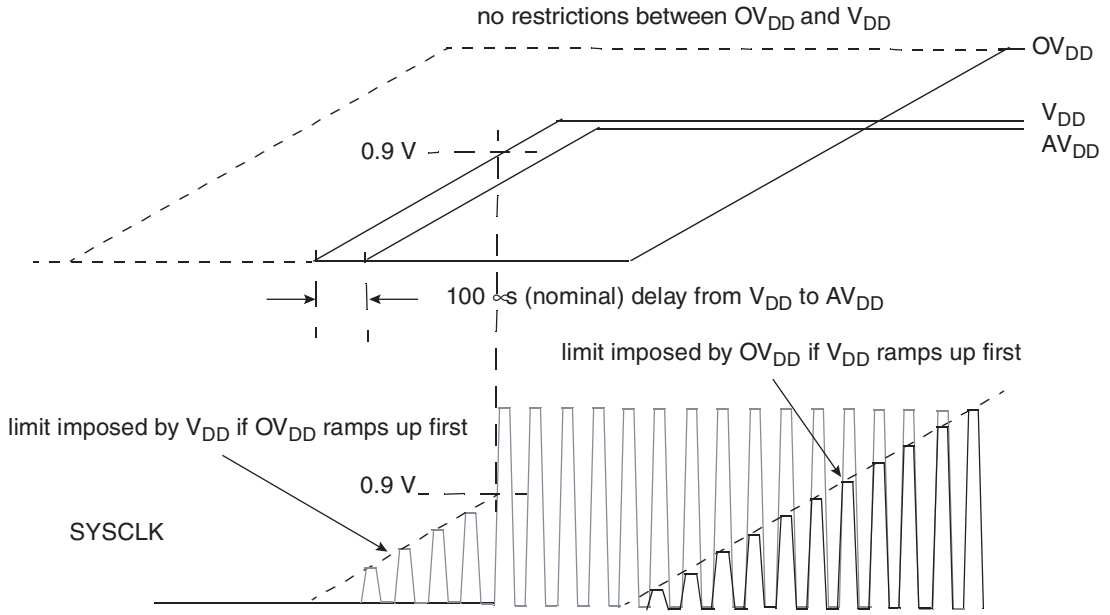
- AV_{DD} must be delayed with respect to V_{DD} by the RC time constant of the PLL filter circuit described in Section 9.2.2 "PLL Power Supply Filtering" on page 35. This time constant is nominally 100 µs.
- OV_{DD} may ramp anytime before or after V_{DD} and AV_{DD}.

Additionally, the following requirements exist regarding the application of SYSCLK:

- The voltage at the SYSCLK input must not exceed V_{DD} until V_{DD} has ramped to 0.9 V.
- The voltage at the SYSCLK input must not exceed OV_{DD} by more 20% during transients (see overshoot/undershoot specifications in Figure 5-1 on page 11) or 0.3V DC (see Table 5-3 on page 12) at any time.

These requirements are shown graphically in Figure 9-1 on page 34.

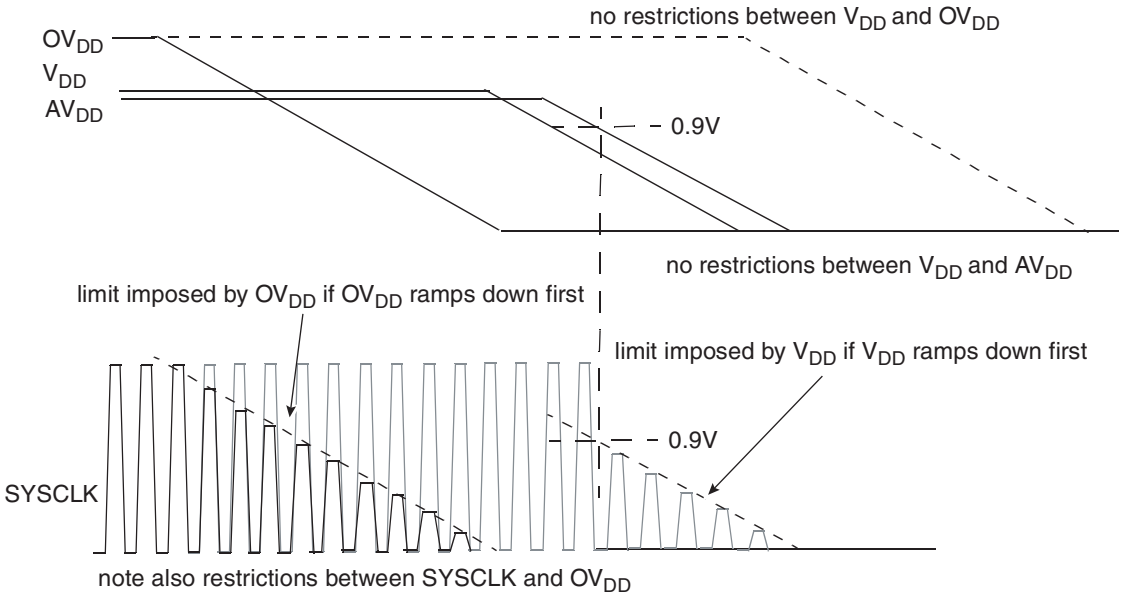
Figure 9-1. PC7448 Power up Sequencing Requirements



Certain stipulations also apply to the manner in which the power rails of the PC7448 power down, as follows:

- OV_{DD} may ramp down any time before V_{DD}. No restrictions apply in this case.
- If OV_{DD} ramps down with or after V_{DD}, then OV_{DD} must not exceed V_{DD} by more than 1.4V during power down (V_{DD} below 90% of its nominal value, see Table 5-3 on page 12), as shown in Figure 9-2.

Figure 9-2. PC7448 Power Down Sequencing Requirements



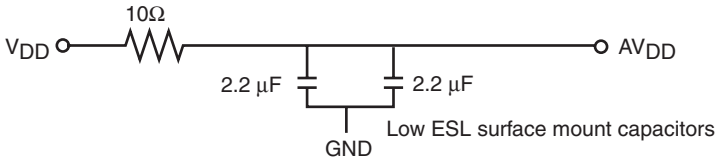
There is no requirement regarding AV_{DD} during power down, but it is recommended that AV_{DD} track V_{DD} within the RC time constant of the PLL filter circuit described in Section 9.2.2 ”PLL Power Supply Filtering” on page 35 (nominally 100 µs).

9.2.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PC7448 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. The circuit shown in Figure 9-3 using surface mount capacitors with minimum effective series inductance (ESL) is strongly recommended. In addition to filtering noise from the AV_{DD} input, it also provides the required delay between V_{DD} and AV_{DD} as described in Section 9.2.1 "Power Supply Sequencing" on page 33.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the device footprint.

Figure 9-3. PLL Power Supply Filter Circuit



9.2.3 Transient Specifications

The ensure the long-term reliability of the device, the PC7448 requires that transients on the core power rail (V_{DD}) be constrained. The recommended operating voltage specifications provided in Table 5-3 on page 12 are DC specifications. That is, the device may be operated continuously with V_{DD} within the specified range without adversely affecting the device's reliability. Excursions above the stated recommended operation range, including overshoot during power-up, can impact the long-term reliability of the device. Excursions are described by their amplitude and duration. Duration is defined as the time period during which the V_{DD} power plane, as measured at the VDD_SENSE pins, will be within a specific voltage range, expressed as percentage of the total time the device will be powered up over the device lifetime. In practice, the period over which transients are measured can be any arbitrary period of time that accurately represents the expected range of processor and system activity. The voltage ranges and durations for normal operation and transients are described in Table 9-3.

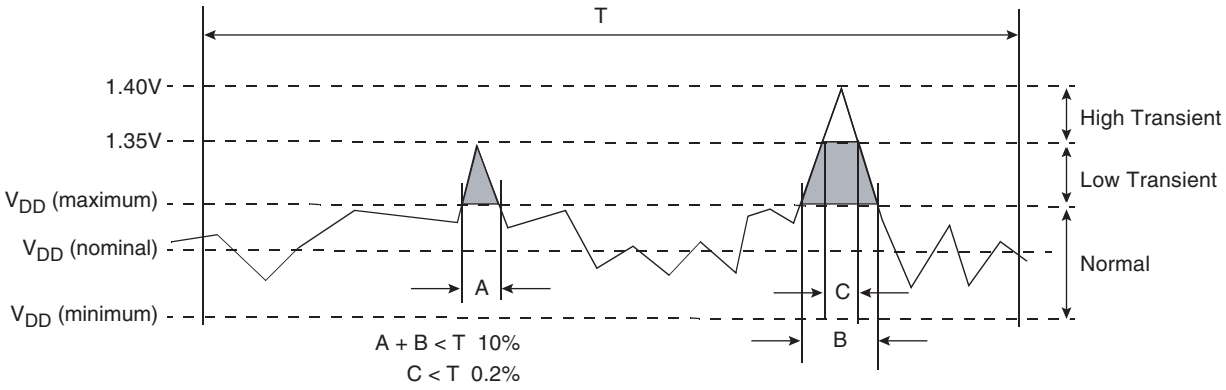
Table 9-3. V_{DD} Power Supply Transient Specificatins (At Recommended Operating Conditions, see Table 5-3 on page 12)

Voltage Region	Voltage Range (V)		Permitted Duration	Notes
	Min	Max		
Normal	V_{DD} minimum	V_{DD} maximum	100%	
Low Transient	V_{DD} maximum	1.35V	10%	
High Transient	1.35V	1.40V	0.2%	

Notes:
1. Permitted duration is defined as the percentage of the total time the device is powered on that the V_{DD} power supply voltage may exist within the specified voltage range.
2. See Table 5-3 on page 12 for nominal V_{DD} specifications.
3. To simplify measurement, excursions into the High Transient region are included in this duration.
4. Excursions above the absolute maximum rating of 1.4V are not permitted; see Table 5-1 on page 11.

Note that, to simplify transient measurements, the duration of the excursion into the High Transient region is also included in the Low Transient duration, so that only the time the voltage is above each threshold must be considered. Figure 9-4 on page 36 shows an example of measuring voltage transients.

Figure 9-4. Voltage Transient Example



9.2.4 Decoupling Recommendations

Due to the PC7448 dynamic power management feature, large address and data buses, and high operating frequencies, the PC7448 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7448 system, and the PC7448 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every 1–2 V_{DD} pins, and a similar or lesser amount for the OV_{DD} pins, placed as close as possible to the power pins of the PC7448. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

9.3 Connection Recommendations

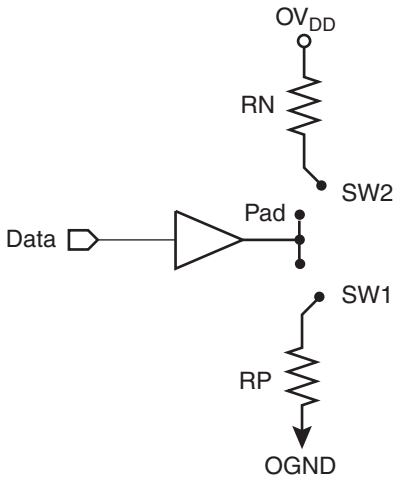
To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted, unused active low inputs should be tied to OV_{DD} and unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins in the PC7448. For backward compatibility with the PC7447, or for migrating a system originally designed for this device to the PC7448, the new power and ground signals (formerly NC, see Table 7-1 on page 24) may be left unconnected if the core frequency is 1 GHz or less. Operation above 1 GHz requires that these additional power and ground signals be connected, and it is strongly recommended that all new designs include the additional connections. See also Section 7. ”Pinout Listings” on page 24, for additional information.

9.4 Output Buffer DC Impedance

The PC7448 processor bus drivers are characterized over process, voltage, and temperature. To measure Z0, an external resistor is connected from the chip pad to OV_{DD} or GND. The value of each resistor is varied until the pad voltage is $OV_{DD}/2$. Figure 9-5 shows the driver impedance measurement.

Figure 9-5. Driver Impedance Measurement



The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and RN is trimmed until the voltage at the pad equals $OV_{DD}/2$. RN then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and RP is trimmed until the voltage at the pad equals $OV_{DD}/2$. RP then becomes the resistance of the pull-up devices. RP and RN are designed to be close to each other in value. Then, Z0 = (RP + RN)/2.

Table 9-4 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 9-4. Impedance Characteristics (At Recommended Operating Conditions, see Table 5-3 on page 12)

Impedance		Processor bus	L3 Bus	Unit
Z_0	Typical	33 – 42	34 – 42	Ω
	Maximum	31 – 51	32 – 44	Ω

9.5 Pull-up/Pull-down Resistor Requirements

The PC7448 requires high-resistive (weak: 4.7-KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7448 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, and $\overline{SHD1}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are $\overline{LSSD\_MODE}$ and TEST[0:3]; the pins that must be pulled down to GND are L1_TSTCLK and TEST[4]. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the PC7448 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 KΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

BVSEL0 and BVSEL1 should not be allowed to float, and should be configured either via pull-up or pull-down resistors or actively driven by external logic. If pull-down resistors are used to configure BVSEL0 or BVSEL1, the resistors should be less than 250Ω (see Table 7-1 on page 24). Because PLL_CFG[0:5] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise, or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7448 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7448 or by other receivers in the system. These signals can be pulled up through weak (10 KΩ) pull-up resistors by the system, address bus driven mode enabled (see the PC7450 RISC Microprocessor Family Users' Manual for more information on this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the PC7448 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{CI}$, $\overline{WT}$, and $\overline{GBL}$.

If address or data parity is not used by the system, and respective parity checking is disabled through HID1, the input receivers for those pins are disabled and do not require pull-up resistors, therefore they may be left unconnected by the system. If extended addressing is not used (HID0[XAEN] = 0), A[0:3] are unused and must be pulled low to GND through weak pull-down resistors; additionally, if address parity checking is enabled (HID1[EBA] = 1) and extended addressing is not used, AP[0] must be pulled up to OV_{DD} through a weak pull-up resistor. If the PC7448 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups or require that those signals be otherwise driven by the system during inactive periods. The data bus signals are D[0:63] and DP[0:7].

9.6 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 9-6 on page 40 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 9-6, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

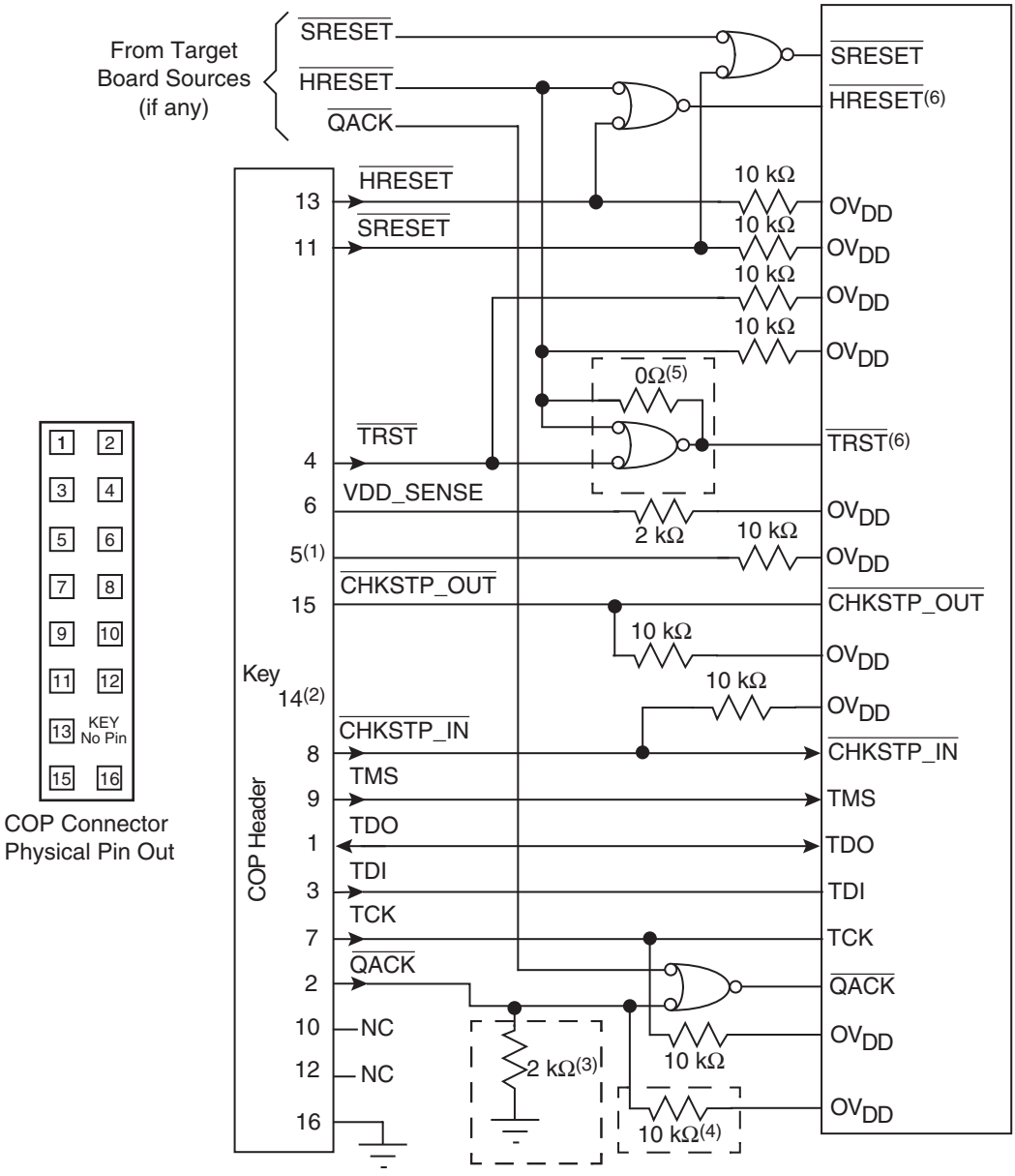
The COP header shown in Figure 9-6 adds many benefits: breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface and can be as inexpensive as an unpopulated footprint for a header to be added when needed.
The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 9-6; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 9-6 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 9-6 is usually connected to the PCI bridge chip in a system and is an input to the PC7448 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the PC7448 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal.

Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the PCI bridge.

Figure 9-6. JTAG Interface Connection



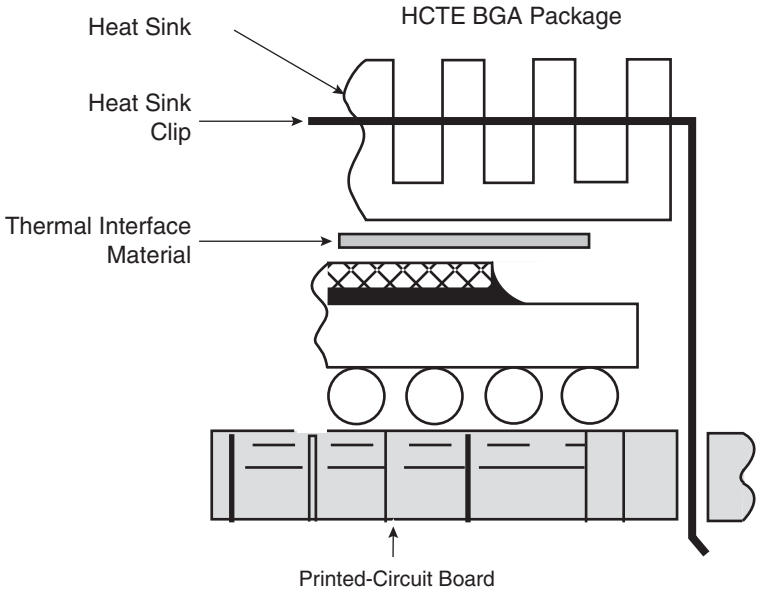
Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7448. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively negate $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

9.7 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HiTCE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design, the heat sink, airflow, and thermal interface material. The PC7448 implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.7.5.1 ”Power Consumption with DFS Enabled” on page 47, for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.7.4 ”Temperature Diode” on page 46, for more information.

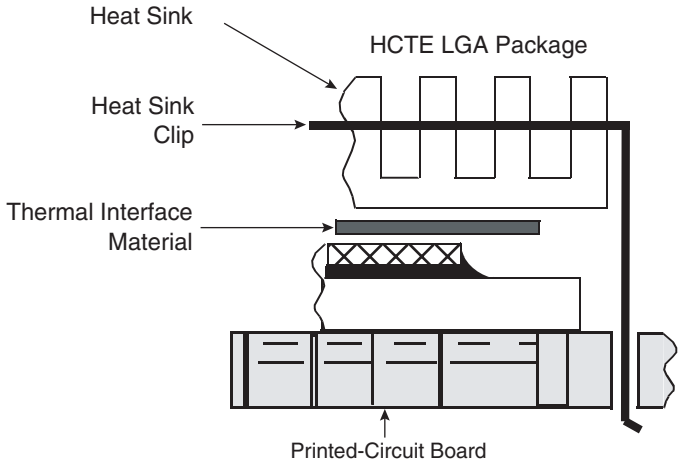
To reduce the die-junction temperature, heat sinks may be attached to the package by several methods, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 9-7); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds.

Figure 9-7. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options



Note: A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board.. A through-hole solution is recommended, as shown in Figure 9-8 below.

Figure 9-8. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options



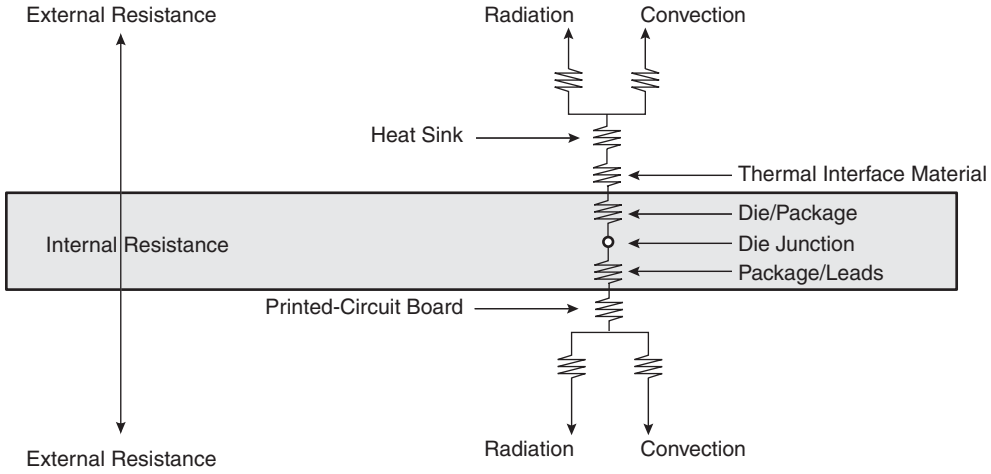
9.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5-4 on page 13, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-ball thermal resistance

Figure 9-5 on page 37 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 9-9. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note the internal versus external package resistance.

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and, finally, to the heat sink, where it is removed by forced-air convection.

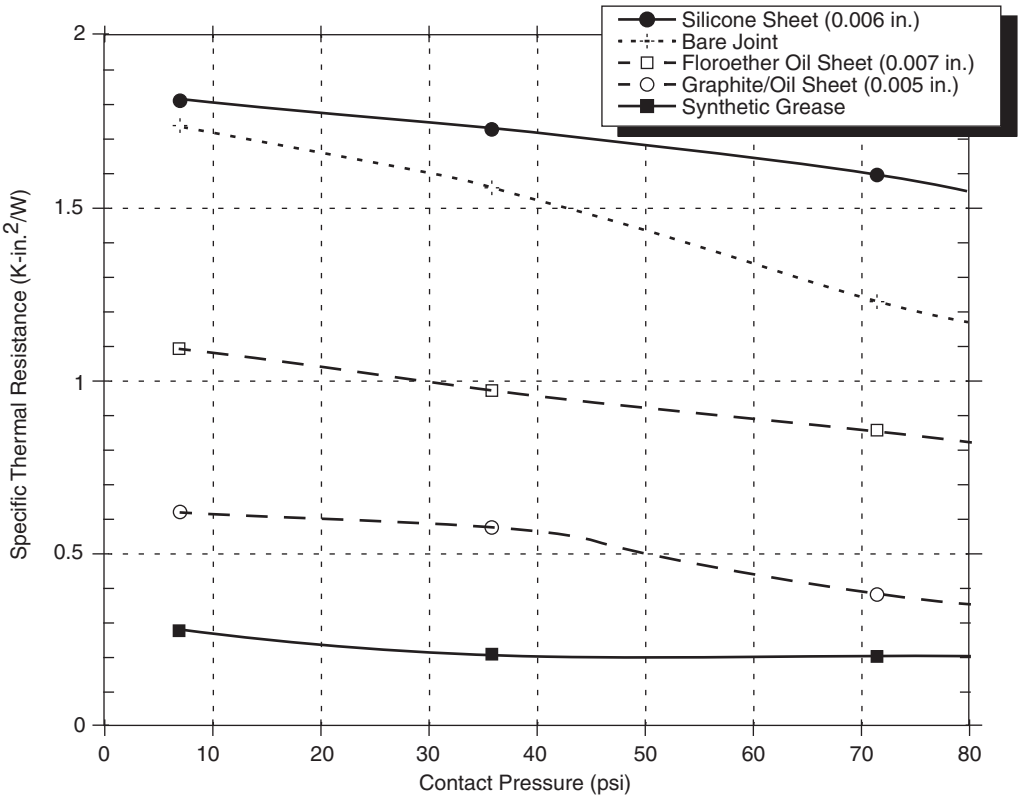
Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

9.7.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 9-10 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 9-7 on page 41). Therefore, synthetic grease offers the best thermal performance due to the low interface pressure and is recommended due to the high power dissipation of the PC7448. Of course, the selection of any thermal interface material depends on many factors, thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

Figure 9-10. Thermal Performance of Select Thermal Interface Material



The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements.

There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 800-347-4572

18930 West 78th St.

Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. 781-935-4850

77 Dragon Ct.

Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481

Corporate Center

P.O. Box 994.

Midland, MI 48686-0994
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674

10028 S. 51st St.

Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050

4707 Detroit Ave.

Cleveland, OH 44102
Internet: www.thermagon.com

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.7.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in Table 5-3 on page 12. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40° C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10° C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.1° C/W. For example, assuming a T_i of 30° C, a T_r of 5° C, an HiTCE package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 21W, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30° C + 5° C + (0.1° C/W + 1.1° C/W + \theta_{sa}) \times 25.6$

For this example, a $R_{\theta sa}$ value of 1.53° C/W or less is required to maintain the die junction temperature below the maximum value of Table 5-3 on page 12.

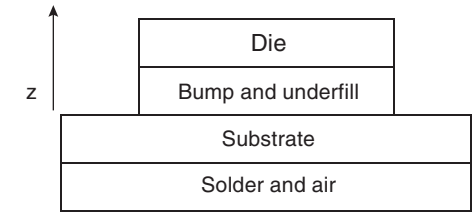
Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

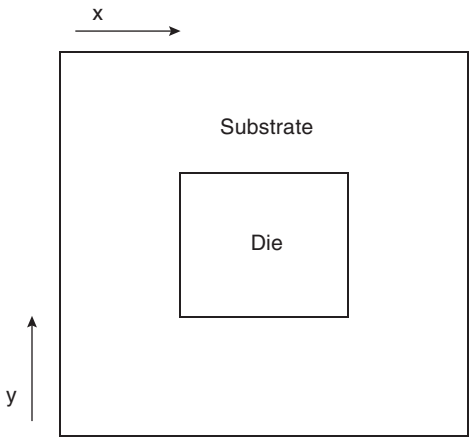
For system thermal modeling, the PC7448 thermal model is shown in Figure 9-11 on page 46. Four volumes represent this device. Two of the volumes, solder ball-air and substrate, are modeled using the package outline size of the package.The other two, die and bump-underfill, have the same size as the die. The silicon die should be modeled 8.0 × 7.3 × 0.86 mm^3 with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 8.0 × 7.3 × 0.07 mm^3 collapsed in the z-direction with a thermal conductivity of 5.0 W/(m • K) in the z-direction. The substrate volume is 25 × 25 × 1.14 mm^3 and has 9.9 W/(m • K) isotropic conductivity in the xy-plane and 2.95 W/(m • K) in the direction of the z-axis. The solder ball and air layer are modeled with the same horizontal dimensions as the substrate and is 0.8 mm thick. For the LGA package the solder and air layer is 0.1 mm thick, but the material properties are the same. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 11.2 W/(m • K) in the direction of the z-axis.

Figure 9-11. Recommended Thermal Model of PC7448

Conductivity	Value	Unit
Die (8.0 x 7.3 x 0.86 mm^3)		
Silicon	Temperature-dependent	W/(m • K)
Bump and underfill (8.0 x 7.3 x 0.07 mm^3)		
k_z	5.0	W/(m • K)
Substrate (25 x 25 x 1.14 mm^3)		
k_x	9.9	W/(m • K)
k_y	9.9	
k_z	2.95	
Solder ball and air (25 x 25 x 0.8 mm^3)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	11.2	



Side view of model (not to scale)



Top view of model (not to scale)

9.7.4 Temperature Diode

The PC7448 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each PC7448's internal diode.

The following are the specifications of the PC7448 on-board temperature diode:

$V_f > 0.40V$

$V_f < 0.90V$

Operating range 2 - 300 µA

Diode leakage < 10 nA at 125° C

Ideality factor over 5 µA – 150 µA at 60° C: n = 1.0275 ± 0.9%

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fW} = I_s\left[e^{\frac{qV_f}{nKT}} - 1\right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L}\right] - 1$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6×10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38×10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$V_H - V_L = 1.986 \times 10^{-4} \times nT$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1{,}986 \times 10^{-4}}$$

9.7.5 Dynamic Frequency Switching (DFS)

The DFS feature in the PC7448 adds the ability to divide the processor-to-system bus ratio by two or four during normal functional operation. Divide-by-two mode is enabled by setting the HID1[DFS2] bit in software or by asserting the $\overline{\text{DFS2}}$ pin via hardware. The PC7448 can be returned for full speed by clearing HID1[DFS2] or negating $\overline{\text{DFS2}}$. Similarly, divide-by-four mode is enabled by setting HID1[DFS4] in software or by asserting the $\overline{\text{DFS4}}$ pin. In all cases, the frequency change occurs in 1 clock cycle and no idle waiting period is required to switch between modes. Note that asserting either $\overline{\text{DFS2}}$ or $\overline{\text{DFS4}}$ overrides software control of DFS, and that asserting both $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ disables DFS completely, including software control. Additional information regarding DFS can be found in the PC7450 RISC Microprocessor Family Reference Manual. Note that minimum core frequency requirements must be observed when enabling DFS, and the resulting core frequency must meet the requirements for f_{CORE_DFS} given in Table 5-7 on page 16.

9.7.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 5-6 on page 14)

P_{DS} = Deep sleep mode power consumption (see Table 5-6 on page 14)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.7.5.2 *Bus-to-Core Multiplier Constraints with DFS*

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:5] during hard reset. The complete listing is shown in Table 9-5.

Table 9-5. Valid divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 9-1 on page 31)	Bus-to-Core Multiplier with HID1[DFS2] = 1 or $\overline{\text{DFS2}}$ = 0 (÷2)	Bus-to-Core Multiplier with HID1[DFS4] = 1 or $\overline{\text{DFS4}}$ = 0 (÷4)
2x	N/A	N/A
3x	N/A	N/A
4x	2x	N/A
5x	2.5x	N/A
5.5x	2.75x	N/A
6x	3x	N/A
6.5x	3.25x	N/A
7x	3.5x	N/A
7.5x	3.75x	N/A
8x	4x	2x
8.5x	4.25x	N/A
9x	4.5x	2.25x
9.5x	4.75x	N/A
10x	5x	2.5x
10.5x	5.25x	N/A
11x	5.5x	2.75x
11.5x	5.75x	N/A
12x	6x	3x
12.5x	6.25x	N/A
13x	6.5x	3.25x
13.5x	6.75x	N/A
14x	7x	3.5x
15x	7.5x	3.75x
16x	8x	4x
17x	8.5x	4.25x
18x	9x	4.5x

Table 9-5. Valid divide Ratio Configurations (Continued)

Bus-to-Core Multiplier Configured by PLL_CFG[0:5] (see Table 9-1 on page 31)	Bus-to-Core Multiplier with HID1[DFS2] = 1 or $\overline{DFS2}$ = 0 (÷2)	Bus-to-Core Multiplier with HID1[DFS4] = 1 or $\overline{DFS4}$ = 0 (÷4)
20x	10x	5x
21x	10.5x	5.25x
24x	12x	6x
28x	14x	7x

9.7.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 5-7 on page 16. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{CORE}.

10. Ordering Information

xx 7448 y xxx nnnn N x

Product Code (1)	Part Identifier	Temperature Range (1)	Package (1)	Processor Frequency (1)	Application Modifier	Revision Level (1)
PC(X) (2)	7448	V: T_C = -40˚C, T_J = +110˚C M: T_C = -55˚C, T_J = +125˚C	GH: Hi-TCE CBGA LH: Hi-TCE LGA SH: RoHS BGA	1000 MHz	1,0V ± 50 mV	D: 2.2 :PVR = 8004_0202
				1250 MHz	1,1V ± 50 mV	
				1267 MHz	1,05V ± 50 mV	

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

11. Definitions

11.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

12. Document Revision History

Table 12-1 provides a revision history for this hardware specification.

Table 12-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	12/08	Page 6: “Parity support on cache” replaced by “Parity support on L1 and L2 cache and L2 Tags”.
D	12/07	Add 1267 MHz parts.
C	08/07	"Preliminary" status removed from this datasheet consecutive to product qualification completion.
B	02/07	Name change from Atmel to e2v. On first page: modifying Typical/Power consumption and maximum frequency. Table 4-1 on page 10 : removed HiTCE in core power supply at 1000 MHz Table 5-3 on page 12 : change operating temperature to T_C = -55 ; T_J = +125 Table 5-6 on page 14 note 3 : change temperature to 125° C Ordering information : - change processor frequency - associated V_{DD} level - Added rev D parts
A	10/05	Initial revision.

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