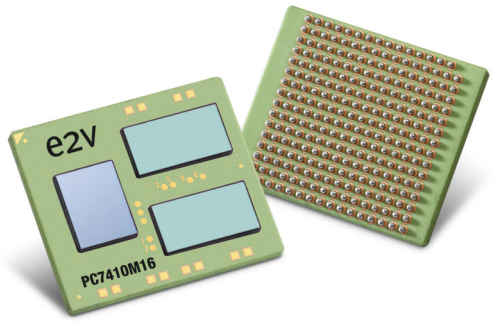
PC7410M16
RISC Microprocessor Multichip Package

Datasheet - *Preliminary Specification*

Features

- **PC7410 RISC Microprocessor**
- **Dedicated 2 MB SSRAM L2 Cache, Configured as 256Kx72**
- **21 mm x 25 mm, 255 Ceramic Ball Grid Array**
- **Maximum Core Frequency = 400 MHz**
- **Maximum L2 Cache Frequency = 200 MHz**
- **Maximum 60x Bus Frequency = 100 MHz**



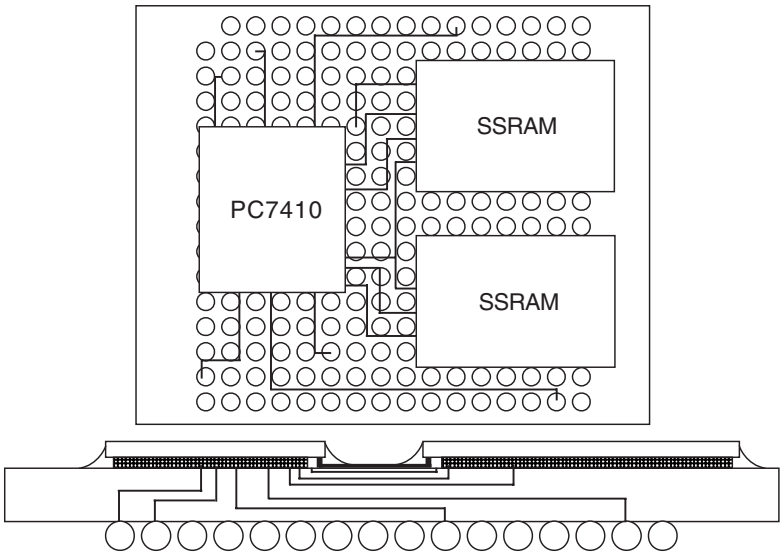
Description

The PC7410M16 multichip package is targeted for high performance, space sensitive, low power systems and supports the following power management features: doze, nap, sleep and dynamic power management.

The PC7410M16 is offered in industrial and military temperature ranges and is well suited for embedded applications.

Screening

- **CBGA Upscreening Based on e2v Standards**
- **Full Military Temperature Range (T_J = -55°C, +125°C), Industrial Temperature Range (T_J = -40°C, +110°C)**



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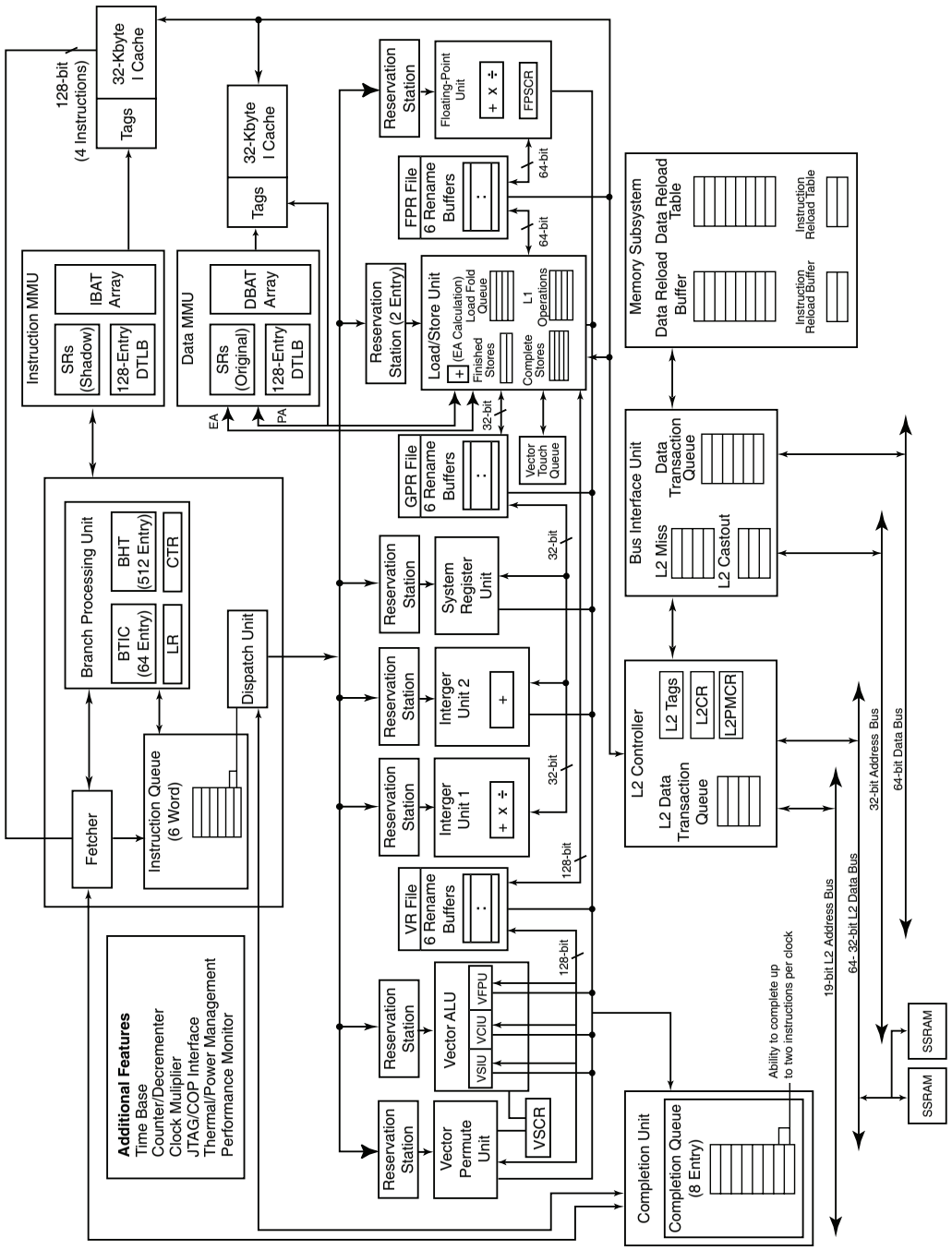
1. Block Diagram

Figure 1-1. PC7410M16 Microprocessor Block Diagram



2. Overview

This section summarizes features of the PC7410M16's implementation of the PowerPC architecture. Major features of the PC7410M16 are as follows:

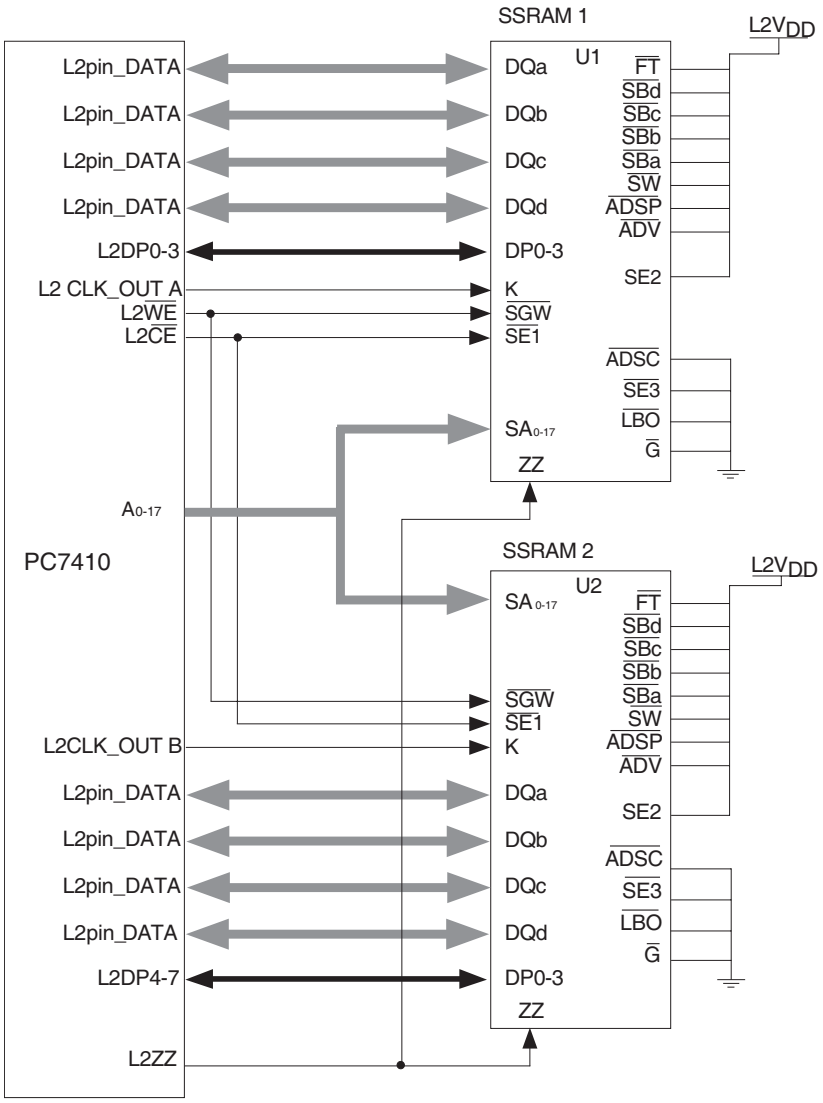
- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec® permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 8-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed-point Units (FXUs) that Share 32 GPRs for Integer Operands
  - Fixed-point unit 1 (FXU1) – multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2) – shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage Floating-point Unit and a 32-entry FPR File
  - Support for IEEE®-754 standard single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single or double precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions

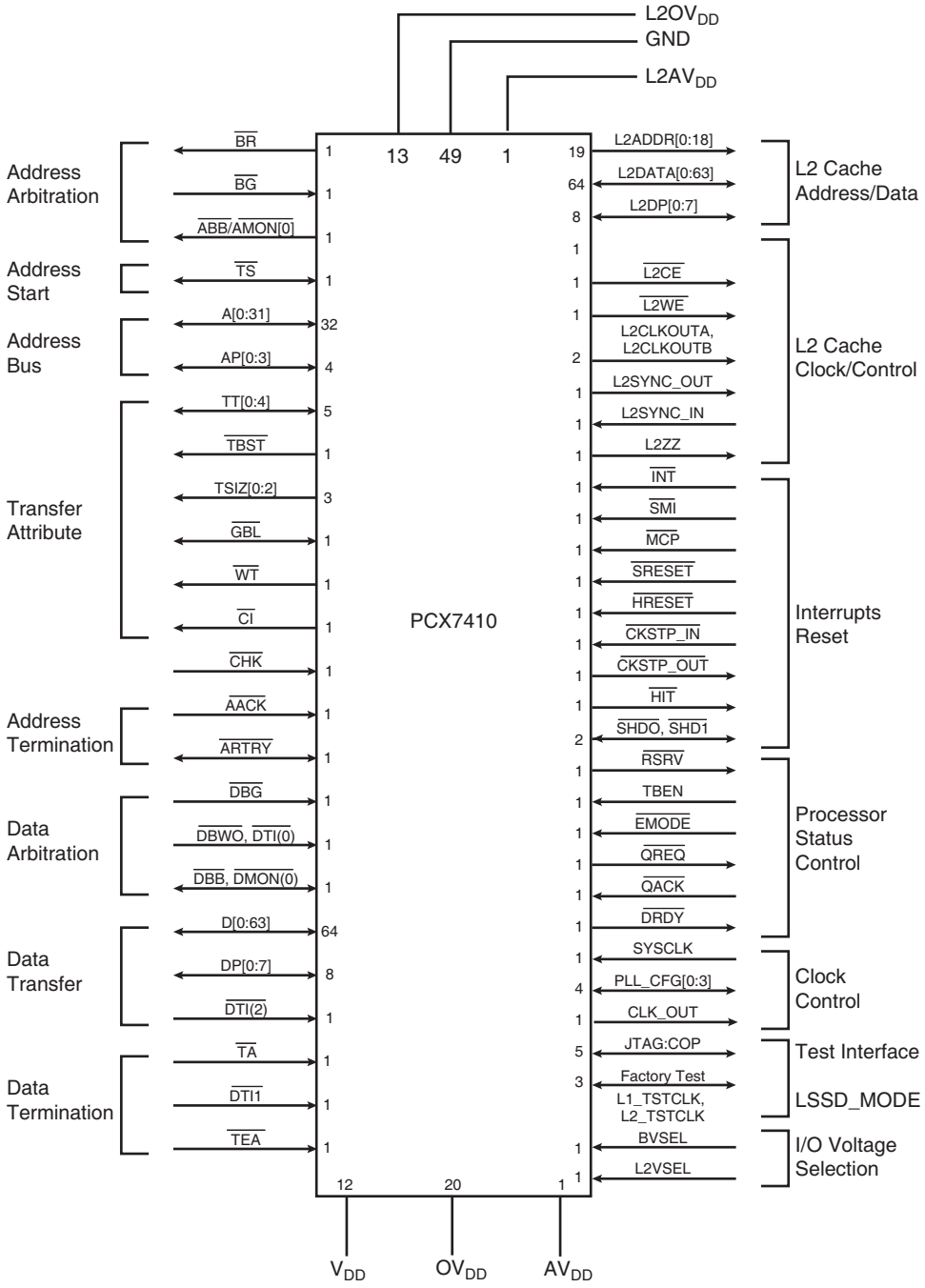
- AltiVec Unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit
  - Contains its own 32-entry 128-bit vector register file (VRF) with six renames
  - The vector ALU unit is further sub-divided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU) and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/Store Unit
  - One-cycle load or store cache access (byte, half-word, word, double-word)
  - Two-cycle load latency with one-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) Cache Structure
  - 32K 32-byte line, 8-way set associative instruction cache (iL1)
  - 32K 32-byte line, 8-way set associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Non-blocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to four petabytes (2^{52}) of virtual memory
  - Real memory support for up to four gigabytes (2^{32}) of physical memory

  - Snooped and invalidated for TLBI instructions
- Efficient Data Flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2 and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits per cycle to/from the VRF
  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s
  - Up to eight outstanding out-of-order cache misses between dL1 and L2/bus
  - Up to seven outstanding out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (i.e., address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - Two-entry finished store queue and four-entry completed store queue between load/store unit and dL1
  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, etc.) from dL1 and L2
- Bus Interface
  - MPX bus extension to 60X processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 9x supported
  - Selectable interface voltages of 1.8V, 2.5V and 3.3V
- Power Management
  - Low-power design with thermal requirements very similar to PC740 and PC750
  - Low voltage 1.8V processor core
  - Selectable interface voltages of 1.8V can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST) – factory test only
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and Serviceability
  - Parity checking on 60x and L2 cache buses

3. Signal Description

Figure 3-1. PC7410M16 Microprocessor Signal Groups





4. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7410M16 in compliance with e2v standard screening.

5. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

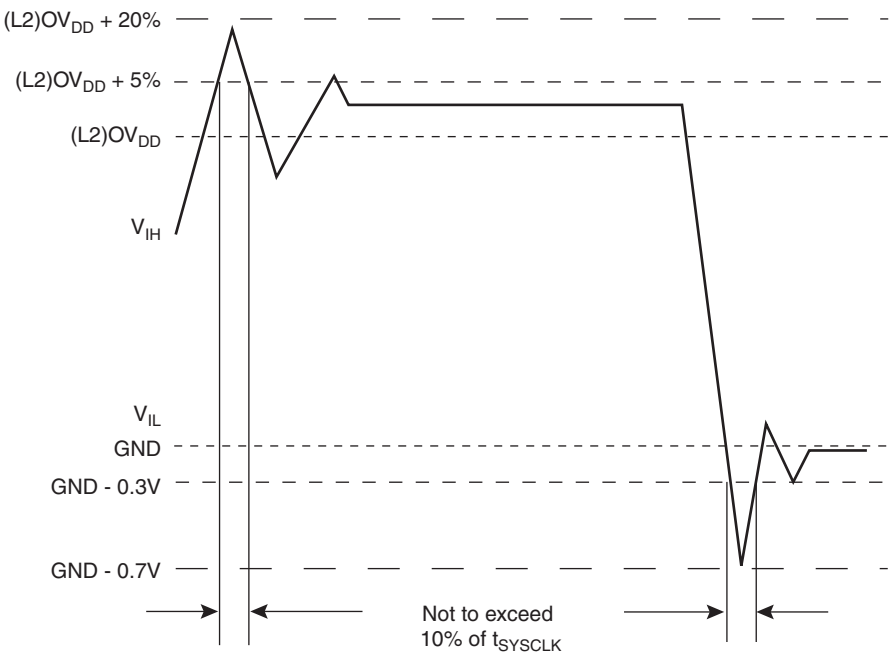
Depending on the package, the terminal connections are as shown in Table 8-1, Section "Recommended Operating Conditions" on page 10 and Figure 3-1.

5.1.2 Absolute Maximum Ratings(1)

Symbol	Characteristic		Value	Unit	Notes
V_{DD}	Core supply voltage		-0.3 to 2.1	V	(4)
AV_{DD}	PLL supply voltage		-0.3 to 2.1	V	(4)
$L2AV_{DD}$	L2 DLL supply voltage		-0.3 to 2.1	V	(4)
OV_{DD}	60x bus supply voltage		-0.3 to 3.465	V	(3)
$L2OV_{DD}$	L2 bus supply voltage		-0.3 to 2.6	V	(3)
$L2V_{DD}$	L2 supply voltage		-0.3 to 4.6	V	(5)
V_{IN}	Input supply	Processor Bus	-0.3 to OV_{DD} + 0,2	V	(2)
V_{IN}		L2 bus	-0.3 to $L2OV_{DD}$ + 0,2	V	(2)
V_{IN}		JTAG Signals	-0.3 to OV_{DD} + 0,2	V	(2)
T_{STG}	Storage temperature range		-55 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Operating Conditions table. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: Vin must not exceed OV_{DD} by more than 0.2V at any time including during power-on reset.
3. Caution: $OV_{DD}/L2OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0V at any time including during power-on reset.
4. Caution: $V_{DD}/AV_{DD}D/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V at any time including during power-on reset.
5. $L2OV_{DD}$ should never exceed $L2V_{DD}$

Figure 5-1. Overshoot/Undershoot Voltage



The PC7410M16 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7410M16 “core” voltage must always be provided at nominal voltage (see “Recommended Operating Conditions” on page 10 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 5-1. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 5-1. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L2VSEL Signal	L2 Bus Input Threshold is Relative to:
0(1)	1.8V	0	1.8
$\overline{\text{HRESET}}$(1) (2)	2.5V	$\overline{\text{HRESET}}$	2.5
1(1)(3)	3.3V	1	2.5
HRESET	3.3V	HRESET	Not supported

Notes:
1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. To select the 2.5V threshold option, L2VSEL/BVSEL should be tied to $\overline{\text{HRESET}}$ so that the two signals change state together. This is the preferred method for selecting this mode operation.
3. Default voltage setting if left unconnected (internal pull-up). To overcome the internal pull up resistance, a pull down resistance less than 250Ω should be used.

5.1.3 Recommended Operating Conditions

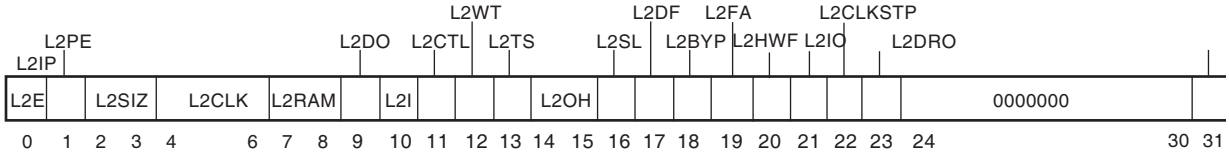
Symbol	Characteristic		Recommended Value	Unit
V_{DD}	Core supply voltage		1.8 ± 100 mV	V
AV_{DD}	PLL supply voltage		1.8 ± 100 mV	V
$L2AV_{DD}$	L2 DLL supply voltage		1.8 ± 100 mV	V
OV_{DD}	Processor bus supply voltage	BVSEL = 0	1.8 ± 100 mV	V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$	2.5 ± 100 mV	V
OV_{DD}		BVSEL = 1 or = HRESET	3.3 ± 165 mV	V
$L2OV_{DD}$	L2 bus supply voltage	L2VSEL = 1 or L2VSEL = HRESET	2.5 ± 100 mV	V
$L2V_{DD}$	Memory core supply voltage		3.3V ± 165mV	V
V_{IN}	Input voltage	Processor bus and JTAG Signals	GND to OV_{DD}	V

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

5.2 L2 Cache Control Register (L2CR)

The L2 cache control register, shown in Figure 5-2, is a supervisor-level, implementation-specific SPR used to configure and operate the L2 cache. It is cleared by hard reset or power-on reset.

Figure 5-2. L2 Cache Control Register (L2CR)



The L2CR bits are described in Table 5-2.

Table 5-2. L2CR Bit Settings

Bit	Name	Function
0	L2E	L2 enable. Enables L2 cache operation (including snooping) starting with the next transaction the L2 cache unit receives. Before enabling the L2 cache, the L2 clock must be configured through L2CR[2CLK], and the L2 DLL must stabilize. All other L2CR bits must be set appropriately. The L2 cache may need to be invalidated globally.
1	L2PE	L2 data parity checking enable. Enables parity generation and checking for the L2 data RAM interface. When disabled, generated parity is always zeros. L2 Parity is supported by PC7410M16, but is dependent on application.
2-3	L2SIZ	L2 size – Should be set according to the size of the private memory setting. Total SRAM space is 2M bytes (256Kx72). See L2 cache/private memory configurations table in Freescale™ User's Manual.

Table 5-2. L2CR Bit Settings (Continued)

Bit	Name	Function
4-6	L2CLK	L2 clock ratio (core-to-L2 frequency divider). Specifies the clock divider ratio based from the core clock frequency that the L2 data RAM interface is to operate at. When these bits are cleared, the L2 clock is stopped and the on-chip DLL for the L2 interface is disabled. For nonzero values, the processor generates the L2 clock and the on-chip DLL is enabled. After the L2 clock ratio is chosen, the DLL must stabilize before the L2 interface can be enabled. The resulting L2 clock frequency cannot be slower than the clock frequency of the 60x bus interface. 000 L2 clock and DLL disabled 001 ÷ 1 010 ÷ 1.5 011 ÷ 3.5 **100 ÷ 2** 101 ÷ 2.5 110 ÷ 3 111 ÷ 4
7-8	L2RAM	L2 RAM type – Configures the L2 RAM interface for the type of synchronous SRAMs used: • Pipelined (register-register) synchronous burst SRAMs that clock addresses in and clock data out The 7410 does not burst data into the L2 cache, it generates an address for each access. **10 Pipelined (register-register) synchronous burst SRAM - Setting for PC7410M16**
9	L2DO	L2 data only. Setting this bit enables Údata-only operation in the L2 cache. When this bit is set, only transactions from the L1 data cache can be cached in the L2 cache. L1 instruction cache operations will be serviced for instruction addresses already in the L2 cache; however, the L2 cache will not be reloaded for L1 instruction cache misses. Note that setting both L2DO and L2IO effectively locks the L2 cache.
10	L2I	L2 global invalidate. Setting L2I invalidates the L2 cache globally by clearing the L2 status bits. This bit must not be set while the L2 cache is enabled. See Freescale's User manual for L2 Invalidation procedure.
11	L2CTL	L2 RAM control (ZZ enable). Setting L2CTL enables the automatic operation of the L2ZZ (low-power mode) signal for cache RAMs. Sleep mode is supported by the **PC7410M16**. While L2CTL is asserted, L2ZZ asserts automatically when the device enters nap or sleep mode and negates automatically when the device exits nap or sleep mode. This bit should not be set when the device is in nap mode and snooping is to be performed through deassertion of QACK.
12	L2WT	L2 write-through. Setting L2WT selects write-through mode (rather than the default write-back mode) so all writes to the L2 cache also write through to the system bus. For these writes, the L2 cache entry is always marked as clean (value unmodified) rather than dirty (value modified). This bit must never be asserted after the L2 cache has been enabled as previously-modified lines can get remarked as clean (value unmodified) during normal operation.
13	L2TS	L2 test support. Setting L2TS causes cache block pushes from the L1 data cache that result from **dcbf** and **dcbst** instructions to be written only into the L2 cache and marked valid, rather than being written only to the system bus and marked invalid in the L2 cache in case of hit. This bit allows a **dcbz**/**dcbf** instruction sequence to be used with the L1 cache enabled to easily initialize the L2 cache with any address and data information. This bit also keeps **dcbz** instructions from being broadcast on the system and single-beat cacheable store misses in the L2 from being written to the system bus.
14-15	L2OH	L2 output hold. These bits configure output hold time for address, data, and control signals driven to the L2 data RAMs. **01: 0.8 ms Hold Time - Setting for PC7410M16**
16	L2SL	L2 DLL slow. Setting L2SL increases the delay of each tap of the DLL delay line. It is intended to increase the delay through the DLL to accommodate slower L2 RAM bus frequencies. **0: Setting for PC7410M16** because L2 RAM interface is operated above 100 MHz.

Table 5-2. L2CR Bit Settings (Continued)

Bit	Name	Function
17	L2DF	L2 differential clock. This mode supports the differential clock requirements of late-write SRAMs. **0: Setting for PC7410M16** because late-write SRAMs are not used.
18	L2BYP	L2 DLL bypass is reserved. **0: Setting for PC7410M16**
19	L2FA	L2 flush assist (for software flush). When this bit is negated, all lines castout from the dL1 which have a state of CDMRSV=01xxx1 (i.e. C-bit negated), will not allocate in the L2 if they miss. Asserting this bit forces every castout from the dL1 to allocate an entry in the L2 if that castout misses in the L2 regardless of the state of the C-bit. The L2FA bit must be set and the L2IO bit must be cleared in order to use the software flush algorithm.
20	L2HWF	L2 hardware flush. When the processor detects the value of L2HWF set to 1, the L2 will begin a hardware flush. The flush will be done by starting with low cache indices and increment these indices for way 0 of the cache, one index at a time until the maximum index value is obtained. Then, the index will be cleared to zero and the same process is repeated for way 1 of the cache. For each index and way of the cache, the processor will generate a castout operation to the system bus for all modified 32-byte sectors. At the end of the hardware flush, all lines in the L2 tag will be invalidated. During the flush, all memory activity from the icache and dcache are blocked from accessing the L2 until the flush is complete. Snoops, however, are fully serviced by the L2 during the flush. When the L2 tags have been fully flushed of all valid entries, this bit will be reset to b'0" by hardware. When this bit is cleared, it does not necessarily guarantee that all lines from the L2 have been written completely to the system interface. L2 copybacks can still be queued in the bus interface unit. Below is the code which must be run to use L2 Hardware Flush. When the final sync completes, all modified lines in the L2 will have been written to the system address bus. Disable interrupts **dssall** **sync** set L2HWF **sync**
21	L2IO	L2 Instruction-Only. Setting this bit enables instruction-only operation in the L2 cache. For this operation, only transactions from the L1 instruction cache are allowed to be reloaded in the L2 cache. Data addresses already in the cache will still hit for the L1 data cache. When both L2DO and L2IO are asserted, the L2 cache is effectively locked.
22	L2CLKSTP	L2 Clock Stop. Setting this bit enables the automatic stopping of the L2CLK_OUT signals for cache rams that support this function. While L2CLKSTP is set, the L2CLK_OUT signals will automatically be stopped when PC7410M16 enters nap or sleep mode, and automatically restarted when PC7410M16 exits nap or sleep.
23	L2DRO	L2 DLL rollover. Setting this bit enables a potential rollover (or actual rollover) condition of the DLL to cause a checkstop for the processor. A potential rollover condition occurs when the DLL is selecting the last tap of the delay line, and thus may risk rolling over to the first tap with one adjustment while in the process of keeping synchronized. Such a condition is improper operation for the DLL, and, while this condition is not expected, it allows detection for added security. This bit can be set when the DLL is first enabled (set with the L2CLK bits) to detect rollover during initial synchronization. It could also be set when the L2 cache is enabled (with L2E bit) after the DLL has achieved its initial lock.
24-30	–	Reserved
31	L2IP	L2 global invalidate in progress (read only) – See the Freescale user's manual for L2 Invalidation procedure.

6. Power Consideration

6.1 Power Management

The PC7410M16 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are:

- Full-power: This is the default power state of the PC7410M16. The PC7410M16 is fully powered and the internal functional units are operating at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution or external hardware.
- Doze: All the functional units of the PC7410M16 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset or machine check brings the PC7410M16 into the full-power state. The PC7410M16 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC7410M16 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset or a machine check input ($\overline{MCP}$). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if $\overline{QACK}$ is negated, the processor is put in doze mode to support snooping.
- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PLL and SYSCLK. Returning the PC7410M16 to the full-power state requires the enabling of the PLL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset or a machine check input ($\overline{MCP}$) signal after the time required to relock the PLL.

6.2 Power Dissipation

Table 6-1. Power Consumption with $V_{DD} = AV_{DD} = 1.8 \pm 0.1V\ V_{DC}$, $L2V_{DD} = 3.3V \pm 5\%\ V_{DC}$, GND = 0 V_{DC} $0 \leq TJ < 125°C$

		Processor (CPU) Frequency/L2 Frenquency 400 MHz/200 MHz	Unit	Notes
Full-on Mode	Typical	5.7	W	(1)(3)
	Maximum	13.5	W	(1)(2)
Doze Mode Maximum	Maximum	5.3	W	(1)(2)
Nap Mode Maximum	Maximum	2.25	W	(1)(2)
Sleep Mode	Maximum	2.20	W	(1)(2)
Sleep Mode–PLL and DLL Disabled	Maximum	2.0	W	(1)(2)

Notes:
1. These values apply for all valid system bus and L2 bus ratios. The values do not include OV_{DD}; AV_{DD} and $L2AV_{DD}$ suppling power. OV_{DD} power is system dependent, but is typically < 10% of V_{DD} power. Worst case power consumption, for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at V_{DD} = 1.9V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.

3. Typical power is an average value measured at V_{DD} = AV_{DD} = $L2AV_{DD}$ = 1.8V, OV_{DD} = $L2OV_{DD}$ = 2.5V in a system, executing typical applications and benchmark sequences.

7. Electrical Characteristics

7.1 Static Characteristics

Table 7-1. DC Electrical Specifications (see "Recommended Operating Conditions" on page 10)

Symbol	Characteristic	Nominal Bus Voltage[1]	Min	Max	Unit
V_{IH}	Input high voltage (all inputs except SYSCLK)[2][3]	1.8	0.65 x (L2)OV_{DD}	(L2)OV_{DD} + 0.2	V
V_{IH}		2.5	1.7	(L2)OV_{DD} + 0.2	V
V_{IH}		3.3	2.0	(L2)OV_{DD} + 0.3	V
V_{IL}	Input low voltage (all inputs except SYSCLK)	1.8	-0.3	0.35 x OV_{DD}	V
V_{IL}		2.5	-0.3	0.2 x (L2)OV_{DD}	V
V_{IL}		3.3	-0.3	0.8	V
CV_{IH}	SYSCLK input high voltage[2]	1.8	1.5	OV_{DD} + 0.2	V
CV_{IH}		2.5	2.0	OV_{DD} + 0.2	V
CV_{IH}		3.3	2.4	OV_{DD} + 0.3	V
CV_{IL}	SYSCLK input low voltage	1.8	-0.3	0.2	V
CV_{IL}		2.5	-0.3	0.4	V
CV_{IL}		3.3	-0.3	0.4	V
I_{IN}	Input leakage current, V_{IN} = $L2OV_{DD}$/OV_{DD}[2][3]			10	µA
I_{TSI}	High-Z (off-state) leakage current, V_{IN} = $L2OV_{DD}$/OV_{DD}[2][3][5]			10	µA
V_{OH}	Output high voltage, I_{OH} = -6 mA	1.8	(L2)OV_{DD} - 0.45		V
V_{OH}		2.5	1.7		V
V_{OH}		3.3	2.4		V
V_{OL}	Output low voltage, I_{OL} = 6 mA	1.8		0.45	V
V_{OL}		2.5		0.4	V
V_{OL}		3.3		0.4	V
C_{IN}	Capacitance, V_{IN} = 0V, f = 1 MHz[3][4]			7.5	pF

Notes:
1. Nominal voltages; see "Recommended Operating Conditions" on page 10.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

7.2 Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. These specifications are for valid processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency.

7.2.1 Clock AC Specifications

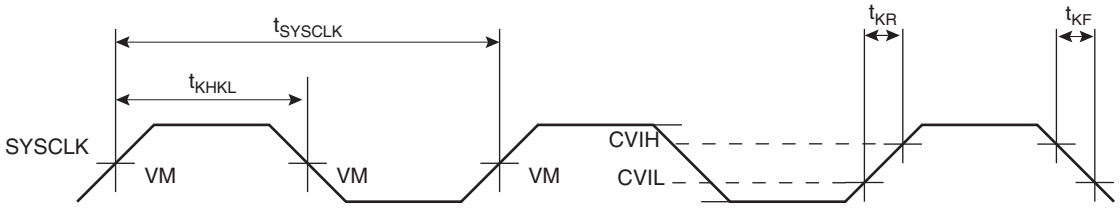
Table 7-2 provides the clock AC timing specifications as defined in Figure 7-1.

Table 7-2. Clock AC Timing Specifications (See “Recommended Operating Conditions” on page 10

Symbol	Characteristic	Maximum Processor Core Frequency				Unit
		400 MHz		450 MHz		
		Min	Max	Min	Max	
f_{CORE}[1]	Processor frequency	350	400	350	450	MHz
f_{VCO}[1]	VCO frequency	450	800	450	900	MHz
f_{SYSCLK}[1]	SYSCLK frequency	33	133	33	133	MHz
t_{SYSCLK}	SYSCLK cycle time	7.5	30	7.5	30	ns
t_{KR} & t_{KF}[2]	SYSCLK rise and fall time		1.0		1.0	ns
t_{KR} & t_{KF}[3]			0.5		0.5	ns
t_{KHKL}/t_{SYSCLK}[4]	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	%
	SYSCLK jitter[5]		±150		±150	ps
	Internal PLL relock time[6]		100		100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in “Clock Selection” on page 25 for valid PLL_CFG[0:3] settings.
2. Rise and fall times for the SYSCLK input measured from 0.4V to 2.4V when OV_{DD} = 3.3V nominal.
3. Rise and fall times for the SYSCLK input measured from 0.2V to 1.2V when OV_{DD} = 1.8V or 2.5V nominal.
4. Timing is guaranteed by design and characterization.
5. This represents total input jitter, short-term and long-term combined, and is guaranteed by design.
6. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 7-1. SYSCLK Input Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.2 Processor Bus AC Specifications

Table 7-3 provides the processor AC timing specifications for the PC7410M16 as defined in Figure 7-3 and Figure 7-4.

Table 7-3. Processor Bus AC Timing Specifications[1] at $V_{DD} = AV_{DD} = 1.8V \pm 100$ mV; $-55°C \le T_J \le 125°C$, $OV_{DD} = 1.8V \pm 100$ mV

Symbol[2]	Parameter	400, 450 MHz		Unit
		Min	Max	
t_{MVRH}[3][4][5][6]	Mode select input setup to $\overline{\text{HRESET}}$	8		t_{SYSCLK}
t_{MXRH}[2][3][5]	$\overline{\text{HRESET}}$ to mode select input hold	0		ns
t_{IVKH}	Input Setup	1.0		ns
t_{IXKH}	Input Hold	0		ns
	Output Valid Times:[7][8]			
t_{KHTSV}	TS		3.0	ns
t_{KHARV}	$\overline{\text{ARTRY}}/\overline{\text{SHD0}}/\overline{\text{SHD1}}$		2.3	
t_{KHOV}	All Other Outputs		3.0	
	Output Hold Times:[7][12]			
t_{KHTSX}	TS	0.5		ns
t_{KHARX}	$\overline{\text{ARTRY}}/\overline{\text{SHD0}}/\overline{\text{SHD1}}$	0.5		
t_{KHOX}	All Other Outputs	0.5		
t_{KHOE}[11]	SYSCLK to Output Enable	0.5		ns
t_{KHOZ}	SYSCLK to Output High Impedance (all except $\overline{\text{ABB/AMON[0]}}$, $\overline{\text{ARTRY}}/\overline{\text{SHD}}$, $\overline{\text{DBB/DMON[0]}}$), $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$)		3.5	ns
t_{KHABPZ}[5][9][11]	SYSCLK to $\overline{\text{ABB/AMON[0]}}$, $\overline{\text{DBB/DMON[0]}}$ High Impedance after precharge		1.0	t_{SYSCLK}
t_{KHARP}[5][10][11]	Maximum Delay to $\overline{\text{ARTRY}}/\overline{\text{SHD0}}/\overline{\text{SHD1}}$ Precharge		1	t_{SYSCLK}
t_{KHARPZ}[5][10][11]	SYSCLK to $\overline{\text{ARTRY}}/\overline{\text{SHD0}}/\overline{\text{SHD1}}$ High Impedance After Precharge		2	t_{SYSCLK}

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 7-3). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs -and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 7-4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds(ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, EMODE, L2VSEL, PLL_CFG[0:3].
7. All other output signals are composed of the following - A[0:31], AP[0:3], TT[0:4], $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
8. Output valid time is measured from 2.4V to 0.8V which may be longer than the time required to discharge from V_{DD} to 0.8V.

9. According to the 60x bus protocol, $\overline{ABB}$ and $\overline{DBB}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 7-2. The nominal precharge width for $\overline{ABB}$ or $\overline{DBB}$ is 0.5 x t_{SYSCLK}, i.e., less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{ABB}$, or $\overline{DBB}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
10. According to the 60x bus protocol, $\overline{ARTRY}$ can be driven by multiple bus masters through the clock period immediately following $\overline{AACK}$. Bus contention is not an issue since any master asserting $\overline{ARTRY}$ will be driving it low. Any master asserting it low in the first clock following $\overline{AACK}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{AACK}$. The nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{SYSCLK} ; i.e., it should be high-Z as shown in Figure 7-2 before the first opportunity for another master to assert $\overline{ARTRY}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
11. Guaranteed by design and not tested.
12. Output hold time characteristics can be altered by the use of the L2_TSTCK pin during system reset, similar to L2 output hold being altered by the use of bits [14-15] in the L2CR register. Information on the operation of the L2_TSTCLK will be included in future revisions of this specification.

Figure 7-2. Input/Output Timing Diagram

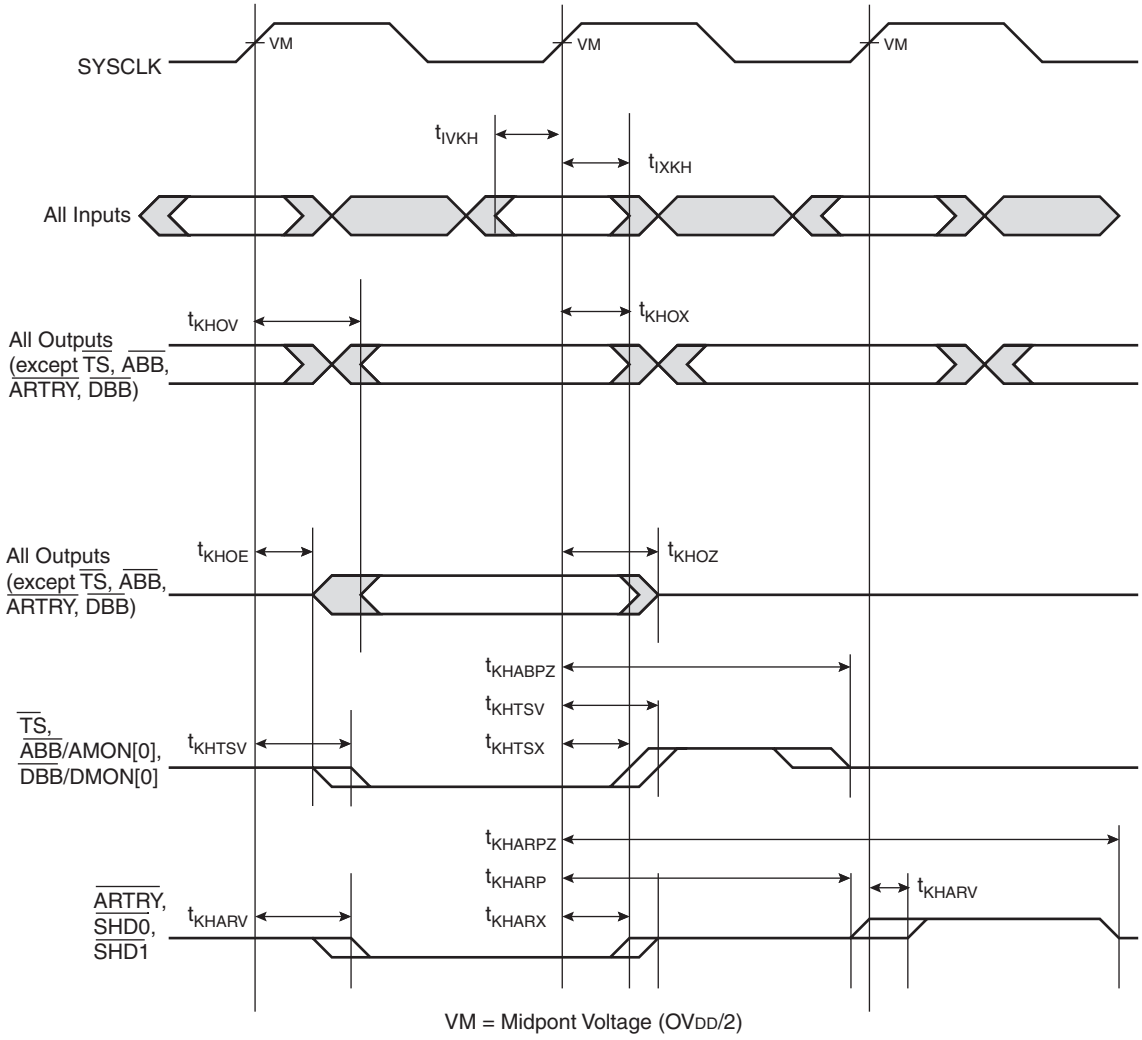


Figure 7-3. AC Test Load for the 60x Interface

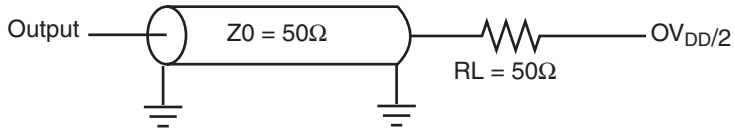
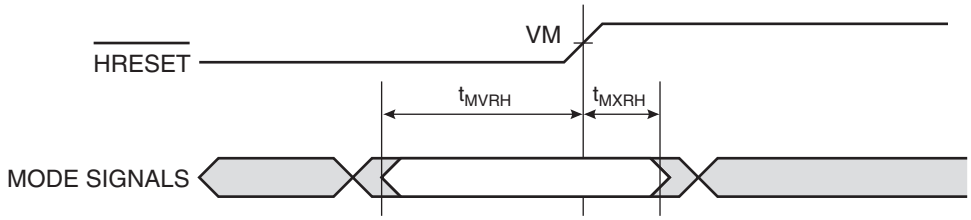


Figure 7-4. Mode Input Timing Diagram



where VM = Midpoint Voltage ($OV_{DD}/2$)

7.2.3 IEEE 1149.1 AC Timing Specifications

Table 7-4 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 7-5, Figure 7-6, Figure 7-7 and Figure 7-8.

Table 7-4. JTAG AC Timing Specifications (Independent of SYSCLK)(1) at Recommended Operating Conditions (see page 10)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30		ns
t_{JHJL}	TCK clock pulse width measured at $OV_{DD}/2$	15		ns
t_{JR} & t_{JF}	TCK rise and fall times	0	2	ns
t_{TRST}(2)	$\overline{TRST}$ assert time	25		ns
	Input Setup Times:			
t_{DVJH}(3)	Boundary-scan data	4		ns
t_{IVJH}	TMS, TDI	0		
	Input Hold Times:			
t_{DXJH}(3)	Boundary-scan data	20		ns
t_{IXJH}	TMS, TDI	25		
	Valid Times:			
t_{JLDV}(4)	Boundary-scan data	4	20	ns
t_{JLOV}	TDO	4	25	
	TCK to output high impedance:			
t_{JLDZ}(4)(5)	Boundary-scan data	3	19	ns
t_{JLOZ}(5)	TDO	3	9	

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 7-5). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.

3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization

Figure 7-5. Alternate AC Test Load for the JTAG Interface

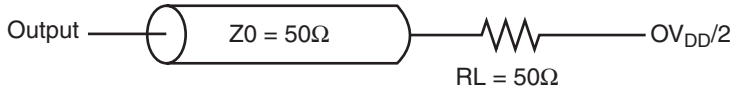
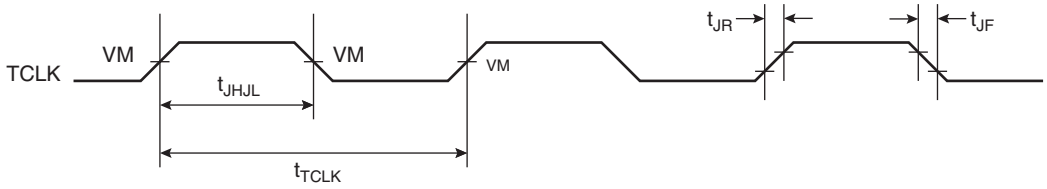
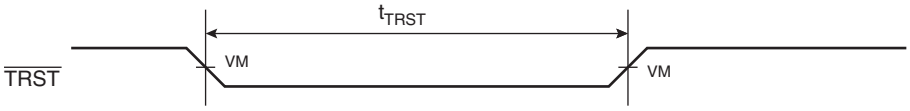


Figure 7-6. JTAG Clock Input Timing Diagram



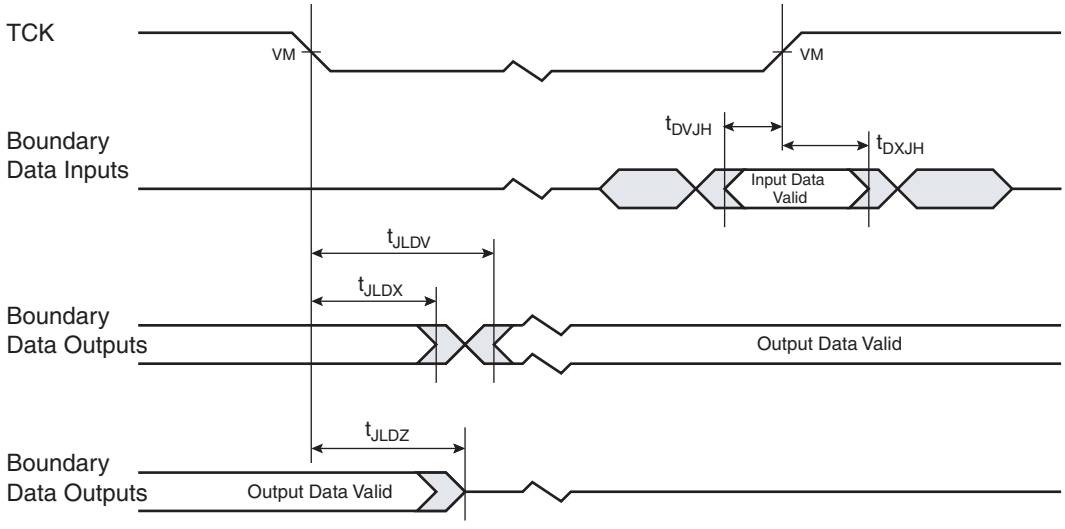
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-7. $\overline{\text{TRST}}$ Timing Diagram



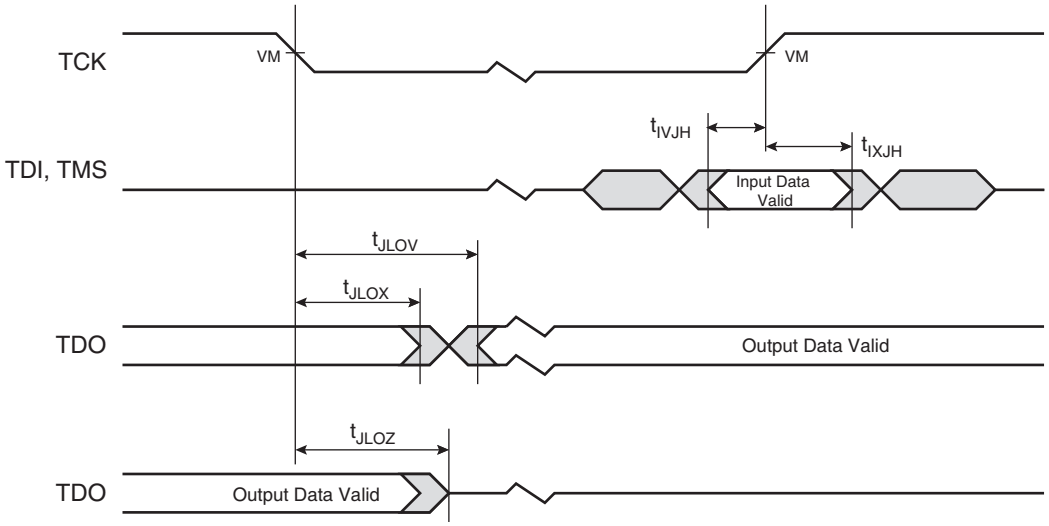
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-8. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-9. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage (OV_{DD}/2)

8. Preparation for Delivery

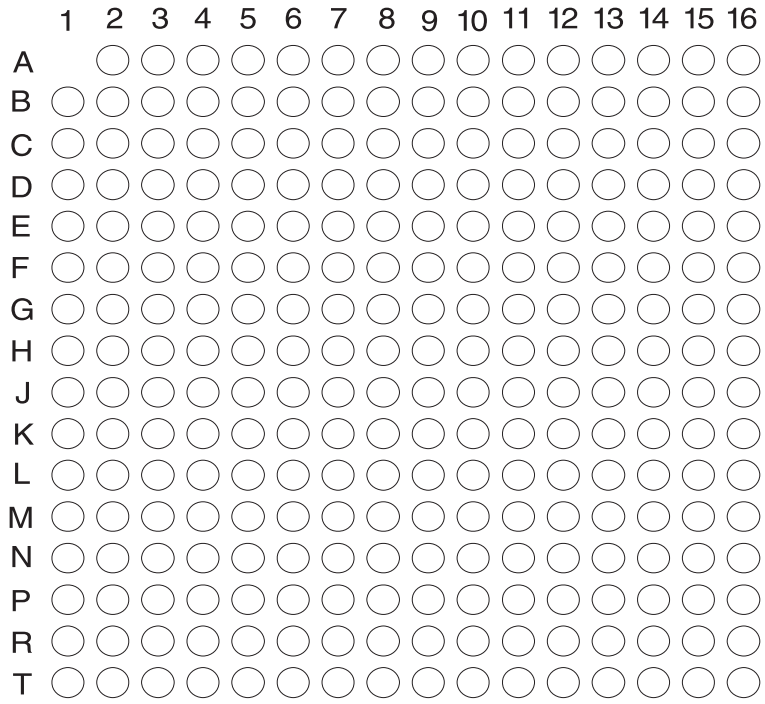
8.1 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces
- Ground test equipment, tools and operator
- Do not handle devices by the leads
- Store devices in conductive foam or carriers
- Avoid use of plastic, rubber or silk in MOS areas
- Maintain relative humidity above 50% if practical
- For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the normal CBGA

Figure 8-1. Pin Assignments

Ball assignments of the 255 CBGA package as viewed from the top surface



Side profile of the CBGA package to indicate the direction of the top surface view

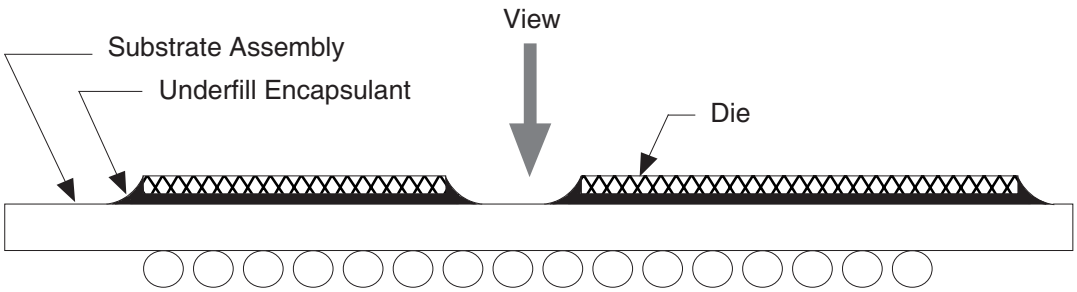


Table 8-1. Package Pinout Listing

Signal Name	Pin Number	Active	I/O	1.8V[7]	2.5V[7]	3.3V[7]
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O			
$\overline{\text{AACK}}$	L2	Low	Input			
$\overline{\text{ABB}}$/$\overline{\text{AMONO}}$[8]	K4	Low	Output			
AP[0-3]	C1, B4, B3, B2	High	I/O			
$\overline{\text{ARTRY}}$	J4	Low	I/O			

Table 8-1. Package Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O	1.8V[7]	2.5V[7]	3.3V[7]
AV_{DD}	A10	–	–	1.8V	1.8V	1.8V
$\overline{BG}$	L1	Low	Input			
$\overline{BR}$	B6	Low	Output			
BVSEL[4][6]	B1	High	Input	GND	$\overline{HRESET}$	OV_{DD}
$\overline{CHK}$[5][6][13]	C6	Low	Input			
$\overline{CI}$	E1	Low	Output			
$\overline{CKSTP\_IN}$	D8	Low	Input			
CKSTP_OUT	A6	Low	Output			
CLK_OUT	D7	–	Output			
$\overline{DBB}$/DMONO[8]	J14	Low	Output			
$\overline{DBG}$	N1	Low	Input			
$\overline{DBWO}$/DTIO	G4	Low	Input			
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O			
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O			
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O			
$\overline{DRDY}$[5][9][12]	D5	Low	Output			
DTI 1-2[9][11]	G16, H15	Low	Input			
$\overline{EMODE}$[10][11]	C4	Low	Input			
$\overline{GBL}$	F1	Low	I/O			
GND	C5, C12, E3, E6, E8, E9, E11, E14, F3, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	–	–	GND	GND	GND
$\overline{HIT}$[5][12]	A3	Low	Output			
$\overline{HRESET}$	A7	Low	Input			
$\overline{INT}$	B15	Low	Input			
L1_TSTCLK[1]	D11	High	Input			
L2_TSTCLK[1]	D12	High	Input			
$L2AV_{DD}$	L11	–	–	1.8V	1.8V	1.8V
$L2V_{DD}$[5][7]	A2, B8, C3, D6, J16	–	–	3.3V	3.3V	3.3V
$L2OV_{DD}$	E10, E12, M12, G12, G14, K12, K14	–	–		2.5V	N/A
L2VSEL[3][6]	B5	High	Input	[15]–	$\overline{HRESET}$	N/A
$\overline{LSSD\_MODE}$[1]	B10	Low	Input		3.3V	
$\overline{MCP}$	C13	Low	Input			

Table 8-1. Package Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O	1.8V(7)	2.5V(7)	3.3V(7)
NC (No-connect)	B7, C8	–	–			
OV_{DD}(2)	C7, E5, G3, G5, K3, K5, P7, P10, E07, M05, M07, M10	–	–			
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input			
$\overline{QACK}$	D3	Low	Input			
$\overline{QREQ}$	J3	Low	Output			
$\overline{RSRV}$	D1	Low	Output			
$\overline{SHDO-1}$(5)(14)	A4, A5	Low	I/O			
$\overline{SMI}$	A16	Low	Input			
$\overline{SRESET}$	B14	Low	Input			
SYSCLK	C9	–	Input			
$\overline{TA}$	H14	Low	Input			
TBEN	C2	High	Input			
$\overline{TBST}$	A14	Low	I/O			
TCK	C11	High	Input			
TDI(6)	A11	High	Input			
TDO	A12	High	Output			
$\overline{TEA}$	H13	Low	Input			
TMS(6)	B11	High	Input			
TRST(6)	C10	Low	Input			
$\overline{TS}$	J13	Low	I/O			
$\overline{TSIZ}$[0-2]	A13, D10, B12	High	Output			
TT[0-4]	B13, A15, B16, C14, C15	High	I/O			
V_{DD}(2)	F6, F8, F9, F11, G7, G10, H4, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9	–	–	1.8V	1.8V	
$\overline{WT}$	D2	Low	Output			

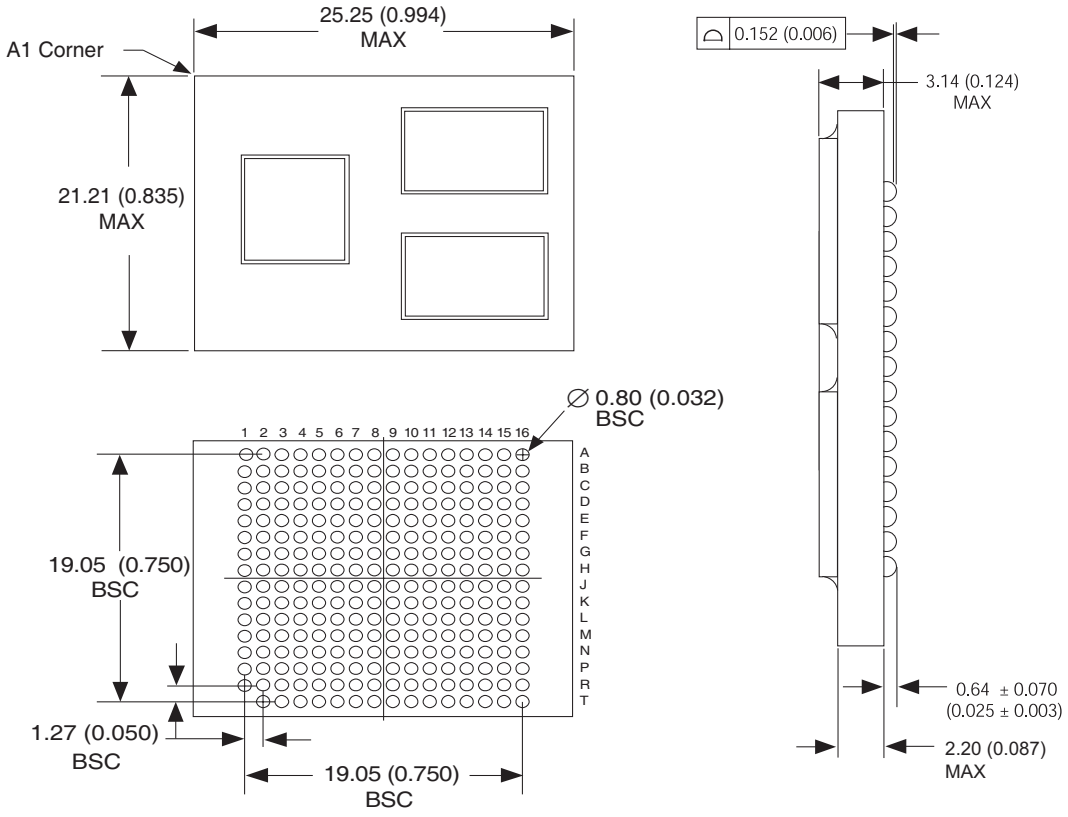
Notes:
1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
3. To allow future L2 cache I/O interface voltage changes.
4. To allow processor bus I/0 voltage changes, provide the option to connect BVSEL to $\overline{HRESET}$ (Selects 2.5V Interface) or to GND (Selects 1.8V Interface) or to OV_{DD} (Selects 3.3V Interface).
5. Uses one of 9 existing no-connects in PC755BM8.
6. Internal pull up on die.
7. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache I/O interface (L2ADDR (0-18], L2DATA (0-63), L2DP{0-7] and L2SYNC-OUT) and the L2 control signals; $L2AV_{DD}$ supplies power to the SSRAM core memory; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration and the voltage supplied. For actual recommended value of Vin or supply voltages see Recommended Operating Conditions.

8. Output only for 7410, was I/O for 750/755.
9. Enhanced mode only.
10. Deasserted (pulled high) at $\overline{\text{HRESET}}$ for 60x bus mode.
11. Reuses 750/755 $\overline{\text{DRTRY}}$, $\overline{\text{DBIS}}$, and TLBISYNC pins (DTI1, DTI2, and $\overline{\text{EMODE}}$ respectively).
12. Unused output in 60x bus mode.
13. Connect to $\overline{\text{HRESET}}$ to trigger post power-on-reset (por) internal memory test.
14. Ignored in 60x bus mode.
15. Not supported on this version.

Table 8-2. Package Description

Package Outline	21 x 25 mm
Interconnects	255 (16 x 16 ball array less one)
Pitch	1.27 mm
Maximum module height	3.90 mm
Ball diameter	0.8 mm

Figure 8-2. Package Dimensions 255 Ball Grid Array



9. Clock Selection

The PC7410M16's PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC7410M16 is shown in Table 9-1 for example frequencies.

Table 9-1. PC7410M16 Microprocessor PLL Configuration

PLL_CFG[0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	**Core-to-VCO Multiplier**	**Bus 33.3 MHz**	**Bus 50 MHz**	**Bus 66.6 MHz**	**Bus 75 MHz**	**Bus 83.3 MHz**	**Bus 100 MHz**	**Bus 133 MHz**
0100	2x	2x							
0110	2.5x	2x							
1000	3x	2x							400 (800)
1110	3.5x	2x						350 (700)	
1010	4x	2x						400 (800)	
0111	4.5x	2x					375 (750)	450 (900)	
1011	5x	2x				375 (750)	416 (833)		
1001	5.5x	2x			366 (733)	412 (825)			
1101	6x	2x			400 (800)	450 (900)			
0101	6.5x	2x			433 (866)				
0010	7x	2x			350 (700)				
0001	7.5x	2x			375 (750)				
1100	8x	2x		400 (800)					
0000	9x	2x		450 (900)					
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC7410M16; see "Clock AC Specifications" on page 15 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7410M16 regardless of the SYSCLK input.

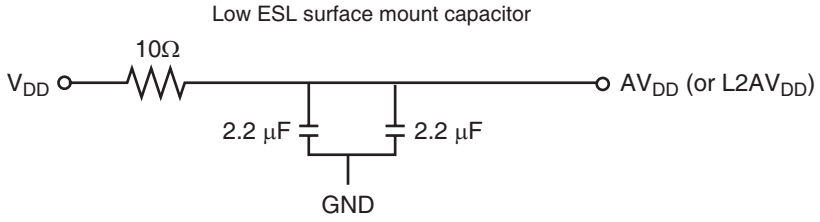
10. System Design Information

10.1 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC7410M16 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 10-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360-ball CBGA footprint without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

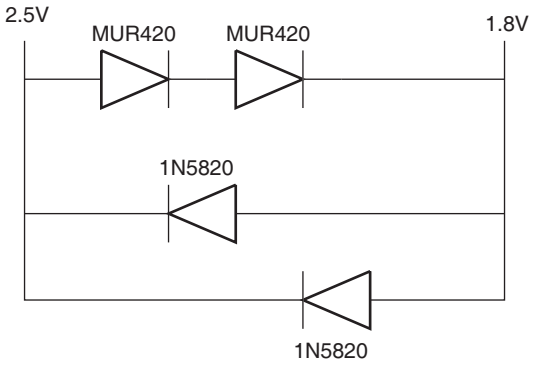
Figure 10-1. PLL Power Supply Filter Circuit



10.2 Power Supply Voltage Sequency

The notes in section "Absolute Maximum Ratings(1)" on page 8 contain cautions about the sequencing of the external bus voltages and core voltage of the PC7410M16 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes will be forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, one or both of the circuits of Figure 10-2 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 10-2 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

Figure 10-2. Example Voltage Sequencing Circuits



10.3 Decoupling Recommendations

Due to the PC7410M16's dynamic power management feature, large address and data buses and high operating frequencies, the PC7410M16 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7410M16 system and the PC7410M16 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the PC7410M16. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling PowerPC microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100 - 330 µF (AVX TPS tantalum or Sanyo OSCON).

10.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the PC7410M16.

See "IEEE 1149.1 AC Timing Specifications" on page 18 for a discussion of the L2SYNC_OUT and L2SYNC_IN signals.

10.5 Output Buffer DC Impedance

The PC7410M16 60x and L2 I/O drivers are characterized over process, voltage and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 10-3).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value.
Then $Z_0 = (R_P + R_N)/2$.

Figure 10-3. Driver Impedance Measurement

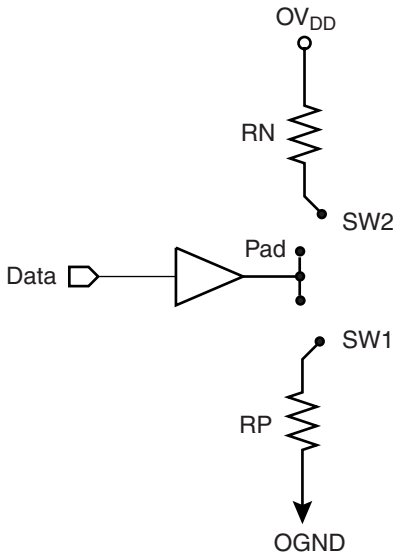


Table 10-1 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 10-1. Impedance Characteristics with V_{DD} = 1.8V, OV_{DD} = 1.8V or 2.5V, T_J = -55°C to 125°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5 - 54.3	42.7 - 54.1	Z_0	Ω
R_P	37.3 - 55.3	39.3 - 50	Z_0	Ω

10.6 Pull-up Resistor Requirements

The PC7410M16 requires high-resistive (weak: 10 kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7410M16 or other bus masters. These pins are $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$ and $\overline{SHD1}$.

In addition, the PC7410M16 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 kΩ – 10 kΩ) if it is used by the system. This pin is $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may therefore float in the high-impedance state for relatively long periods of time. Since the PC7410M16 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7410M16 or by other receivers in the system. It is recommended that these signals be pulled up through weak (10 kΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are A[0:31], AP[0:3], TT[0:4], and $\overline{GBL}$.

In systems where $\overline{GBL}$ is not connected and another device may be asserting $\overline{TS}$ for a snoopable transaction while not driving $\overline{GBL}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and therefore do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are D[0:63], DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

10.7 JTAG Configuration Signals

Figure 10-4. Suggested $\overline{\text{TRST}}$ Connection

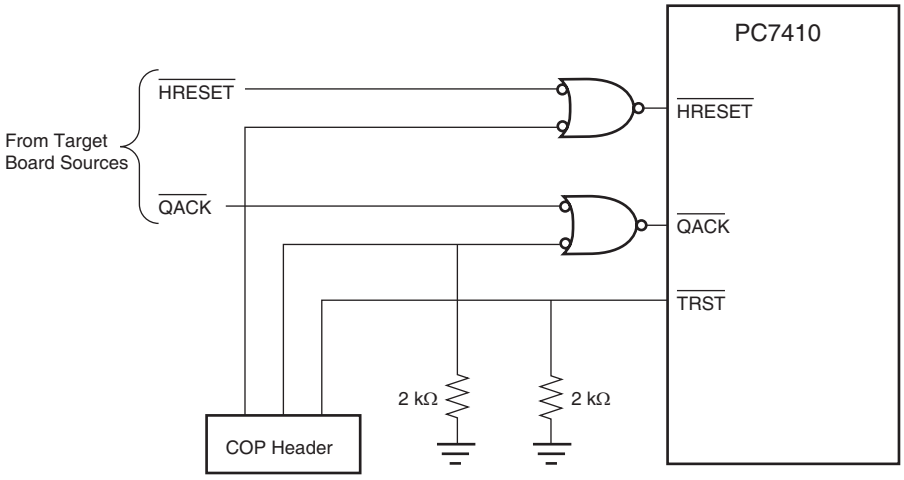
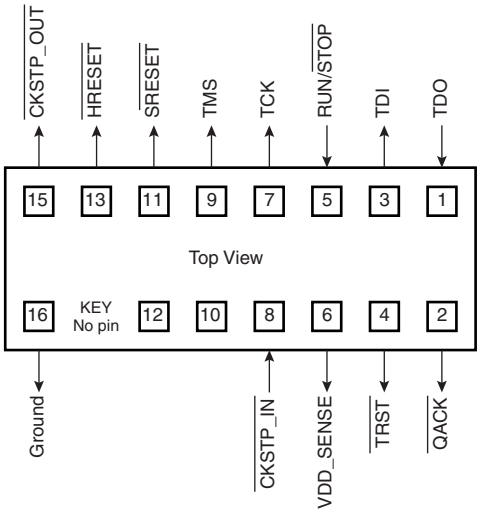


Figure 10-5. COP Connector Diagram



Note: Pins 10, 12 and 14 are no connects. Pin 14 is not physically present.

Table 10-2. COP Pin Definitions

Pins	Signal	Connection	Special Notes
1	TDO	TDO	
2	$\overline{\text{QACK}}$	QACK	Add 2K pull-down to ground. Must be merged with on-board $\overline{\text{QACK}}$, if any.
3	TDI	TDI	
4	$\overline{\text{TRST}}$	TRST	Add 2K pull-down to ground. Must be merged with on-board $\overline{\text{TRST}}$ if any. See Figure 10-4.
5	RUN/$\overline{\text{STOP}}$	No Connect	Used on 604e; leave no-connect for all other processors.
6	VDD_SENSE	VDD	Add 2K pull-up to OV_{DD} (for short circuit limiting protection only).
7	TCK	TCK	
8	$\overline{\text{CKSTP\_IN}}$	CKSTP_IN	Optional. Add 10K pull-up to OV_{DD}. Used on several emulator products. Useful for checkstopping the processor from a logic analyzer of other external trigger.
9	TMS	TMS	
10	N/A		
11	$\overline{\text{SRESET}}$	SRESET	Merge with on-board $\overline{\text{SRESET}}$, if any.
12	N/A		
13	$\overline{\text{HRESET}}$	HRESET	Merge with on-board $\overline{\text{HRESET}}$.
14	N/A		Key location; pin should be removed.
15	$\overline{\text{CKSTP\_OUT}}$	CKSTP_OUT	Add 10K pull-up to OV_{DD}.
16	Ground	Digital Ground	

Boundary scan testing is enabled through the JTAG interface signals. (BSDL descriptions of the PC7410M16 are available on the Internet at:
www.mot.com/PowerPC/teksupport.).
The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all PowerPC implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The common on-chip processor (COP) function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 10-4 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. The pull-down resistor on $\overline{\text{TRST}}$ ensures that the JTAG scan chain is initialized during power-on if a JTAG interface cable is not attached; if it is attached, it is responsible for driving $\overline{\text{TRST}}$ when needed.

The COP header shown in Figure 10-4 adds many benefits – breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a "Berg" header). The connector typically has pin 14 removed as a connector key, as shown in Figure 10-5.

11. Definitions

11.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

12. Ordering Information

xx 7410 M 16 y xxx nnnn L x

Product Code (1)	Part Identifier		L2 cache densik	Temperature Range T_J (1)	Package (1)	Max Internal Processor Speed (1)	Application Modifier (1)	Revision Level (1)
PC(X) (2)	7410	Multichip Package	16 Mbits: 256K x 72 SSRAM	V: -40˚C, +110˚C M: -55˚C, +125˚C	G: CBGA GH: HITCE (TBC)	400 MHz 450 MHz (TBC)	L: 1.8V ± 100 mV	E

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

13. Document Revision History

Table 13-1 provides a revision history for this hardware specification.

Table 13-1. Document Revision History

Rev. No	Date	Substantive Change(s)
C	07/2007	Name change from Atmel to e2v Ordering information update
B	11/2004	Product specification release subsequent to product qualification Motorola changed to Freescale
A	11/2002	Initial revision

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