AT84AD001-EB Evaluation Kit

User Guide

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Section 1
Introduction

1.1 Scope

The AT84AD001-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the AT84AD001B dual 8-bit 1 Gsps ADC.

The AT84AD001-EB Evaluation Kit includes:

- The dual 8-bit 1 Gsps ADC evaluation board.
- A cable for connection to the RS-232 port.
- 8 SMA caps for CLKQ, CLKQN, CLKI, CLKIN, VINQ, VINQB, VINI, VINIB SMAs.
- Software tools necessary for the use of the 3-wire serial digital interface.

This user guide uses the AT84AD001-EB Evaluation Kit as an evaluation and demonstration platform and provides guidelines for its proper use.

This user guide usually refers to the dual 8-bit 1 Gsps ADC datasheet ref. 0817F.

1.2 Description

Thanks to its user-friendly interface, the AT84AD001-EB Evaluation Kit enables testing of all the functions of the AT84AD001B dual 8-bit 1 Gsps ADC:

- Input clock selection
- Analog input switch selection
- Autocalibration function
- Gain and offset control
- Standby mode
- 1:1 or 1:2 demultiplexer function
- Die junction temperature monitoring function

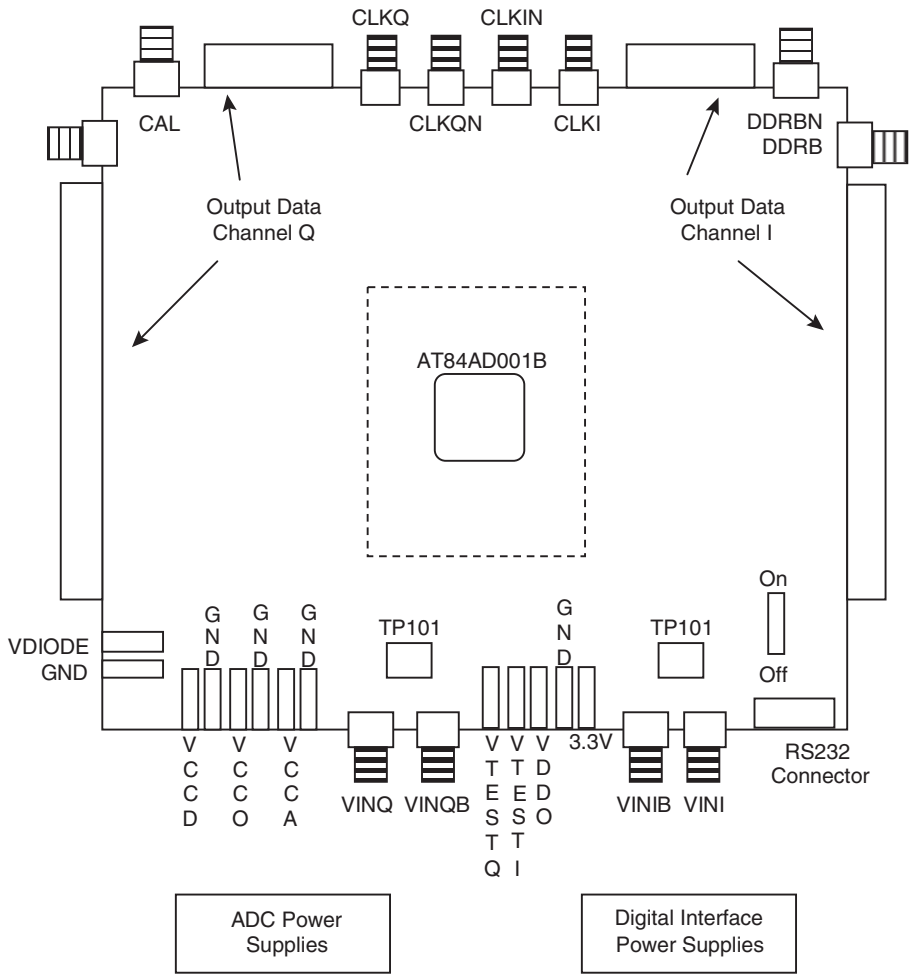
To achieve optimal performance, the AT84AD001-EB Evaluation Board was designed in a 4-metal-layer board with FR4 dielectric layers. The board implements the following devices:

- The AT84AD001B dual 8-bit 1 Gsps ADC device
- SMA connectors for the analog and clock inputs

- 2.54 mm pitch connectors for the digital data and clock inputs (compatible with high frequency acquisition system probes)
- An RS-232 connector for PC interface
- Banana jacks for the power supply accesses

The board is made of four metal layers for signal traces, ground and power supply layers, and three dielectric layers featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain. The board dimensions are 193 mm × 216 mm.

Figure 1-1. AT84AD001-EB Evaluation Board Block Diagram



As shown in Figure 1-1, five different power supplies are required:

- V_{CCA} = 3.3V ADC analog power supply
- V_{CCD} = 3.3V ADC digital power supply
- V_{CCO} = 2.25V ADC output power supply
- V_{DDO} = 2.25V digital interface power supply (can be connected to V_{CCO})
- 3.3V digital interface primary power supply for the microcontroller

Finally, two RF transformers (TP-101) are provided for the analog inputs (V_{INI} and V_{INQ}). They enable you to operate the ADC in differential mode via single-ended analog inputs.

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Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full-speed operation of the AT84AD001B dual 8-bit 1 Gsps ADC, a multi-layer board structure was retained for the Evaluation Board. Four copper layers are used, respectively dedicated to the signal traces, ground planes and power supply planes. Each layer is separated by an FR4 epoxy dielectric layer.

The following table gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Thickness of copper = 35 µm Input signals: 50Ω microstrip lines
Layer 2 FR4 dielectric layer	Thickness of layer = 200 µm Dielectric constant = 4.6
Layer 3 Copper layer	Thickness of copper = 35 µm Reference plane (GND)
Layer 4 FR4 dielectric layer	Thickness of layer = 400 µm Dielectric constant = 4.6
Layer 5 Copper layer	Thickness of copper = 35 µm Power Supplies plane
Layer 6 FR4 dielectric layer	Thickness of layer = 860 µm Dielectric constant = 4.6
Layer 7 Copper layer	Thickness of copper = 35 µm Reference plane (GND) + DDRB, DDRBN reset signals and calibration signal

The board is 1.6 mm thick.

The input/output signal traces occupy the top metal layer, except for the DRRB and DRRBN Data Ready Asynchronous Reset signals, which are located on the fourth metal layer, together with the second reference plane. The ground planes occupy the second and fourth planes. The third layer is dedicated to the power supplies (both ADC and digital interfaces).

2.2 Analog and Clock Inputs/ Digital Outputs

The board uses 50Ω impedance microstrip lines for the differential analog and clock inputs, and the differential digital outputs.

The analog and clock inputs are routed on one layer only (top metal layer), without use of through-hole vias.

The line lengths are matched to within approximately 1 mm. The clock input lines are AC coupled via 10 nF chip capacitors.

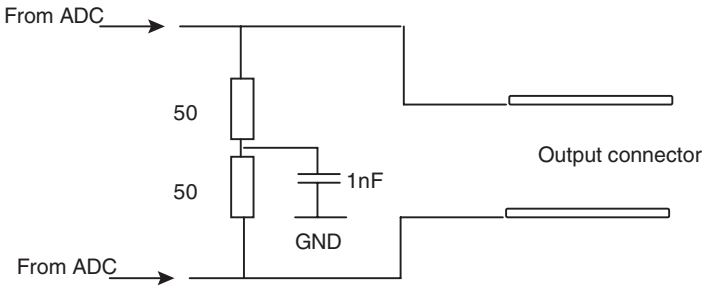
The analog input lines are coupled to ground. In addition, the analog input lines are correctly reverse-terminated by 50Ω surface mount chip resistors, which are placed very close to the ADC device.

The analog inputs are accessed via SMA connectors in single-ended fashion. The signals are then translated to differential signals by way of two RF transformers (one for each channel). The transformers used are of TP-101 type (see “Appendices” on page 1 for more information).

The output data trace lengths are matched to within approximately 5 mm to minimize the data output skew.

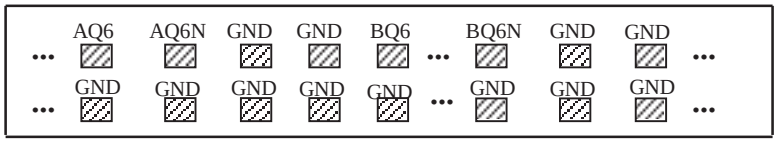
All digital outputs are 50Ω differentially terminated to ground via a 1 nF chip capacitor, as shown in Figure 2-1.

Figure 2-1. Data Output Differential On-board Termination



The digital output data is accessed via two rows of 2.54 mm pitch connectors, as illustrated in Figure 2-2.

Figure 2-2. Output Data 2.54 mm Pitch Connector



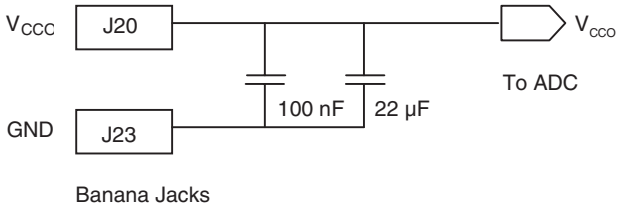
2.3 Power Supplies

The fifth metal layer is dedicated to the ADC’s power supplies and to the digital interface (V_{CCA}, V_{CCD}, V_{CCO}, V_{DDO}, 3.3V for the microcontroller).

Each incoming power supply is decoupled by 22 µF tantalum chip capacitors in parallel to a 100 pF ceramic chip capacitor, located as close as possible to the power supply accesses (banana jacks).

An example is given for V_{CCO} in Figure 2-3 on page 3.

Figure 2-3. Power Supply Decoupling Scheme



Each power supply is bypassed very close to the device by 10 nF in parallel to 100 pF chip capacitors.

Note: These capacitors are superimposed with the 100 pF capacitor mounted first.

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Section 3

Operating Characteristics and Procedures

3.1 Introduction

This section describes a typical configuration for analog and clock inputs.

The Evaluation Board is designed to facilitate the evaluation and the characterization of the AT84AD001B dual 8-bit 1Gsps ADC.

The input signals are accessed in single-ended fashion and the RF transformer is used to translate them into differential signals.

Note: For proper operation of the ADC, the analog input signal has to be used in differential mode using an RF transformer.

The clock inputs are accessed in single-ended or differential mode, with a preference for the single-ended configuration as it corresponds to the easiest and quickest setting for evaluating the AT84AD001B dual 8-bit 1Gsps ADC.

The RF sources can be connected directly to the ADC's in-phase clock input.

3.2 Operating Procedure

1. Connect the ADC's power supplies and ground accesses (V_{CCA} = 3.3V, GND = 0V, V_{CCD} = 3.3V, V_{CCO} = 2.25V) through the dedicated banana jacks.
   V_{CCA} and V_{CCD} have separated supply planes.

2. Connect the serial interface's power supplies and ground accesses (V_{DDO} = 2.25V, GND = 0V, 3.3V) through the dedicated banana jacks.
   V_{CCO} and V_{DDO} can be connected together.

3. Connect the CLKQ or CLKI clock signals (depending on your ADC configuration).
   The inverse phase clock inputs CLKQN and CLKIN must be connected to a 50Ω load. Use a low-phase noise RF source. The clock input level can be set to -9 dBm and should not exceed 6 dBm into a 50Ω terminal resistor. The clock frequency can range from 50 MHz to 1 Gsps.

4. Connect the VINQ or VINI input signals (depending on your ADC configuration). Use a low-phase noise RF source. Full-scale is 0.250V peak-to-peak around 0V (±125 mV). The analog input frequency can range from 1 MHz to 1.5 GHz.

5. Connect the high-speed data acquisition system probes to the output connector. The connector pitch (2.54 mm) is compatible with High-speed Digital Acquisition System probes. The digital data is differentially terminated on-board. However, the output data can be intercepted in either single-ended or differential mode.
6. Serial interface: connect your PC's RS-232 connector to the Evaluation Board.
7. Serial mode inactive: turn off the switch (green LED off).

All instrumentation and connectors are now connected.

8. Switch on the ADC supplies first (start with the V_{CCA} and V_{CCD} power supplies).
9. Serial interface: switch the V_{DDO} power supply on first.
10. Turn the RF clock generator on.
11. Turn the RF input generator on.
12. Serial mode inactive: turn off the switch (green LED off) /RESET Mode.
13. Serial mode active: turn on the switch (green LED on).
14. Serial interface software:

    The ADC has been correctly turned on and the serial interface can now be run.

    The ADC can then be configured as needed by using the specified software tools (refer to Section 4 for further information).

3.3 Electrical Characteristics

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Analog positive supply voltage	V_{CCA}	3.6	V
Digital positive supply voltage	V_{CCD}	3.6	V
Output supply voltage	V_{CCO}	3.6	V
Maximum difference between V_{CCA} and V_{CCD}	V_{CCA} to V_{CCD}	± 0.8	V
Minimum V_{CCO}	V_{CCO}	1.6	V
Serial interface 2.25V	V_{DDO}	2.5	V
Serial interface 3.3V	3V3	3.6	V
Analog input voltage	V_{INI} or V_{INIB} V_{INQ} or V_{INQB}	1/-1	V
Digital input voltage	V_D	-0.3 to V_{CCD} + 0.3	V
Clock input voltage	V_{CLK} or VC_{LKB}	-0.3 to V_{CCD} + 0.3	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}	-2 to 2	V
Maximum junction temperature	T_J	125	°C
Storage temperature	T_{stg}	-65 to 150	°C
Lead temperature (soldering 10s)	T_{leads}	300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

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Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Recommended Value	Unit
Analog supply voltage	V_{CCA}	3.3	V
Digital supply voltage	V_{CCD}	3.3	V
Output supply voltage	V_{CCO}	2.25	V
Serial interface 2.25V	V_{DDO}	2.25	V
Serial interface 3.3V	3V3	3.3	V
Differential analog input voltage (full-scale)	V_{INi} -V_{IniB} or V_{INQ} -V_{INQB}	500	mVpp
Differential clock input level	Vinclk	600	mVpp
Internal settling adjustment	ISA	-50	ps
Operating temperature range	$T_{Ambient}$	0 < T_A < 70 (“C “ grade) -40 < T_A < 85 (“ I “ grade)	°C

Note: V_{DDO} should not differ from V_{CCO} by more than ±5%.
I(V_{DDO}) and I(3V3) should not exceed 100 mA.

The following conditions apply to the electrical operating characteristics given in Table 3-3.

Unless otherwise specified:

- V_{CCA} = 3.3V; V_{CCD} = 3.3V; V_{CCO} = 2.25V
- V_{INI} - V_{INIB} or V_{INQ} - V_{INQB} = 500 mVpp full-scale differential input
  Digital outputs LVDS (100Ω)
- T_A (typical) = 25°C. Full temperature range: 0°C < T_A < 70°C (commercial grade) or -40°C < T_A < 85°C (industrial grade)

Table 3-3. Electrical Operating Characteristics in Nominal Conditions (Gain Setting 0 dB, One Clock Input, No Standby Mode [Full Power Mode], 1:1 DMUX, Calibration Off)

Parameter	Symbol	Min	Typ	Max	Unit
Resolution			8		Bits
Power Requirements					
Positive supply voltage					
Analog	V_{CCA}	3.15	3.3	3.45	V
Digital	V_{CCD}	3.15	3.3	3.45	V
Output digital (LVDS) and serial interface	V_{CCO}	2.0	2.25	2.5	V
Supply current (typical conditions)					
Analog	I_{CCA}		150	180	mA
Digital	I_{CCD}		230	275	mA
Output	I_{CCO}		100	120	mA
Supply current (1:2 DMUX mode)					
Analog	I_{CCA}		150	180	
Digital	I_{CCD}		260	310	mA
Output	I_{CCO}		175	210	mA
Supply current (2 input clocks, 1:2 DMUX mode)					
Analog	I_{CCA}		150	180	mA
Digital	I_{CCD}		290	350	
Output	I_{CCO}		180	215	
Supply current (1 channel only, 1:1 DMUX mode)					
Analog	I_{CCA}		80	95	mA
Digital	I_{CCD}		160	190	mA
Output	I_{CCO}		55	65	mA
Supply current (1 channel only, 1:2 DMUX mode)					
Analog	I_{CCA}		80	95	mA
Digital	I_{CCD}		170	205	mA
Output	I_{CCO}		90	110	mA
Supply current (full standby mode)					
Analog	I_{CCA}		12	20	mA
Digital	I_{CCD}		24	39	mA
Output	I_{CCO}		3	7	mA

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Table 3-3. Electrical Operating Characteristics in Nominal Conditions (Gain Setting 0 dB, One Clock Input, No Standby Mode [Full Power Mode], 1:1 DMUX, Calibration Off) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Nominal dissipation (1 clock, 1:1 DMUX mode, 2 channels)	P_D		1.4	1.7	W
Nominal dissipation (full standby mode)	stbpd		120		mW
Analog Inputs					
Full-scale differential analog input voltage	V_{INi} - V_{IniB} or V_{INQ} - V_{INQB}	450	500	550	mV mV
Analog input capacitance I and Q	C_{IN}			2	pF
Full Power input bandwidth (-3 dB)	FPBW		1.5		GHz
Gain flatness (-0.5dB)			500		MHz
Clock Input					
Logic compatibility for clock inputs and DDRB Reset (pins 124,125,126,127,128,129)		PECL/ECL/LVDS			
PECL/LVDS clock inputs voltages ($V_{CLKI/IN}$ or $V_{CLKQ/QN}$) Differential logical level	V_{IL} - V_{IH}		600		mV
Clock input power level		-9	0	6	dBm
Clock input capacitance			2		pF
Digital Outputs					
Logic compatibility for digital outputs (depending on the value of V_{CCO})		LVDS			
Differential output voltage swings (assuming V_{CCO} = 2.25V)	V_{OD}	220	270	350	mV
Output levels (assuming V_{CCO} = 2.25V) 100Ω differentially terminated Logic *0* voltage Logic *1* voltage	 V_{OL} V_{OH}	 1.0 1.25	 1.1 1.35	 1.2 1.48	 V V
Output offset voltage (assuming V_{CCO} = 2.25V) 100Ω differentially terminated	V_{OS}	1125	1250	1340	mV
Output impedance	R_O		50		W
Output current (shorted output)				12	mA
Output current (grounded output)			30		mA
Output level drift with temperature			1.3		mV/°C
Digital Input (Serial Interface)					
Maximum clock frequency (input clk)	Fclk			50	MHz
Input logical level *0* (clk, mode, data, ldn)		-0.4	0	0.4	V
Input logical level *1* (clk, mode, data, ldn)		V_{CCO} - 0.4	V_{CCO} - 0.4	V_{CCO} + 0.4	V
Output logical level *0* (cal)		-0.4	0	0.4	V
Output logical level *1* (cal)		V_{CCO} - 0.4	V_{CCO}	V_{CCO} + 0.4	V
Maximum output load (cal)				15	pF

3.3.1 Timing Diagrams

Figure 3-1. Timing Diagram, ADC I or ADC Q, 1:2 DMUX Mode, Clock I for ADC I, Clock Q for ADC Q

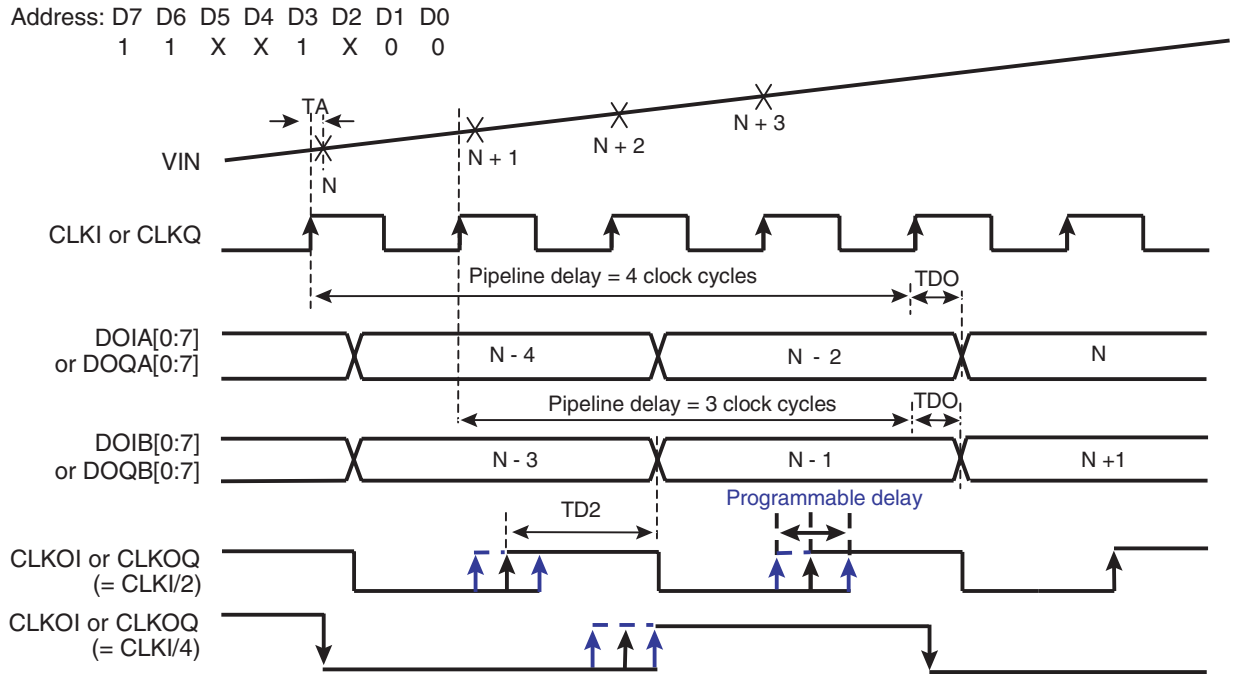
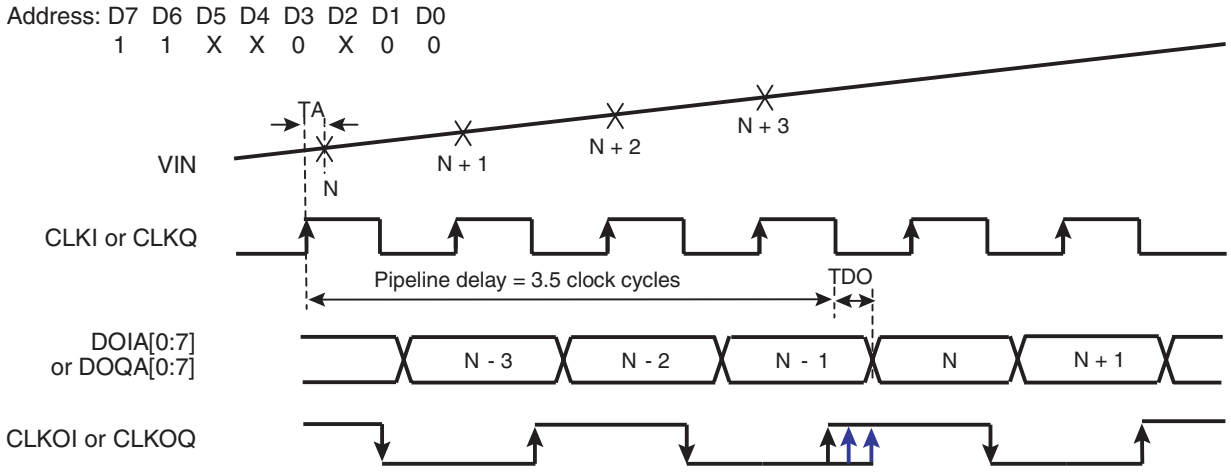
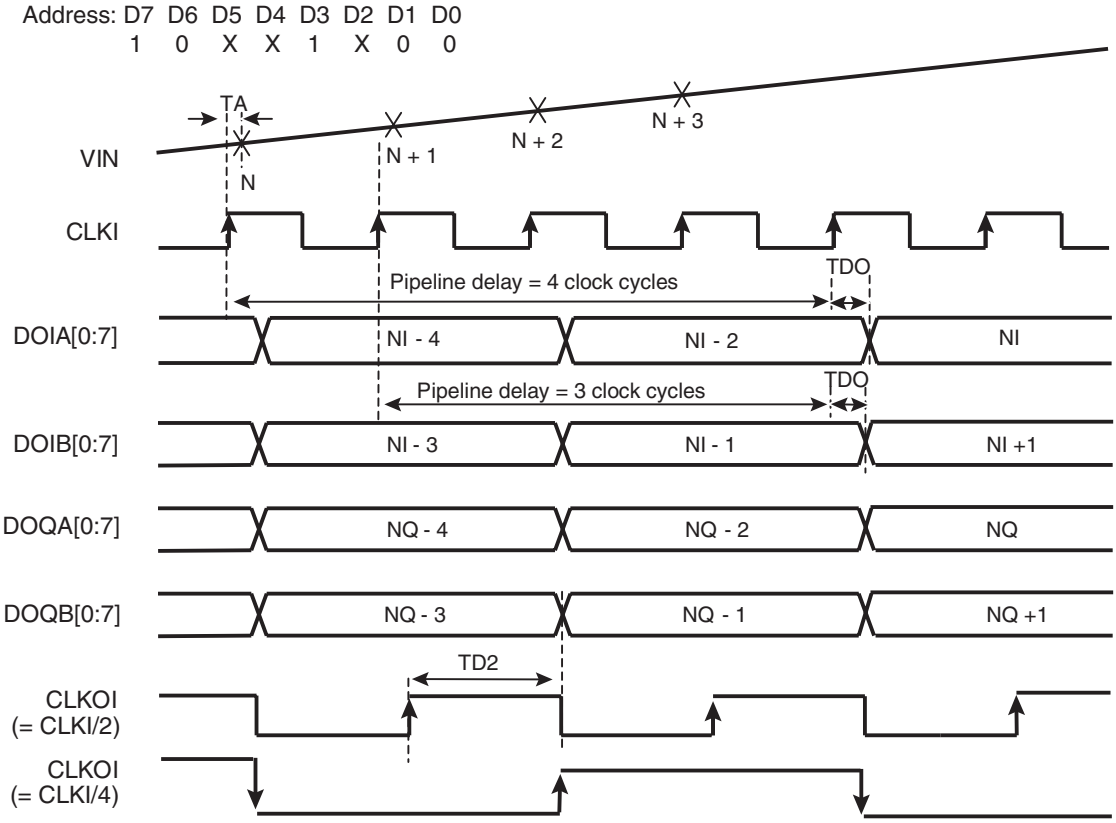


Figure 3-2. 1:1 DMUX Mode, Clock I = ADC I, Clock Q = ADC Q



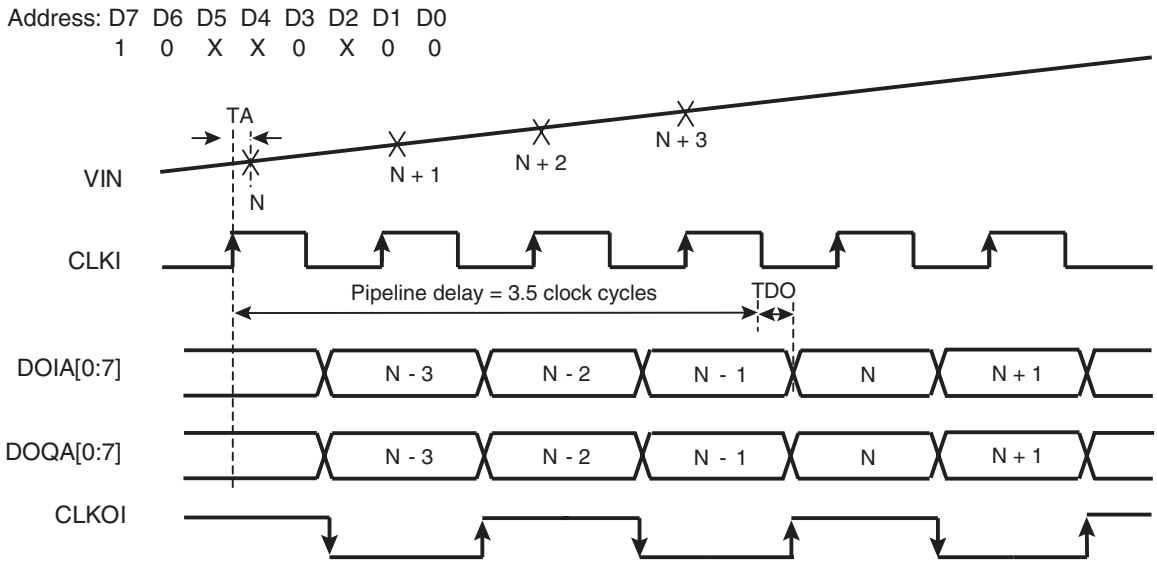
DOIB[0:7] and DOQB[0:7] are high impedance

Figure 3-3. 1:2 DMUX Mode, Clock I = ADC I, Clock I = ADC Q



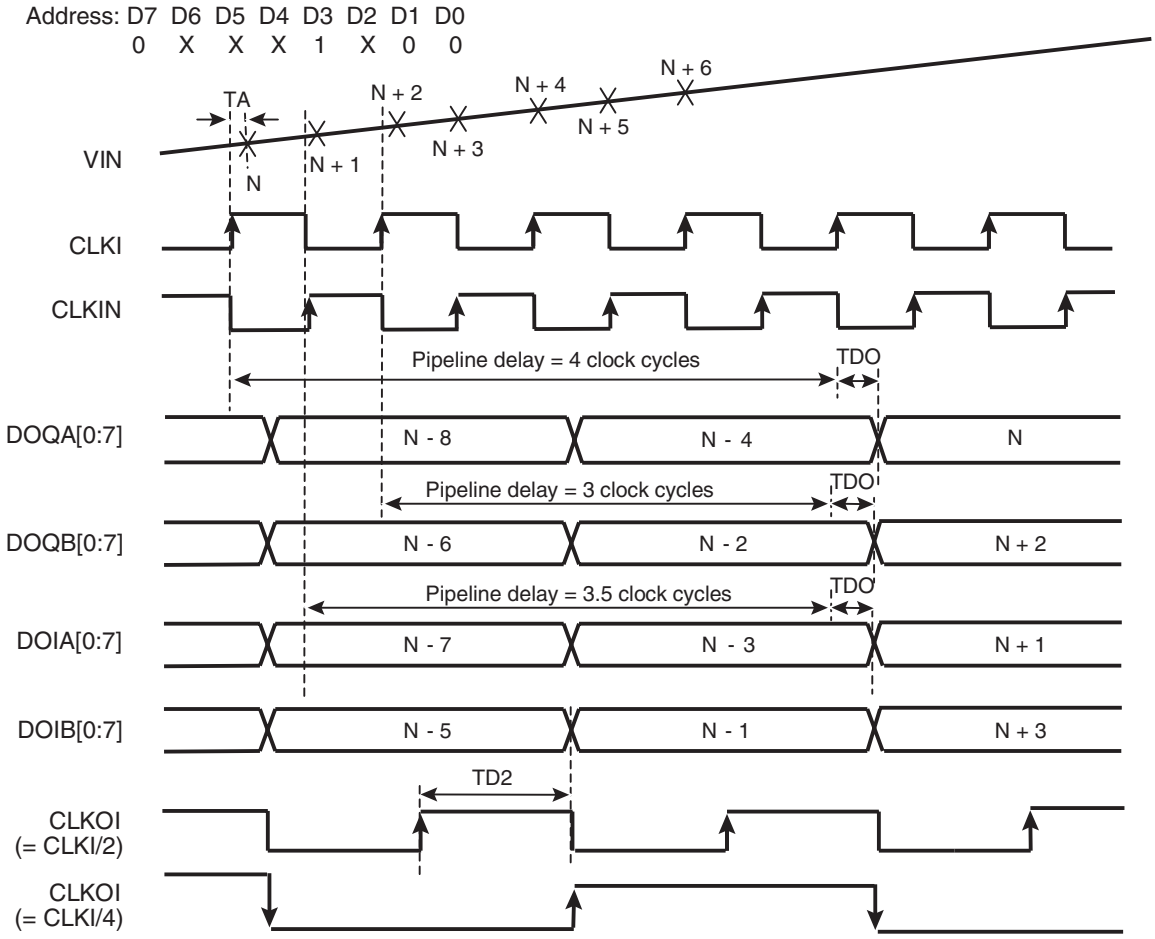
CLKOQ is high impedance

Figure 3-4. 1:1 DMUX Mode, Clock I = ADC I, Clock I = ADC Q



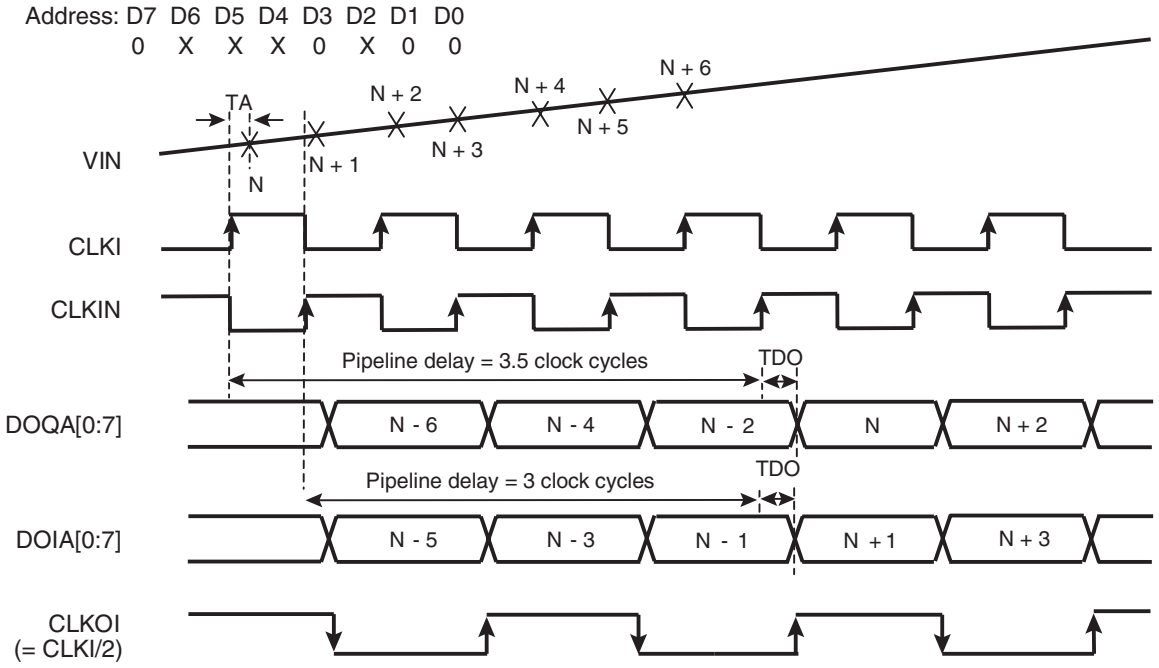
DOIB[0:7] and DOQB[0:7] are high impedance
CLKOQ is high impedance

Figure 3-5. 1:2 DMUX Mode, Clock I = ADC I, Clock IN = ADC Q



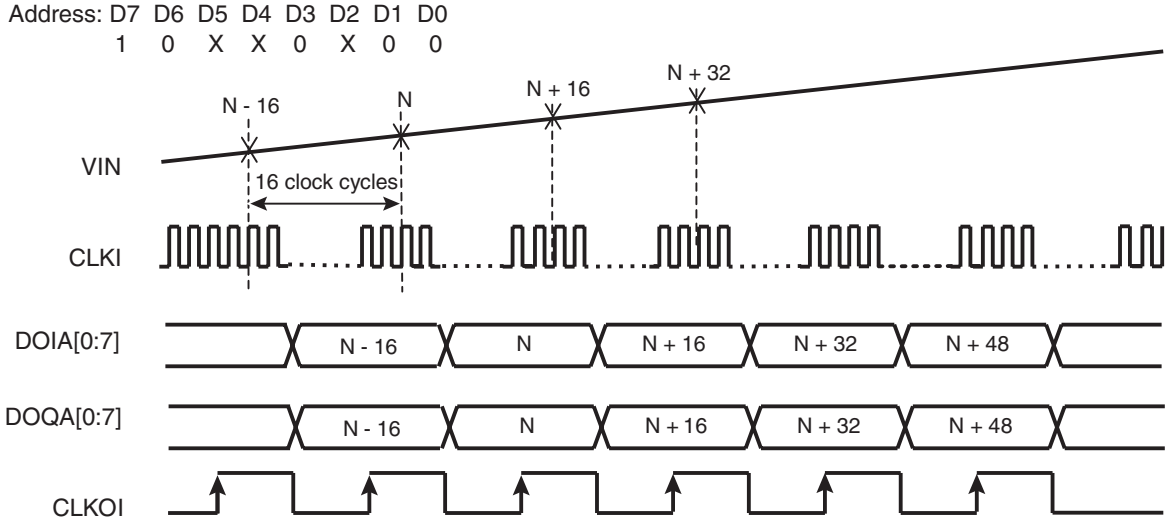
CLKOQ is high impedance

Figure 3-6. 1:1 DMUX Mode, Clock I = ADC I, Clock IN = ADC Q



DOIB[0:7] and DOQB[0:7] are high impedance
CLKOQ is high impedance

Figure 3-7. 1:1 DMUX Mode, Decimation Mode Test (1:16 Factor)



DOIB[0:7] and DOQB[0:7] are high impedance
CLKOQ is high impedance

Notes: 1. The maximum clock frequency in decimation mode is 750 Msps.
2. Frequency (CLKOI) = Frequency (Data) = Frequency (CLKI)/16.

Figure 3-8. Data Ready Reset

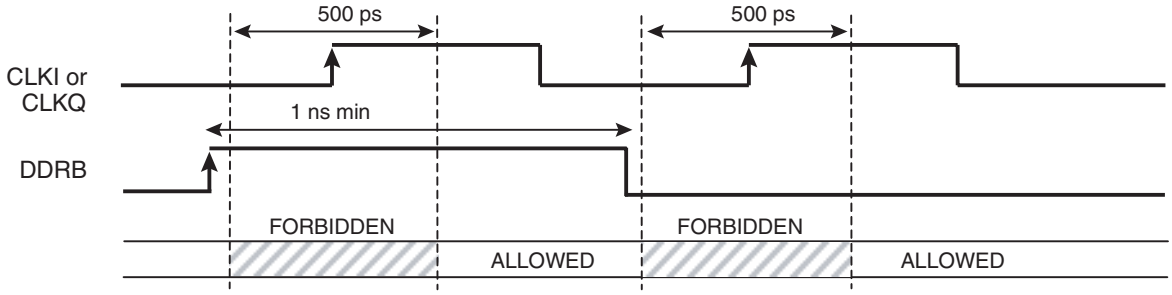
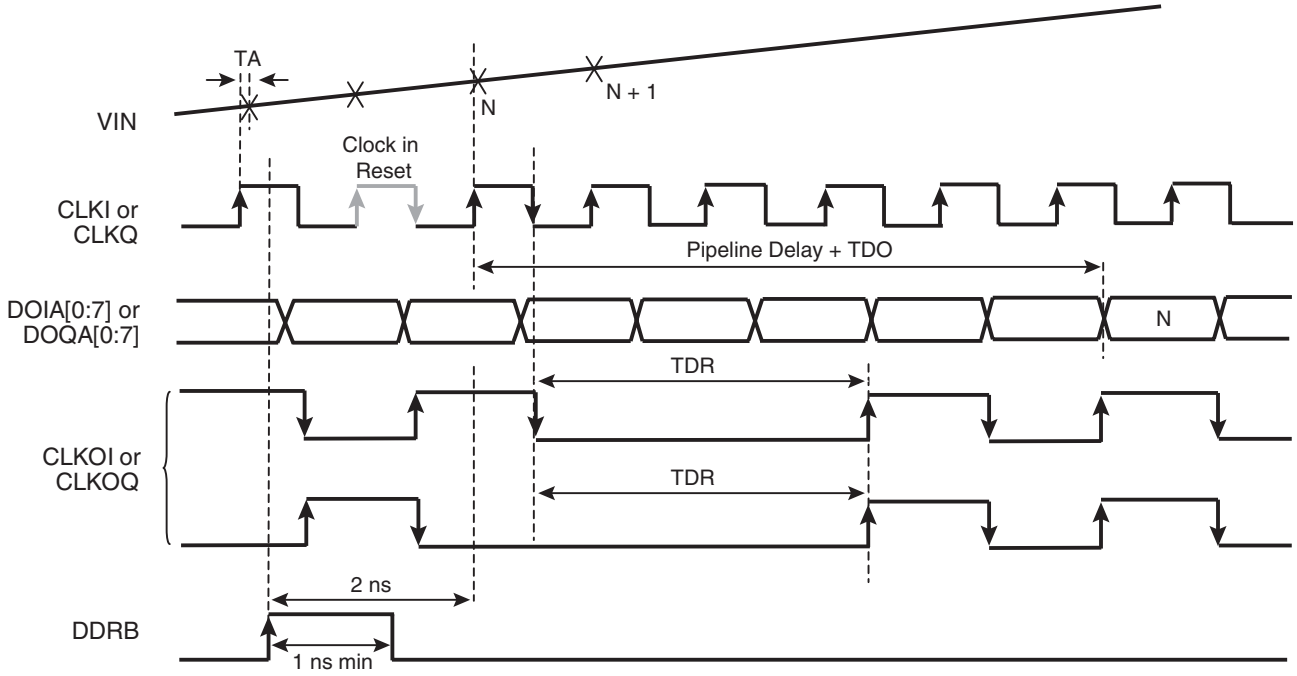
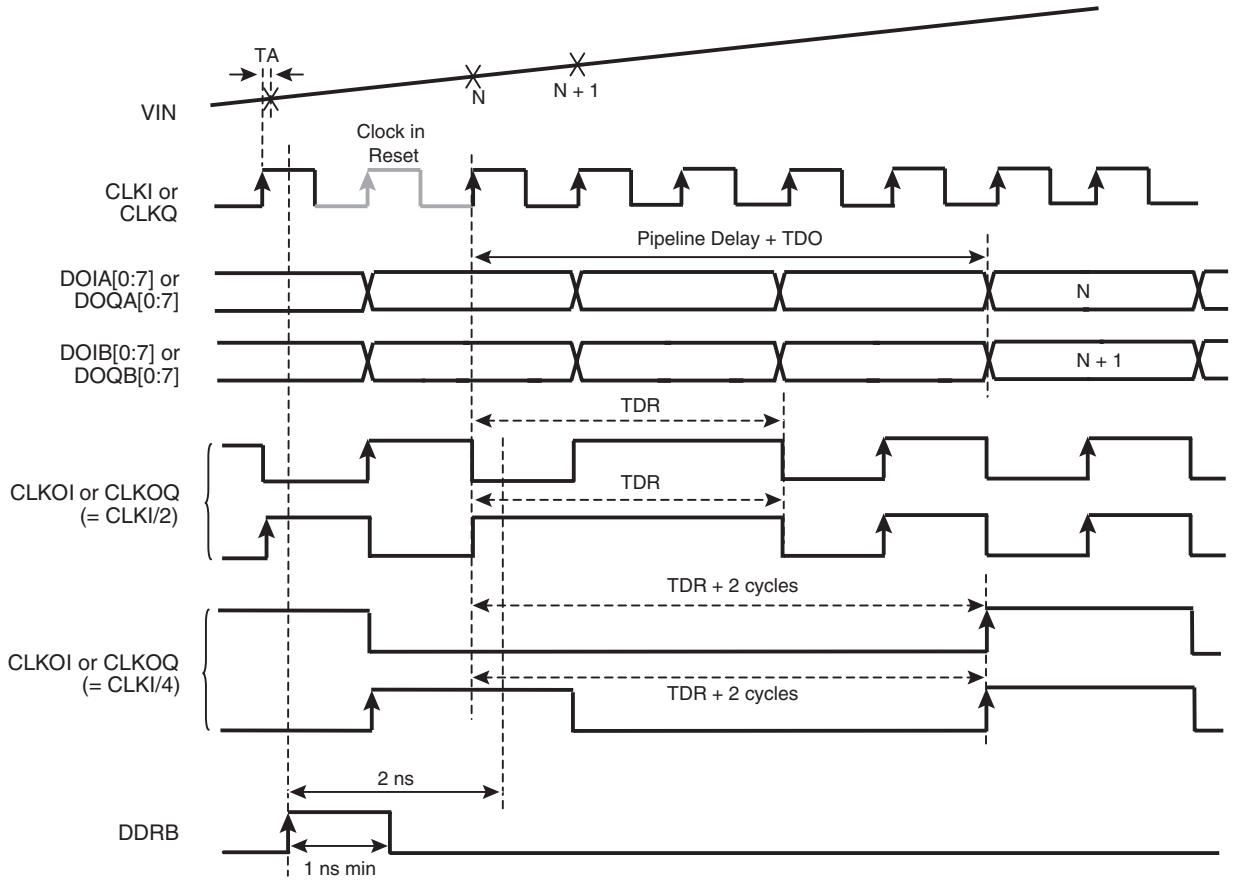


Figure 3-9. Data Ready Reset 1:1 DMUX Mode



Note: The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:1 DMUX mode). The next falling edge of the input clock after reset makes the output clock return to normal mode (after TDR).

Figure 3-10. Data Ready Reset 1:2 DMUX Mode



Notes: 1. In 1:2 DMUX, Fs/2 mode:
The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is low, it goes high only when its half cycle is complete; if the reset occurs when it is low, it remains high) and then only, remains in reset state (frozen to a high level in 1:2 DMUX Fs/2 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

2. In 1:2 DMUX, Fs/4 mode:
The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:2 DMUX Fs/4 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

3.3.2 Digital Coding

Table 3-4. Digital Output Coding (Nominal Setting)

Differential Analog Input	Voltage Level	Digital Output I or Q (Binary Coding)	Out-of-range Bit
> 250 mV	> Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1
250 mV 248mV	Positive full-scale + 1/2 LSB Positive full-scale - 1/2 LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0 0

Table 3-4. Digital Output Coding (Nominal Setting) (Continued)

Differential Analog Input	Voltage Level	Digital Output I or Q (Binary Coding)	Out-of-range Bit
1 mV -1 mV	Bipolar zero + 1/2 LSB Bipolar zero - 1/2 LSB	1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	0 0
-248 mV -250 mV	Negative full-scale + 1/2 LSB Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
< -250 mV	< Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 0	1

3.4 Test and Control Features

3.4.1 3-wire Serial Interface Control Settings

Table 3-5. Control Settings

Mode	Characteristics
MODE = 1 (2.25V)	3-wire serial bus interface activated
MODE = 0 (0V)	3-wire serial bus interface inactivated Nominal setting: Dual channel I and Q activated One clock I 0 dB gain DEMUX mode 1:1 DRDA I & Q = 0 ps ISA I & Q = 0 ps FiSDA Q = 0 ps Binary output Decimation test mode OFF Calibration setting OFF Data Ready = Fs /2

3.4.2 3-wire Serial Interface Address and Data Description

This 3-wire bus is activated with the control bit Mode equal to 1. The length of the word is 19 bits: 16 for the data and 3 for the address. The maximum clock frequency is 50 Msps.

Table 3-6. 3-wire Serial Interface Address Setting Description

Address	Setting
000	**Standby** Gray/binary mode 1:1 or 1:2 DEMUX mode Analog input MUX Clock selection Auto-calibration Decimation test mode Data Ready Delay Adjust
001	**Analog gain adjustment** Data7 to Data0: gain channel I Data15 to Data8: gain channel Q Code 00000000: -1.5 dB Code 10000000: 0 dB Code 11111111: 1.5 dB Steps: 0.011 dB
010	**Offset compensation** Data7 to Data0: offset channel I Data15 to Data8: offset channel Q Data7 and Data15: sign bits Code 11111111b: 31.75 LSB Code 10000000b: 0 LSB Code 00000000b: 0 LSB Code 01111111b: -31.75 LSB Steps: 0.25 LSB Maximum correction: ±31.75 LSB
011	**Gain compensation** Data6 to Data0: channel I/Q (Q is matched to I) Code 11111111b: -0.315 dB Code 10000000b: 0 dB Code 0000000b: 0 dB Code 0111111b: 0.315 dB Steps: 0.005 dB Data6: sign bit
100	**Internal Settling Adjustment (ISA)** Data2 to Data0: channel I Data5 to Data3: channel Q Data15 to Data6: 1000010000

Table 3-6. 3-wire Serial Interface Address Setting Description (Continued)

Address	Setting
101	**Testability** Data3 to Data0 = 0000 Mode S/H transparent OFF: Data4 = 0 ON: Data4 = 1 Data7 = 0 Data8 = 0
110	**Built-In Test (BIT)** Data0 = 0 BIT Inactive Data0 = 1 BIT Active Data1 = 0 Static BIT Data1 = 1 Dynamic BIT If Data1 = 1Ports BI & BQ = Rising Ramp Ports AI & AQ = Decreasing Ramp If Data1 = 0, then Data2 to Data9 = Static Data for BIT Ports BI & BQ = Data2 to Data9 Ports AI & AQ = NOT (Data2 to Data9)
111	**Data Ready Delay Adjust (DRDA)** Data2 to Data0: clock I Data5 to Data3: clock Q Steps: 140 ps 000:-560 ps 100: 0 ps 111: 420 ps **Fine Sampling Delay Adjustment (FiSDA) on channel Q** Data10 to Data6: channel Q Steps: 5 ps Data4: sign bit Code 11111: -64 ps Code 10000: 0 ps Code 00000: 0 ps Code 01111: 120 ps

Notes:
1. The Internal Settling Adjustment could change independently of the two analog sampling times (TA channels I and Q) of the sample/hold (with a fixed digital sampling time) with steps of ±50 ps:
   Nominal mode will be given by Data2…Data0 = 100 or Data5…Data3 = 100.
   Data5…Data3 = 000 or Data2…Data0 = 000: sampling time is -200 ps compared to nominal.
   Data2…Data0 = 111 or Data5…Data3 = 111: sampling time is 150 ps compared to nominal.
   We recommend setting the ISA to -50 ps to optimize the ADC's dynamic performances.
2. The Fine Sampling Delay Adjustment enables you to change the sampling time (steps of ±5 ps) on channel Q more precisely, particularly in the interleaved mode.
3. A Built-In Test (BIT) function is available to rapidly test the device's I/O by either applying a defined static pattern to the dual ADC or by generating a dynamic ramp at the output of the dual ADC. This function is controlled via the 3-wire bus interface at the address 110. The maximum clock frequency in dynamic BIT mode is 750 Msps.
   Please refer to "Built-In Test" on page 19 of this section dedicated to the description of this function for more information.
4. The decimation mode enables you to lower the output bit rate (including the output clock rate) by a factor of 16, while the internal clock frequency remains unchanged. The maximum clock frequency in decimation mode is 750 Msps.
5. The "S/H transparent" mode (address 101, Data4) enables bypassing of the ADC's track/hold. This function optimizes the ADC's performances at very low input frequencies (Fin < 50 MHz).
6. In the Gray mode, when the input signal is overflow (that is, the differential analog input is greater than 250 mV), the output data must be corrected using the output DOIR:
   If DOIR = 1: Data7 unchanged
   Data6 = 0, Data5 = 0, Data4 = 0, Data3 = 0, Data2 = 0, Data1 = 0, Data0 = 0.

Table 3-7. 3-wire Serial Interface Data Setting Description

Setting for Address: 000	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**[1]	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Full standby mode	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1	1
Standby channel I[2]	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0	1
Standby channel Q[3]	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1	0
No standby mode	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0	0
Binary output mode	X	X	X	X	X	X	0	X	X	X	X	X	X	1	X	X
Gray output mode	X	X	X	X	X	X	0	X	X	X	X	X	X	0	X	X
DEMUX 1:2 mode	X	X	X	X	X	X	0	X	X	X	X	X	1	X	X	X
DEMUX 1:1 mode	X	X	X	X	X	X	0	X	X	X	X	X	0	X	X	X
Analog selection mode Input I → ADC I Input Q → ADC Q	X	X	X	X	X	X	0	X	X	X	1	1	X	X	X	X
Analog selection mode Input I → ADC I Input I → ADC Q	X	X	X	X	X	X	0	X	X	X	1	0	X	X	X	X
Analog selection mode Input Q → ADC I Input Q → ADC Q	X	X	X	X	X	X	0	X	X	X	0	X	X	X	X	X
Clock Selection mode CLKI → ADC I CLKQ → ADC Q	X	X	X	X	X	X	0	X	1	1	X	X	X	X	X	X
Clock selection mode CLKI → ADC I CLKI → ADC Q	X	X	X	X	X	X	0	X	1	0	X	X	X	X	X	X
Clock selection mode CLKI → ADC I CLKIN → ADC Q	X	X	X	X	X	X	0	X	0	X	X	X	X	X	X	X
Decimation OFF mode	X	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X
Decimation ON mode	X	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X
Keep last calibration calculated value[4] No calibration phase	X	X	X	X	0	1	0	X	X	X	X	X	X	X	X	X
No calibration phase[5] No calibration value	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X
Start a new calibration phase	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X

Table 3-7. 3-wire Serial Interface Data Setting Description (Continued)

Setting for Address: 000	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**(1)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Control wait bit calibration(6)	X	X	a	b	X	X	0	X	X	X	X	X	X	X	X	X
In mode DEMUX 1:2 FDataReady I & Q = Fs/2	X	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X
In mode DEMUX 1:2 FDataReady I & Q = Fs/4	X	1	X	X	X	X	0	X	X	X	X	X	X	X	X	X

Notes:
1. D9 must be set to “0”
2. Mode standby channel I: use analog input I Vini, Vinib and Clocki.
3. Mode standby channel Q: use analog input Q Vinq, Vinqb and Clockq.
4. Keep last calibration calculated value - no calibration phase: D11 = 0 and D10 = 1. No new calibration is required. The values taken into account for the gain and offset are either from the last calibration phase or are default values (reset values).
5. No calibration phase - no calibration value: D11 = 0 and D10 = 0. No new calibration phase is required. The gain and offset compensation functions can be accessed externally by writing in the registers at address 010 for the offset compensation and at address 011 for the gain compensation.
6. The control wait bit gives the possibility to change the internal setting for the auto-calibration phase:
   For high clock rates (>500 Msps) use a = b = 1.
   For clock rates >250 Msps and < 500 Msps use a = 1 and b = 0.
   For clock rates >125 Msps and < 250 Msps use a = 0 and b = 1.
   For low clock rates <125 Msps use a = 0 and b = 0.

3.4.3 3-wire Serial Interface Timing Description

The 3-wire serial interface is a synchronous write-only serial interface made of three wires:

- sclk: serial clock input
- sldn: serial load enable input
- sdata: serial data input

The 3-wire serial interface gives a write-only access to as many as 8 different internal registers of up to 16 bits each. The input format is always fixed with 3 bits of register address followed by 16 bits of data. The data and address are entered with the Most Significant Bit (MSB) first.

The write procedure is fully synchronous with the rising clock edge of “sclk” and described in the write chronogram hereafter:

- “sldn” and “sdata” are sampled on each rising clock edge of “sclk” (clock cycle).
- “sldn” must be set to 1 when no write procedure is performed.
- A minimum of one rising clock edge (clock cycle) with “sldn” at 1 is required for a correct start of the write procedure.
- A write starts on the first clock cycle with “sldn” at 0. “sldn” must stay at 0 during the complete write procedure.
- During the first 3 clock cycles with “sldn” at 0, 3 bits of the register address from MSB (a[2]) to LSB (a[0]) are entered.
- During the next 16 clock cycles with “sldn” at 0, 16 bits of data from MSB (d[15]) to LSB (d[0]) are entered .

- An additional clock cycle with “sldn” at 0 is required for parallel transfer of the serial data d[15:0] into the addressed register with address a[2:0]. This gives 20 clock cycles with “sldn” at 0 for a normal write procedure.
- A minimum of one clock cycle with “sldn” returned at 1 is requested to close the write procedure and before the interface is ready for a new write procedure. Any clock cycle where “sldn” is at 1 *before* the write procedure is completed interrupts this procedure and no further data transfer to the internal registers is performed.
- Additional clock cycles with “sldn” at 0 *after* the parallel data transfer to the register (done at the 20th consecutive clock cycle with “sldn” at 0) do not affect the write procedure and are ignored.

It is possible to have only one clock cycle with sldn at 1 between two following write procedures.

- 16 bits of data must always be entered even if the internal addressed register has less than 16 bits. Unused bits (usually MSBs) are ignored. Bit signification and bit positions for the internal registers are detailed in Section 3.4.1 and Section 3.4.2.

To reset the registers, the Pin mode can be used as a reset pin for chip initialization, even when the 3-wire serial interface is used.

Figure 3-11. Write Chronogram

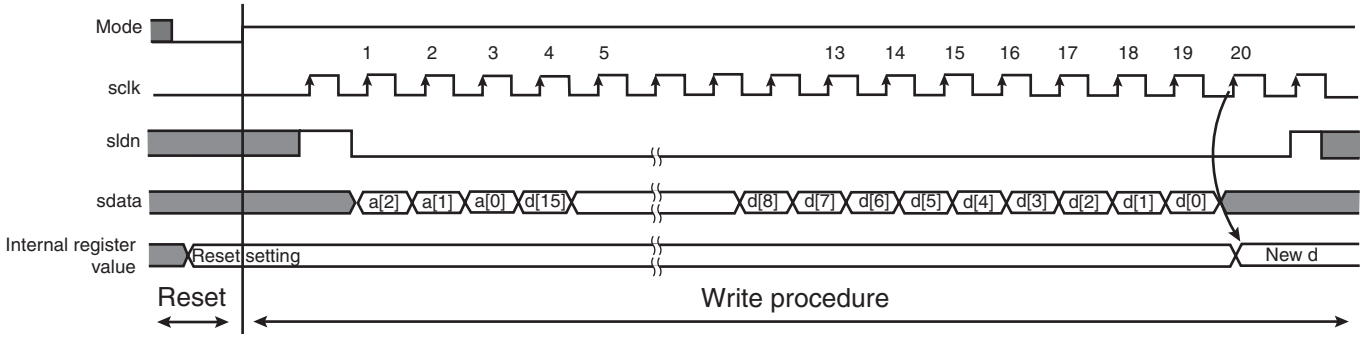


Figure 3-12. Timing Definition

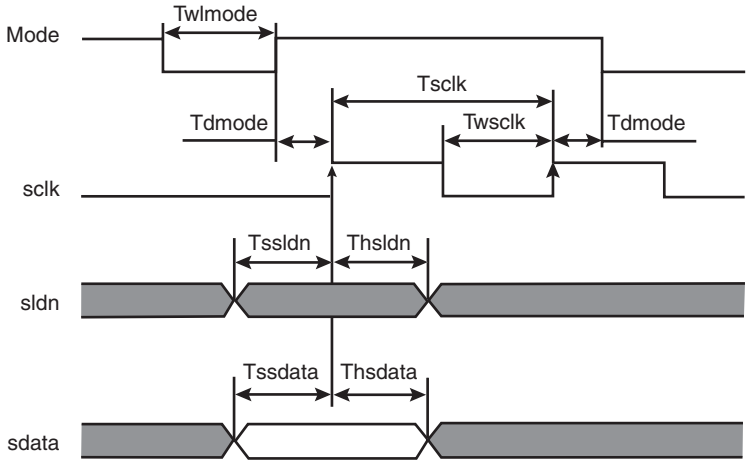


Table 3-8. Timing Description

Name	Parameter	Value			Unit
		Min	Typ	Max	
Tsclk	Period of Sclk	20			ns
Twsclk	High or low time of sclk	5			ns
Tssldn	Setup time of sldn before rising edge of sclk	4			ns
Thsldn	Hold time of sldn after rising edge of sclk	2			ns
Tssdata	Setup time of sdata before rising edge of sclk	4			ns
Thsdata	Hold time of sdata after rising edge of sclk	2			ns
Twlmode	Minimum low pulse width of mode	5			ns
Tdmode	Minimum delay between an edge of mode and the rising edge of sclk	10			ns

3.4.4 Calibration Description

The AT84AD001B offers the possibility of reducing offset and gain matching between the two ADC cores.

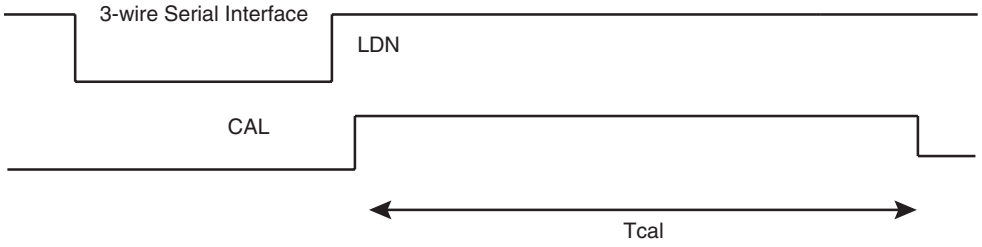
An internal digital calibration may start right after the end of the loading of the 3-wire serial interface (using data D12 of the 3-wire serial interface with address 000).

The beginning of calibration disables the two ADCs and a standard data acquisition is performed.

The output bit CAL goes to a high level during the entire calibration phase. When this bit returns to a low level, the two ADCs are calibrated with offset and gain and can be used again for a standard data acquisition .

If only one channel is selected (I or Q) the offset calibration duration is divided by two and no gain calibration between the two channels is necessary .

Figure 3-13. Internal Calibration Timing



The Tcal duration is a multiple of the clock frequency ClockI (master clock). Even if a dual clock scheme is used during calibration ClockQ will not be used.

The control wait bits (D13 and D14) give the possibility of changing the calibration's setting depending on the clock's frequency:

- For high clock rates (> 500 Msps) use a = b = 1, Tcal = 10112 clock I periods.
- For clock rates > 250 Msps and < 500 Msps use a = 1, b = 0, Tcal = 6016 clock I periods.
- For clock rates > 125 Msps and < 250 Msps use a = 0, b = 1 ,Tcal = 3968 clock I periods.

- For low clock rates (< 125 Msps) use a = 0, b = 0 , Tcal = 2944 clock I periods.

The calibration phase is necessary when using the AT84AD001B in interlace mode, where one analog input is sampled at both ADC cores on the common input clock's rising and falling edges. This operation is equivalent to converting the analog signal at twice the clock frequency.

Table 3-9. Matching Between Channels

Parameter	Value			Unit
	Min	Typ	Max	
Gain error (single channel I or Q) without calibration		0		LSB
Gain error (single channel I or Q) with calibration	-2	0	2	LSB
Offset error (single channel I or Q) without calibration		0		LSB
Offset error (single channel I or Q) with calibration	-2	0	2	LSB
Mean offset code without calibration (single channel I or Q)		127.5		
Mean offset code with calibration (single channel I or Q)	126	127.5	129	

During the ADC's auto-calibration phase, the dual ADC is set with the following:

- Decimation mode ON
- 1:1 DMUX mode
- Binary mode

Any external action applied to any signal of the ADC's registers is inhibited during the calibration phase.

3.4.5 Gain and Offset Compensation Functions

It is also possible for the user to have external access to the ADC's gain and offset compensation functions:

- Offset compensation between I and Q channels (at address 010)
- Gain compensation between I and Q channels (at address 011)

To obtain manual access to these two functions, used to set the offset to middle code 127.5 and to match the gain of channel Q with that of channel I (if only one channel is used, the gain compensation does not apply), it is necessary to set the ADC to "manual" mode by writing 0 at bits D11 and D10 of address 000.

3.4.6 Built-In Test

A Built-In Test (BIT) function is available to allow rapid testing of the device's I/O by either applying a defined static pattern to the ADC or by generating a dynamic ramp at the ADC's output. The dynamic ramp can be used with a clock frequency of up to 750 Msps. This function is controlled via the 3-wire bus interface at address 101.

- The BIT is active when Data0 = 1 at address 110.
- The BIT is inactive when Data0 = 0 at address 110.
- The Data1 bit allows you to choose between static mode (Data1 = 0) and dynamic mode (Data1 = 1).

When the static BIT is selected (Data1 = 0), it is possible to write any 8-bit pattern by defining the Data9 to Data2 bits. Port B then outputs an 8-bit pattern equal to *Data9 ... Data2* and Port A will output an 8-bit pattern equal to *NOT (Data9 ... Data2)*.

Example:

Address = 110

Data =

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	1	0	1	0	1	0	1	0	1

One should then obtain 01010101 on port B and 10101010 on port A .

When the dynamic mode is chosen (Data1 = 1) port B outputs a rising ramp while port A outputs a decreasing one.

3.4.7 Decimation Mode

The decimation mode is provided to enable rapid testing of the ADC at a maximum clock frequency of 750 Msps. In the decimation mode, one data out of 16 is output, thus leading to a maximum output rate of 46.875 Msps.

Section 4

Software Tools

4.1 Overview

The dual 8-bit evaluation user interface software is a Visual C++® compiled graphical interface that does not require a licence to run on a Windows® NT® and Windows® 2000/98/XP® PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Configuration

The advised configuration for Windows® 98 is:

- PC with Intel® Pentium® Microprocessor of over 100 MHz
- Memory of at least 24 Mo

For other versions of Windows® OS, use the recommended configuration from Microsoft®.

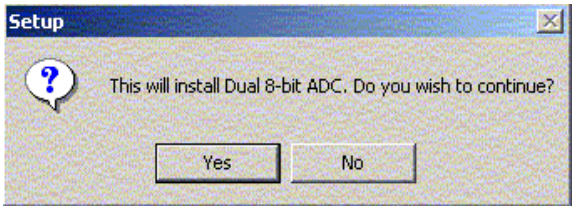
Note: Two COM ports are necessary to use two boards simultaneously.

4.3 Getting Started

1. Install the ADC dual 8-bit 1 Gsps application on your computer by launching the Dual8bitADC_2.x.x.exe installer (please refer to the latest version available).

The following window appears:

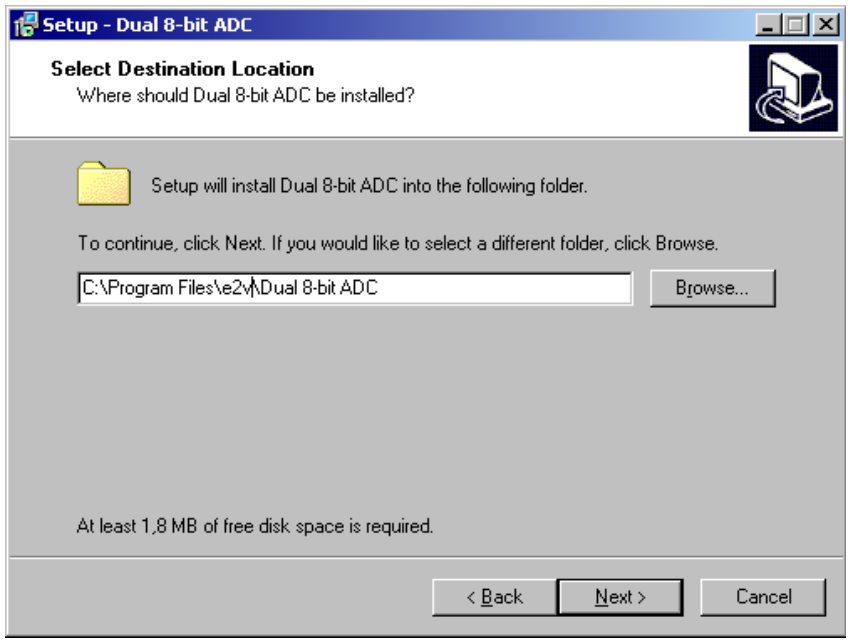
Figure 4-1. Dual 8-bit ADC Setup Window



2. Click on *Yes* to start the Dual 8-bit application.

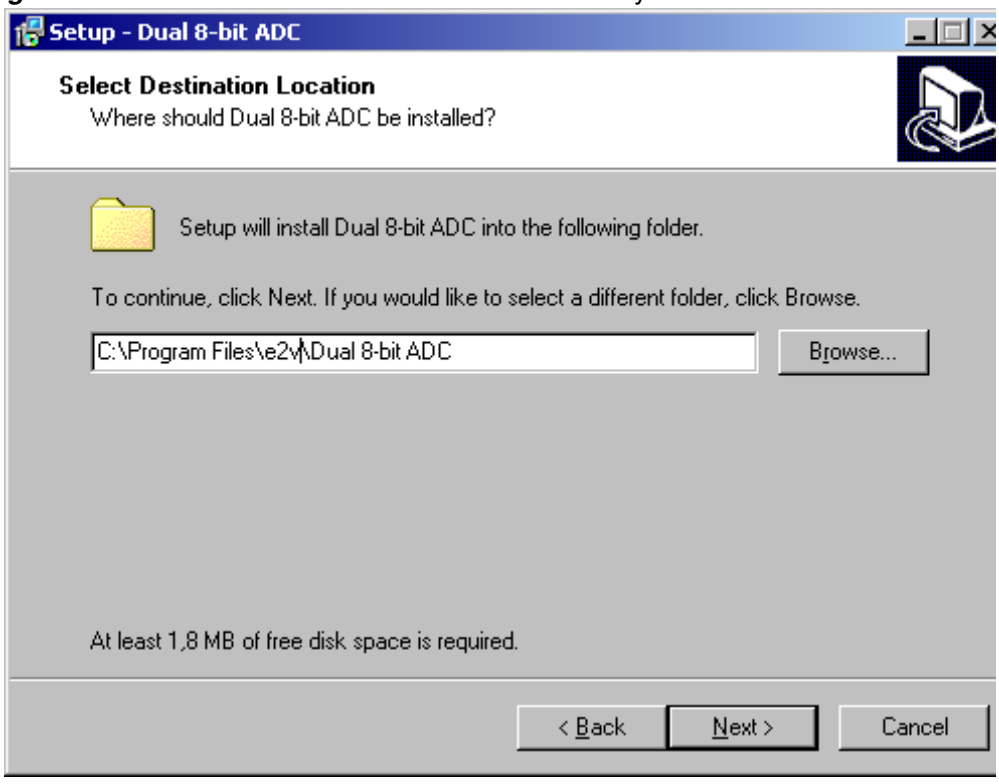
The following screen is displayed:

Figure 4-2. Dual 8-bit ADC Application Setup Wizard Window



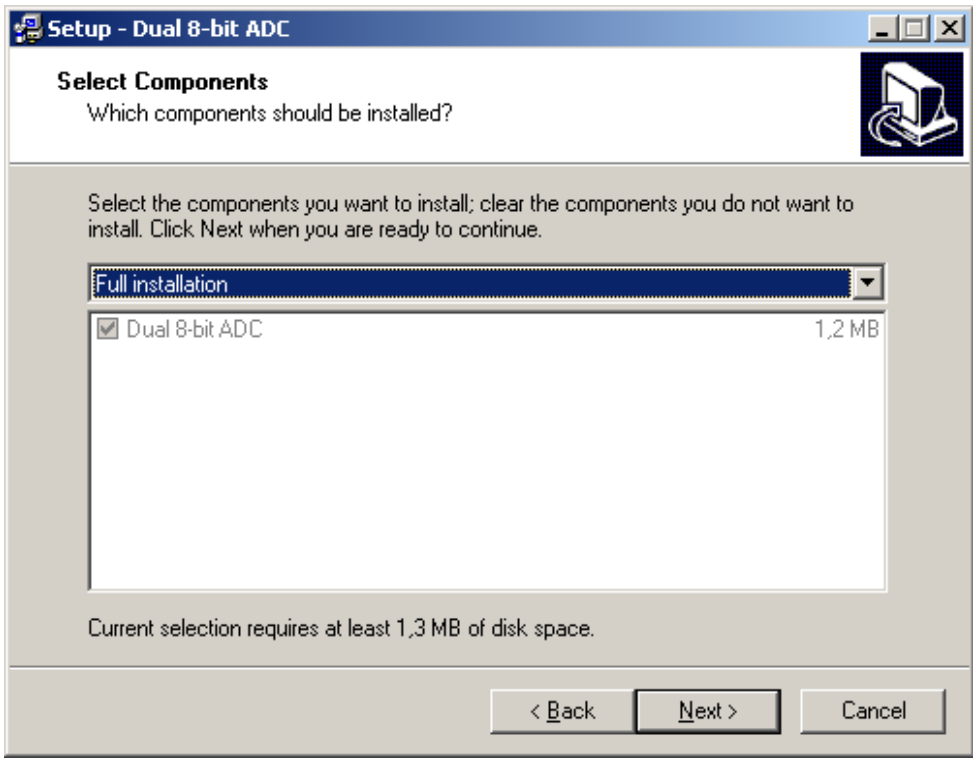
3. Select a destination directory.

Figure 4-3. Dual 8-bit ADC Select Destination Directory Window



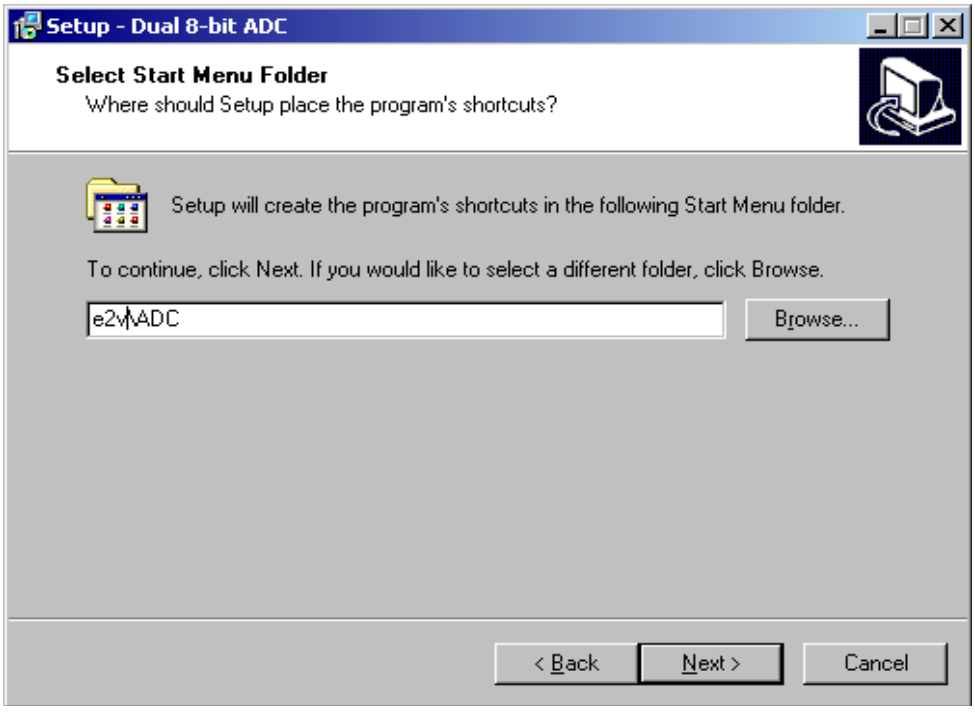
4. Select components (choose *Full installation*)

Figure 4-4. Dual 8-bit ADC Select Component Window



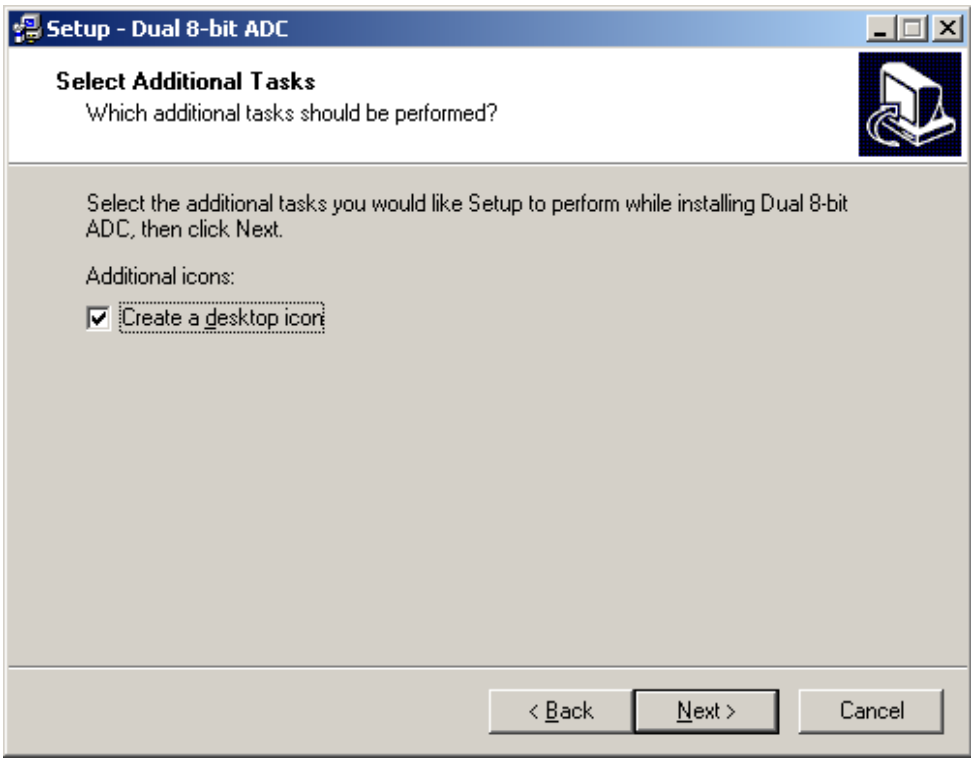
5. Select the *Start* Menu.

Figure 4-5. Dual 8-bit ADC Select Start Menu Window



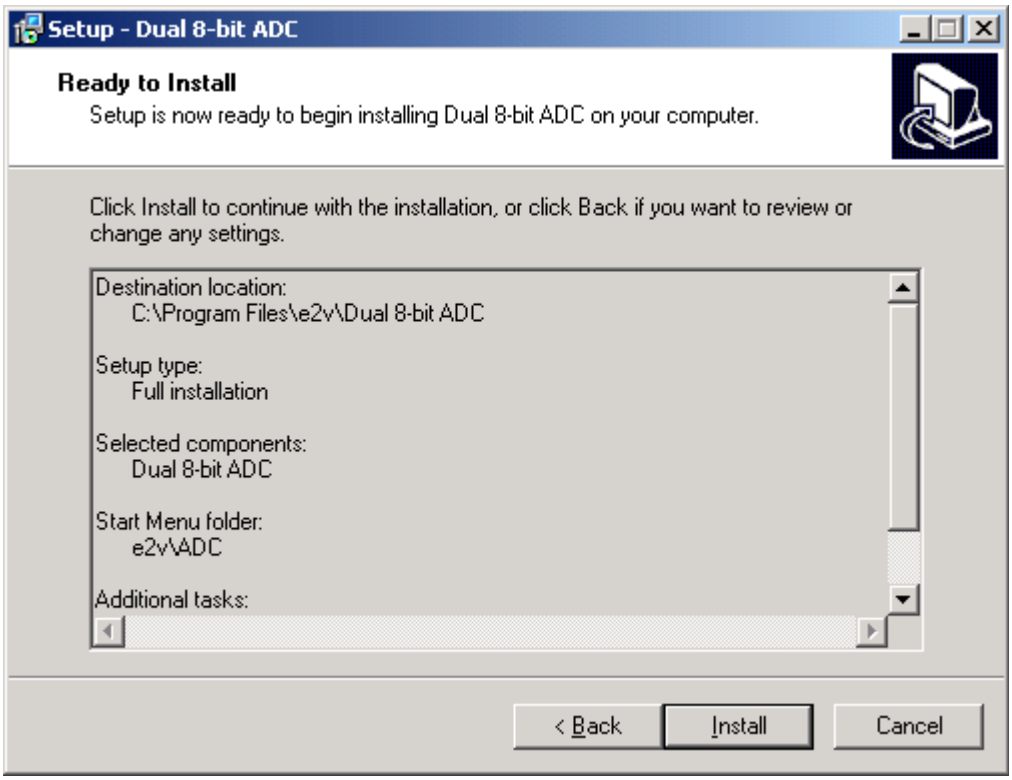
6. Select *Additional Tasks*

Figure 4-6. Dual 8-bit ADC Select Additional Tasks Window



7. Verify the installation configuration.

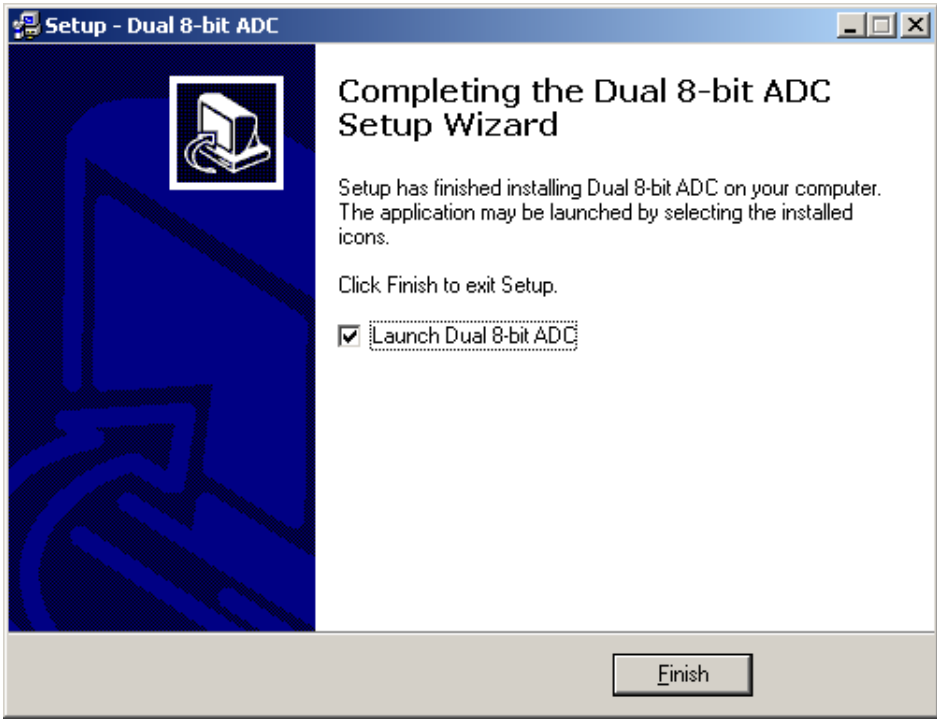
Figure 4-7. Dual 8-bit ADC Ready to Install Window



8. If you agree with the installation configuration, press the *Install* button.

The software installation is now complete.

Figure 4-8. Dual 8-bit ADC Completing Setup Wizard Window

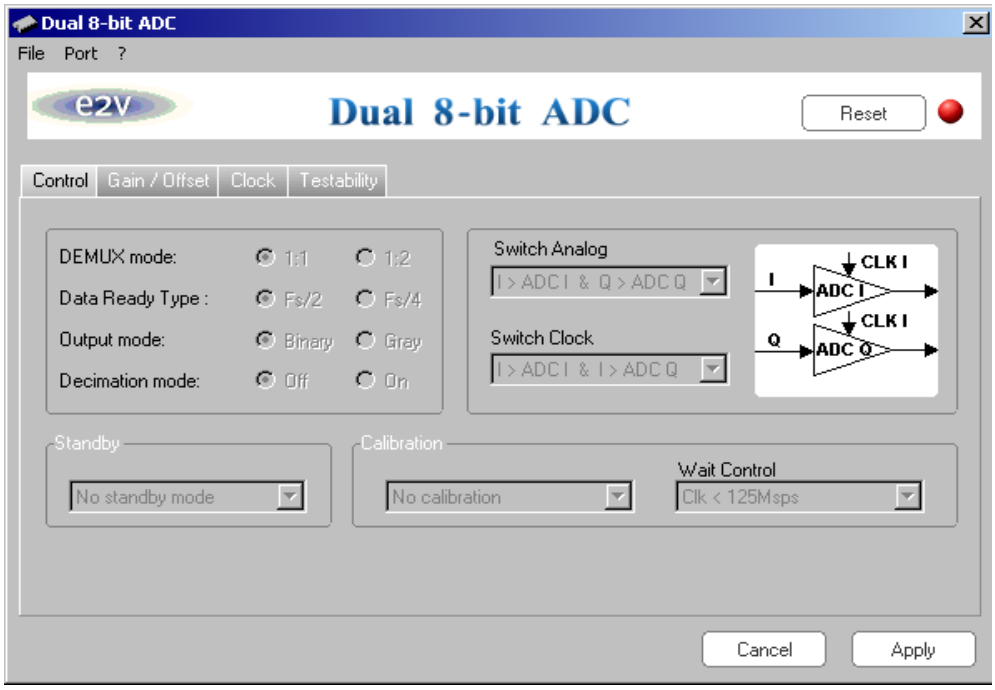


After the installation, you can launch the interface with the following file:

```
C:\Program Files\e2v\Dual 8-bit ADC\Dual8BitADC.exe
```

The window shown in Figure 4-10 is displayed.

Figure 4-9. Dual 8-bit ADC User Interface Window



Note: If the Dual 8-bit ADC Application board is not connected or not switched on, a red LED light appears to the right of the reset button as shown in Figure 4-10, and the application is grayed out.

If this is the case, you should:

– Check your connection and restart the application.
If the serial interface is not active, the LED appears orange and the application is again grayed out.

Figure 4-10. Dual 8-bit ADC User Interface Window

9. Turn ON the demo board. The application should start and the LED turns green.

Figure 4-11. Dual 8-bit ADC User Interface Window

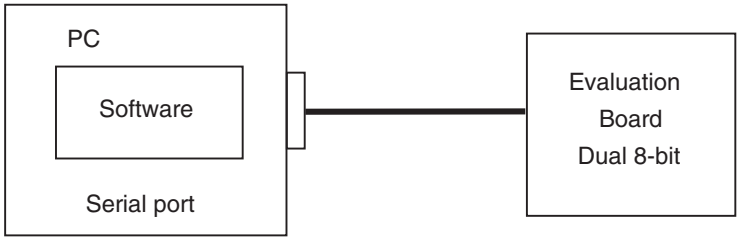
4.3.0.1 Troubleshooting

1. Check that you own rights to write in the directory.
2. Check for the available disk space.
3. Check that at least one RS-232 serial port is free and properly configured.
4. Check that the serial port and DB9 connector are properly connected.
5. Check that all supplies are properly powered on.
6. Check that the serial mode is active (green LED on).

The serial port configuration should be as follows:

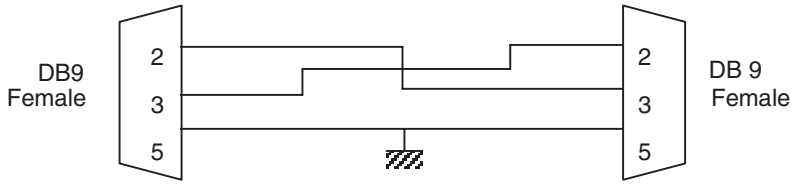
- Bit rate: 19200
- Data coding: 8 bits
- 1 start bit, 1 stop bit
- No parity check

Figure 4-12. Dual 8-bit ADC User Interface Hardware Implementation



1. Use an RS-232 port to send data to the ADC.
2. Connect the crossed DB9 (F/F) cable between your PC and your evaluation board as illustrated in Figure 4-14.

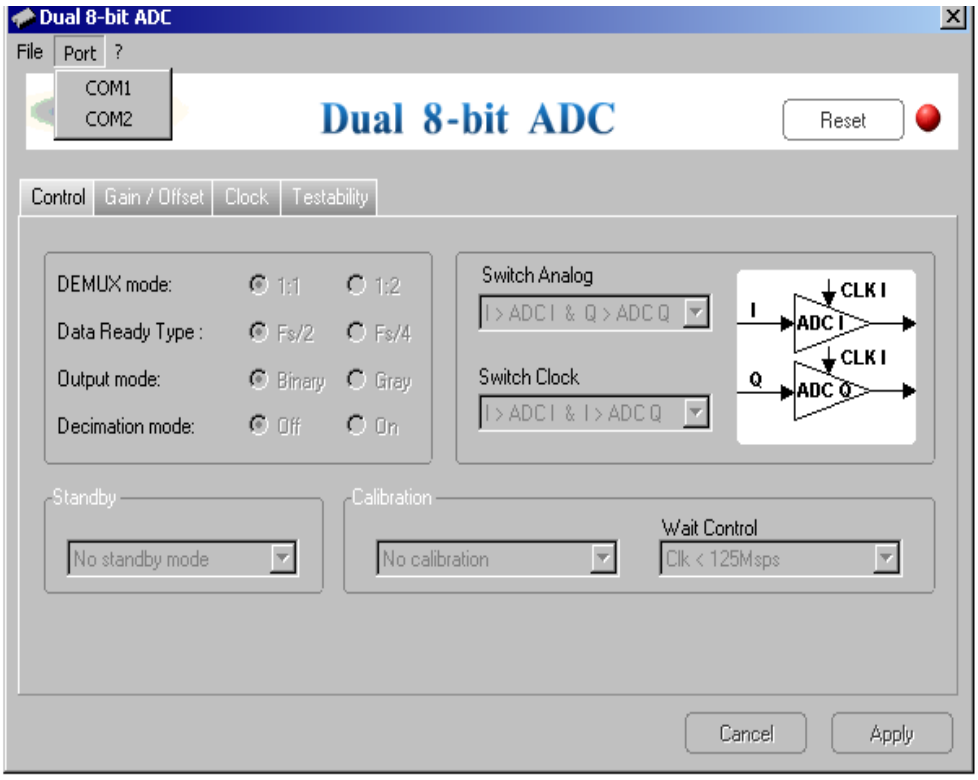
Figure 4-13. Crossed Cable



4.4 Installation Software

When the application is started, it automatically checks all RS-232 ports available on the computer and tries to find the evaluation board connected to the RS-232 port.

Figure 4-14. Dual 8-bit ADC User Interface Port Menu



The port menu shows all available ports on your computer. The port currently used has a check mark to its left. By clicking another port item, the application tries to connect to an evaluation board via the selected port. If a board is successfully detected on the new port, the LED turns green (or orange depending on the serial interface switch) and the new port becomes active. If the application is not able to find a board on this port, an error message is displayed and the LED turns red.

4.5 Operating Modes

4.5.1 Overview

The software provides a graphical user interface to configure the ADC. Push buttons, pop-up menus and capture windows enable easy activation of the following:

- Control mode
- Switch analog and switch clock
- Standby
- Calibration and wait controls
- Gain and balance controls
- Offset
- SDA balance

Always press the *Apply* button to validate a command:

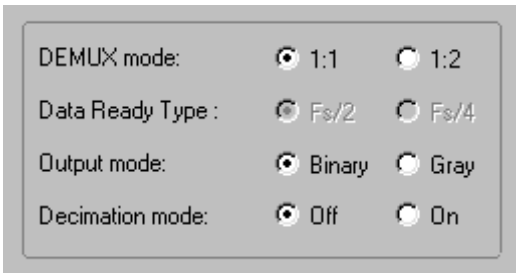
Pressing the *Cancel* button restores the last settings sent with the *Apply* button.

The *Reset* button enables re-configuration of the ADC (Mode 0):

4.5.2 Control Mode

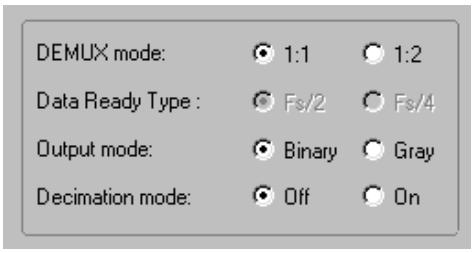
The control mode enables you to control the DEMUX, the output, the decimation and set the Data Ready Type modes. Figure 4-16 shows the normal mode configuration:

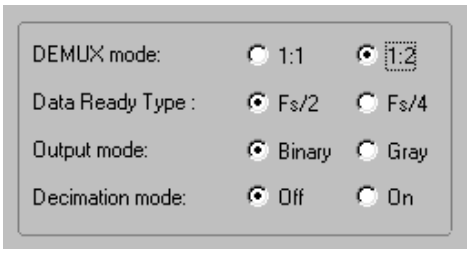
Figure 4-15. Normal Mode Configuration



4.5.3 DEMUX Mode

Figure 4-16. DEMUX Mode Configuration (1:1 or 1:2)

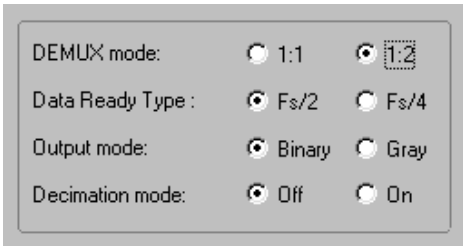


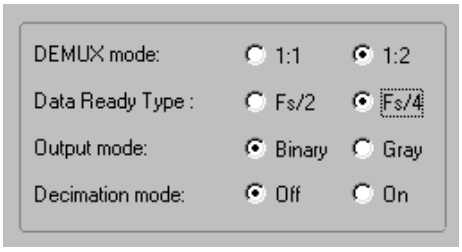


Note: In DEMUX mode 1:1, the DataReady type is fixed to Fs/2 by design.

4.5.4 Data Ready Type

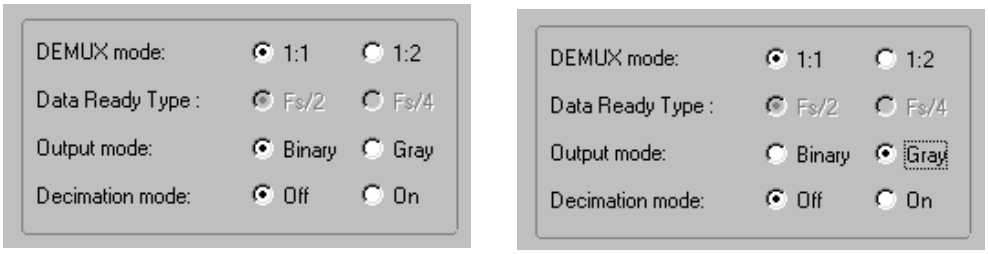
Figure 4-17. Data Ready Type Fs/2 or Fs/4





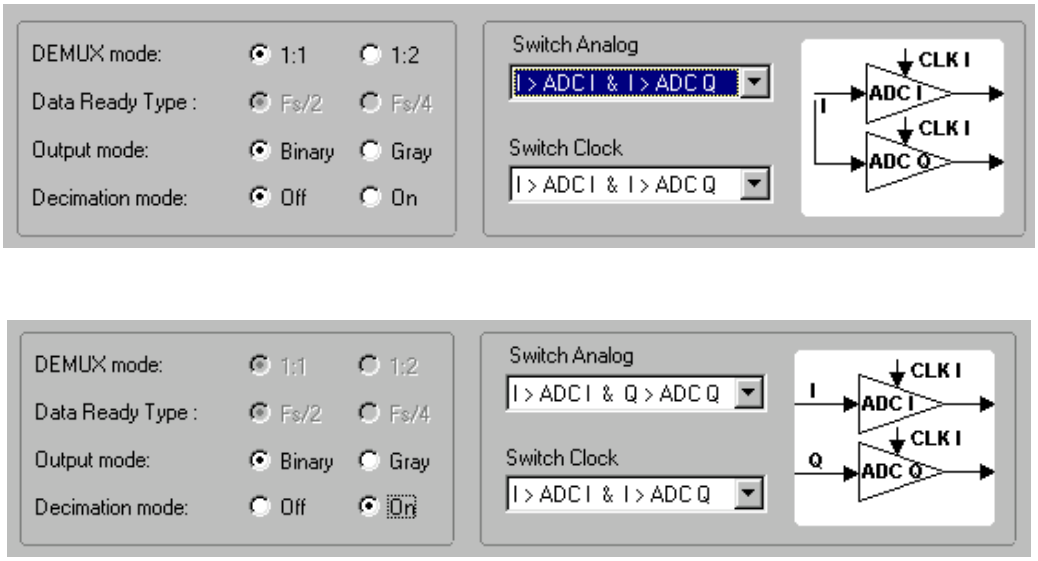
4.5.5 Output Mode

Figure 4-18. Output Mode Configurable in Binary or Gray



4.5.6 Decimation Mode

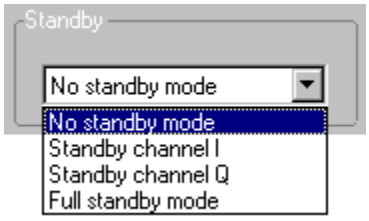
Figure 4-19. Decimation OFF or ON (Division of 16)



Note: The maximum clock frequency in Decimation mode is 750 Msps.

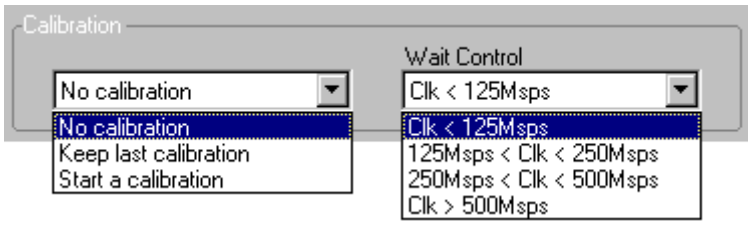
4.5.7 Standby Mode

Figure 4-20. Standby Mode Pop-up Menu



4.5.8 Calibration Mode

Figure 4-21. Calibration Mode Pop-up Menu

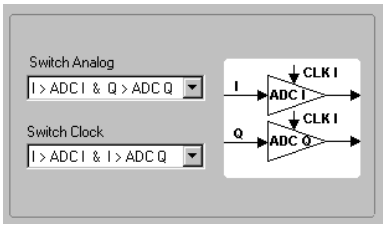


Note: Do not forget to configure the “Wait Control” parameter for a calibration phase.

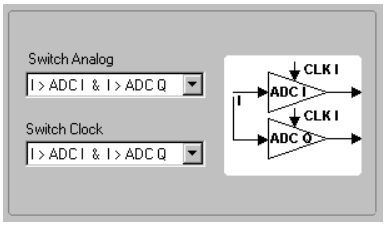
4.5.9 Analog Input Signal Selection

Figure 4-22. Switch Analog Pop-up Menus

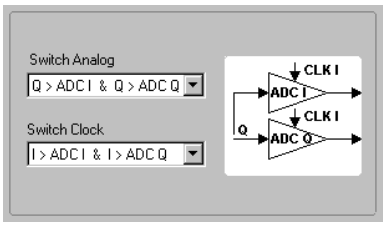
Input I > ADC I and Input Q > ADC Q (Normal Mode)



Input I > ADC I and Input I > ADC Q



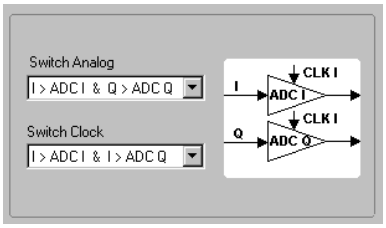
Input Q > ADC I and Input Q > ADC Q



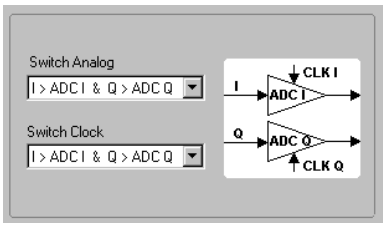
4.5.10 Clock Selection

Figure 4-23. Switch Clock Pop-up Menus

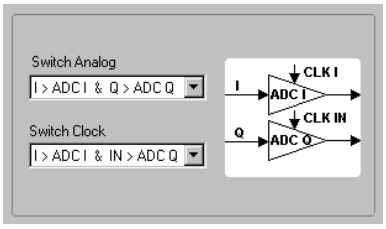
Clock I > ADC I and Clock I > ADC Q (Normal Mode)



Clock I > ADC I and Clock Q > ADC Q

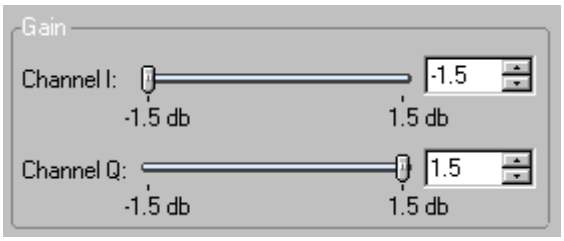


Clock I > ADC I and Clock IN > ADC Q (Interlacing Mode)



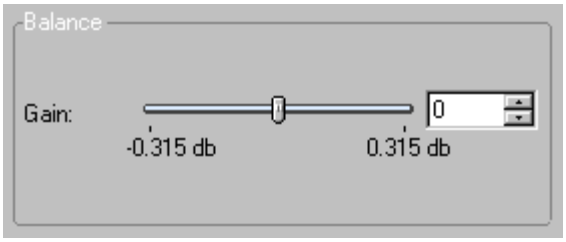
4.5.11 Gain Adjust

Figure 4-24. Gain of ADC I and ADC Q (-1.5 to 1.5 dB)



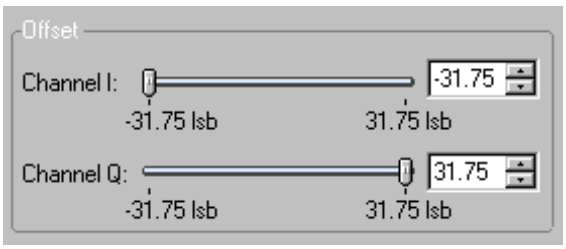
4.5.12 Gain Compensation

Figure 4-25. Gain Balance (Compensation of Channel Q) - 0.315 to 0.315 dB



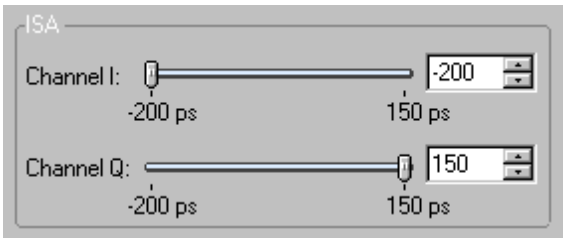
4.5.13 Offset Adjust

Figure 4-26. Offset of ADC I and ADC Q (-31.75 to 31.75 LSB)



4.5.14 Internal Setting Adjustment

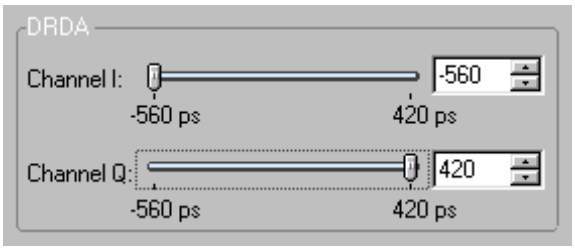
Figure 4-27. ISA of ADC I and ADC Q (-200 ps to 150 ps)



Note: We recommended setting the ISA to -50 ps to optimize the ADC's dynamic performances.

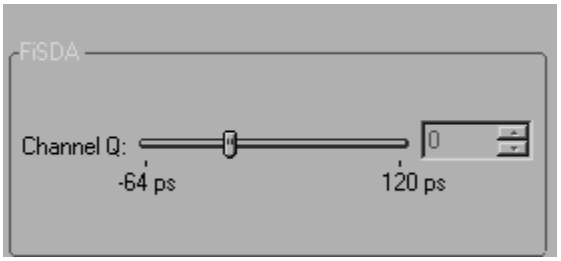
4.5.15 Data Ready Delay Adjust

Figure 4-28. DRDA of ADC I and ADC Q (-560 ps to 420 ps)



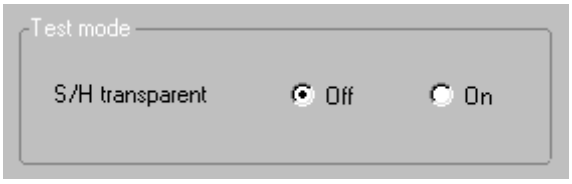
4.5.16 Fine Sampling Delay Adjust

Figure 4-29. FiSDA of ADC I and ADC Q (-64 ps to 120 ps)



4.5.17 Test Mode

Figure 4-30. Test Mode



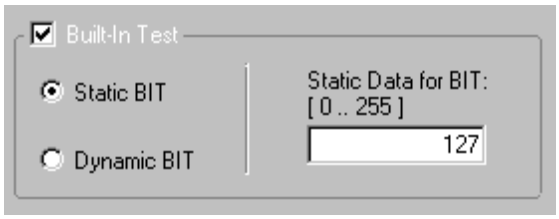
Note: This mode may be used for low input frequencies to optimize the dynamic performances (Fin <50 MHz).

4.5.18 Built-In Test

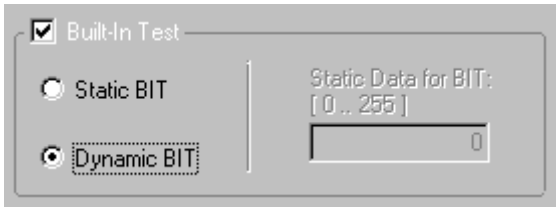
Figure 4-31. Built-in Test Configuration Windows

Built-In Test Inactive

Built-In Test Active (Static BIT)



Built-In Test Active (Dynamic BIT)



Note: The maximum clock frequency in Dynamic BIT mode is 750 Msps.

Section 5

Application Information

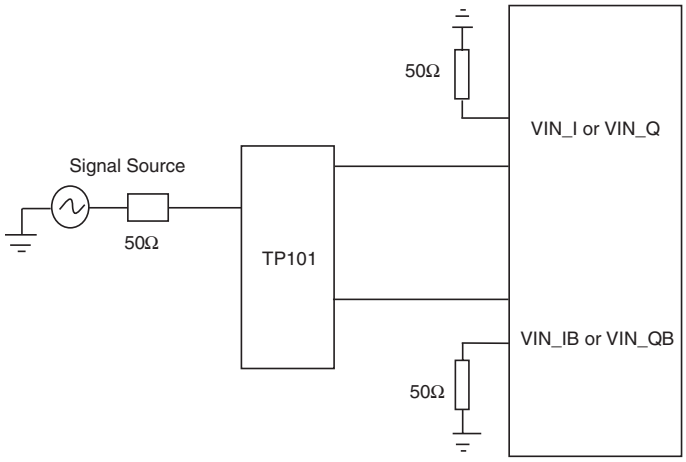
5.1 Analog Input

The analog inputs (V_{INI} or V_{INQ}) are entered in differential mode thanks to an RF transformer.

The RF transformer provides an excellent solution to convert a single-ended signal to a fully differential signal. In this example we used a TP-101 RF transformer 500 kHz - 1.5 GHz to create a differential input signal.

The analog inputs are DC coupled to ground. The transmission line must be routed to 50Ω impedance signal traces.

Figure 5-1. Analog Input Implementation



Both ADCs can convert the same analog input signal I or Q. The analog input switch is configurable via a serial interface address 000 bit 4 and bit 5.

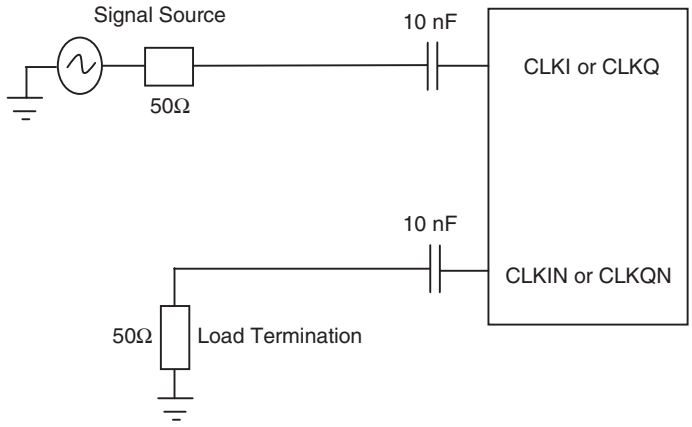
Table 5-1. Analog Input Switch Settings

Setting for Address: 000	D5	D4
Analog selection mode Input I → ADC I Input Q → ADC Q	1	1
Analog selection mode Input I → ADC I Input I → ADC Q	1	0
Analog selection mode Input Q → ADC I Input Q → ADC Q	0	X

5.2 Clock Input

The clock inputs can be entered in differential or single-ended mode with no performance degradation. The clock input signals enter in CLK (in-phase input), while pin CLKB (inverted phase) is terminated by a 50Ω load termination. The transmission lines are routed at 50Ω impedance signal traces.

Figure 5-2. Clock Input Implementation



The analog input switch is configurable via the serial interface at address 000 on bit 7 and bit 6.

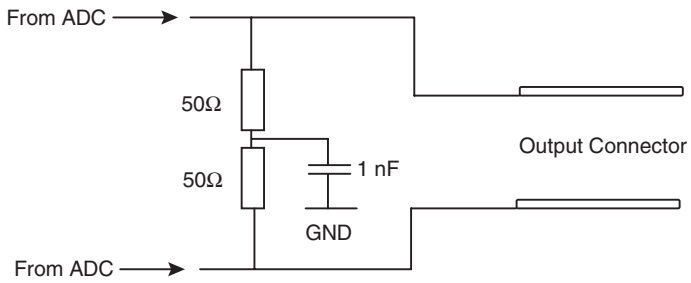
Table 5-2. Clock Input Switch Settings

Setting for Address: 000	D7	D6
Clock selection mode CLKI → ADC I CLKQ → ADC Q	1	1
Clock selection mode CLKI → ADC I CLKI → ADC Q	1	0
Clock selection mode CLKI → ADC I CLKIN → ADC Q	0	X

5.3 Data Output Termination

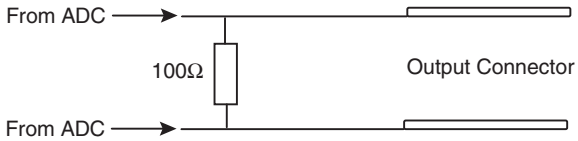
All digital outputs are 50Ω differentially terminated via a 1 nF chip capacitor, as shown in Figure 5-3.

Figure 5-3. Digital Output Termination



Note: It is possible to use a 100Ω differentially terminated output.

Figure 5-4. 100Ω Differential Digital Output Termination



The data output format is configurable via the serial interface at address 000 on bit 2.

Table 5-3. Digital Output Format Settings

Setting for Address: 000	D2
Binary output mode	1
Gray output mode	0

5.4 Control Function Settings

5.4.1 ADC Gain Adjust

The gain is adjustable via the serial interface at addresses 001 and 011. The channel I and Q gains can be configured separately using address 001 (with a variation of 1.5 dB to -1.5 dB). The channel Q gain can be configured in correlation with channel I using address 011.

Table 5-4. Analog Gain Settings

Address	Setting
011	Gain compensation Data6..Data0: channel I/Q Steps: 0.005 dB Data6: sign bit
001	Analog gain adjustment : Data7..Data0: Gain channel I Data15..Data8: Gain Channel Q Code 00000000: -1.5 dB Code 10000000: 0 dB Code 11111111: 1.5 dB Steps: 0.011 dB

5.4.2 ADC Offset Adjust

The offset can be compensated via the serial interface address 010.

The offset of channel I and Q can be configured separately.

Variation 31.75 LSB to -31.75 LSB.

Table 5-5. Offset Settings

Address	Setting
010	Offset compensation Data7..Data0 : offset channel I Data15..Data8: offset channel Q Data7 and Data15: sign bits Steps: 0.25 LSB Maximum correction: ±31.75 LSB

5.4.3 ADC Gain Compensation

The gain can be compensated via the serial interface at address 011. The gain of channel I and Q can be configured separately with a variation of -0.315 dB to +0.315 dB.

Table 5-6. Gain Compensation Settings

Address	Setting
011	Gain compensation Data6..Data0: Gain channel I/Q Code 1111111b: -0.315 dB Code 1000000b: 0 dB Code 0000000b: 0dB Code 0111111b: 0.315 dB Data6: sign bit Steps :0.005 dB

Note: This gain compensation function is used to adjust the gain of channel Q with respect to channel I.

5.4.4 ADC ISA

The Internal Settling Adjustment can independently adjust the two analog sampling times (TA channel I and Q) of the sample/hold (with a fixed digital sampling time) by steps of ±50 ps:

- The nominal mode is given by Data0/1/2 = 001 or Data3/4/5 = 001
- Data0/1/2 = Data3/4/5 = 000: sampling time - 200 ps compared to nominal
- Data0/1/2 = Data3/4/5 = 111: sampling time + 150 ps compared to nominal

Table 5-7. ISA Settings

Address	Setting
100	ISA Data2..Data0: channel I Data5..Data3: channel Q

Note: We recommend setting the ISA to -50 ps to optimize the ADC's dynamic performances.

5.4.5 Data Ready Delay Adjust

With this function, a certain delay can be added on the Data Ready signal (-560 ps to 420 ps by 140 ps steps) so that it is correctly centered on the data outputs.

Table 5-8. DRDA Settings

Address	Setting
111	Data Ready Delay Adjust Data2..Data0: output clock I Data5..Data3: output clock Q Steps: 140 ps Code 000: -560 ps Code 100: 0 ps Code 111: 420 ps

5.4.6 Fine Sampling Delay Adjust

With this function, a delay can be added on channel Q's input clock (-64 ps to 120 ps by 8 ps steps) in order to precisely adjust channel Q's sampling time. This function is particularly useful when the ADC is used in the interleaving mode (where channels I and Q have to be synchronized accurately).

Table 5-9. FiSDA Settings

Address	Setting
111	FiSDA Data10..Data6: channel Q Steps: 8 ps Code 11111: -64 ps Code 10000: 0 ps Code 00000: 0 ps Code 01111: 120 ps

5.4.7 Die Junction Temperature Monitoring

For operation in the extended temperature range, forced convection is required, to maintain the device's junction temperature below the specified maximum value (T_J max = 125°C).

A die junction temperature measurement setting has been included on the board for junction temperature monitoring.

There are two banana jack of 2 mm section, provided to source current and measure the VBE voltage across the dedicated transistor.

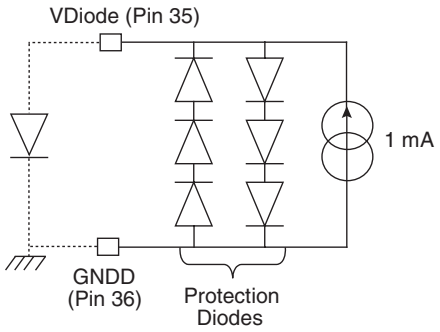
The measurement method consists of a 1 mA current flowing into a diode-mounted transistor.

Caution should be given to respecting the current source's polarity.

In any case, make sure the maximum voltage compliance of the current source is limited to a maximum of 1V or use a resistor serial-mounted with the current source to avoid damaging the transistor device (this may occur if the current source is reverse-connected).

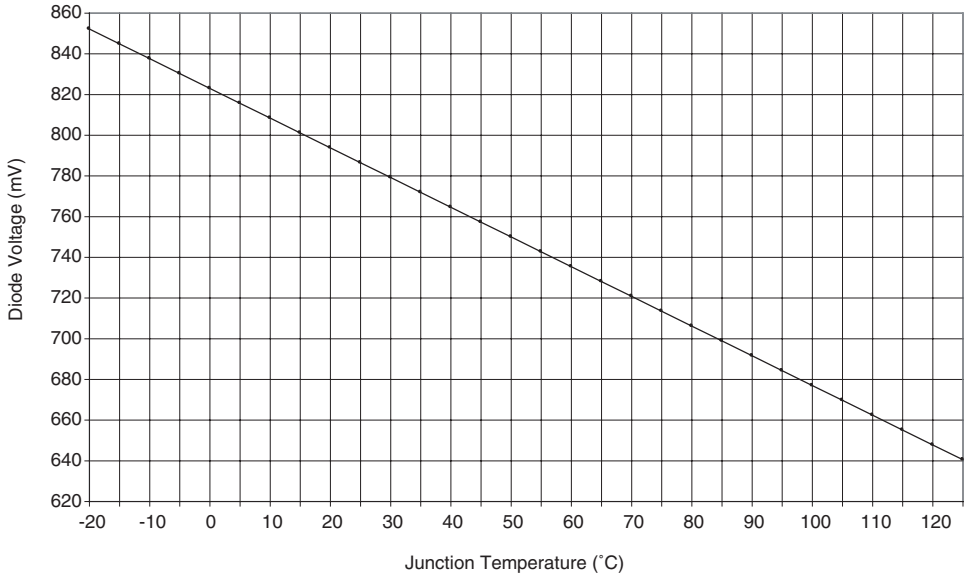
The measurement setup is described in Figure 5-5.

Figure 5-5. Die Junction Temperature Monitoring Function Implementation



The VBE diode's forward voltage in relation to the junction temperature (in steady-state conditions) is given in Figure 5-6.

Figure 5-6. Diode Characteristics Vs T_J



5.4.8 Asynchronous Data Ready Reset I and Q

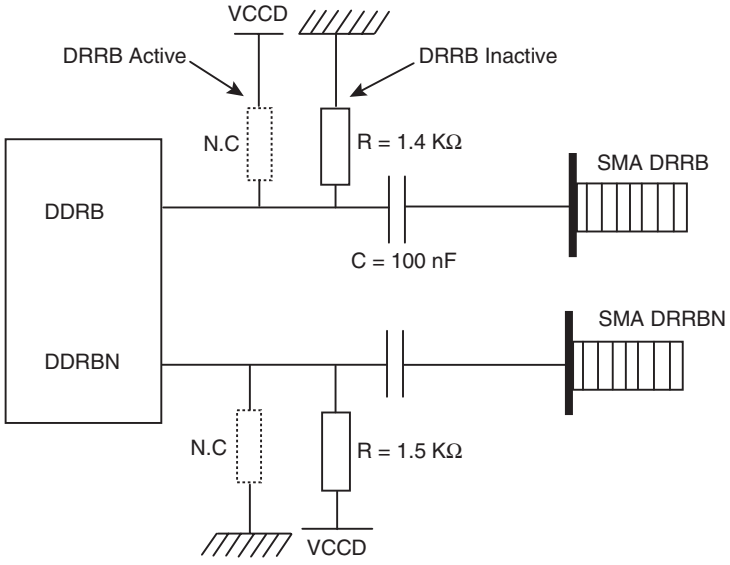
Two SMA connectors are provided for a differential DRRB command.

The Data Ready Reset command (it may be a pulse) is active on the high level.

A pull-up resistor is implemented on the evaluation board to maintain the DRRB signal inactive in normal mode.

Note: An unconnected resistor maintains the DRRB signal active (it should not be used in a normal configuration).

Figure 5-7. Data Ready Output Termination



Section 6

Ordering Information

6.1 Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84AD001BCTD	LQFP 144	*C* grade 0°C < T_{amb} < 70°C	Standard	Please contact your local sales office
AT84AD001BITD	LQFP 144	*I* grade -40°C < T_{amb} < 85°C	Standard	Please contact your local sales office
AT84AD001TD-EB	LQFP 144	Ambient	Prototype	Evaluation kit
AT84XAD001BEPW	LQFP-ep 144L green (RoHS compliant)	Ambient	Prototype	
AT84AD001BCEPW	LQFP-ep 144L green (RoHS compliant)	*C* grade 0°C < T_{amb} < 70°C	Standard	
AT84AD001BVEPW	LQFP-ep 144L green (RoHS compliant)	*V* grade -40°C < T_{amb} < 85°C	Standard	

Figure 6-1. AT84AD001B LQFP 144 Pinout (Top View)

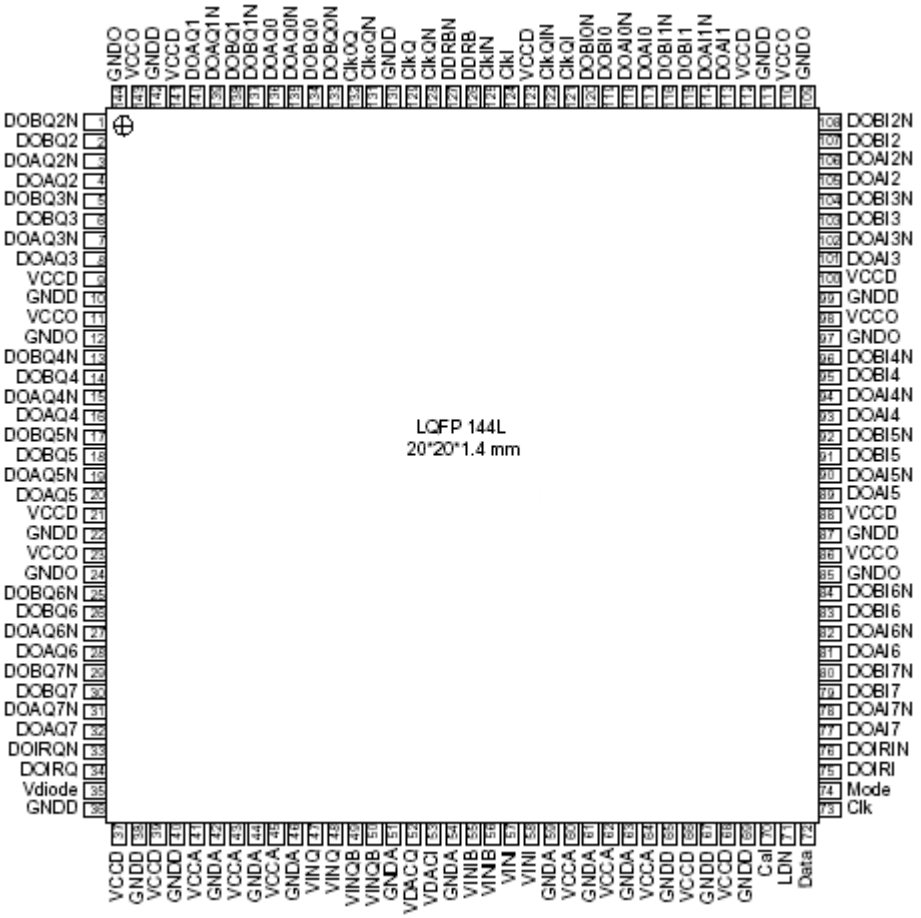


Table 6-2. AT84AD001B LQFP 144 Pin Description

Symbol	Pin number	Function
GNDA, GNDD, GNDO	10, 12, 22, 24, 36, 38, 40, 42, 44, 46, 51, 54, 59, 61, 63, 65, 67, 69, 85, 87, 97, 99, 109, 111, 130, 142, 144	Ground pins. To be connected to external ground plane
V_{CCA}	41, 43, 45, 60, 62, 64	Analog positive supply: 3.3V typical
V_{CCD}	9, 21, 37, 39, 66, 68, 88, 100, 112, 123, 141	3.3V digital supply
V_{CCO}	11, 23, 86, 98, 110, 143	2.25V output supply
V_{INI}	57, 58	In-phase (+) analog input signal of the sample & hold differential preamplifier channel I
V_{INIB}	55, 56	Inverted phase (-) of analog input signal (V_{INI})
V_{INQ}	47, 48	In-phase (+) analog input signal of the sample & hold differential preamplifier channel Q
V_{INQB}	49, 50	Inverted phase (-) of analog input signal (V_{INQ})

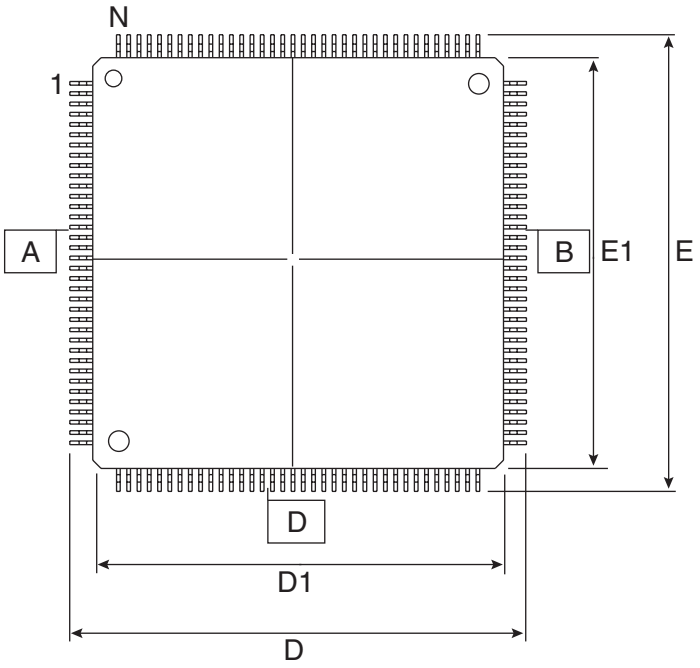
Table 6-2. AT84AD001B LQFP 144 Pin Description (Continued)

Symbol	Pin number	Function
CLKI	124	In-phase (+) PECL clock input signal. The analog input I is sampled and held on the rising edge of the CLKI signal
CLKIN	125	Inverted phase (-) of PECL clock input signal (CLKI)
CLKQ	129	In-phase (+) PECL clock input signal. The analog input Q is sampled and held on the rising edge of the CLKI signal
CLKQN	128	Inverted phase (-) of PECL clock input signal (CLKQ)
DDRB	126	Synchronous data ready reset I and Q
DDRBN	127	Inverted phase (-) of input signal (DDRB)
DOAI0, DOAI1, DOAI2, DOAI3, DOAI4, DOAI5, DOAI6, DOAI7	117, 113, 105, 101, 93, 89, 81, 77	In-phase (+) digital outputs first phase demultiplexer (channel I) DOAI0 is the LSB. D0AI7 is the MSB
DOAI0N, DOAI1N, DOAI2N, DOAI3N, DOAI4N, DOAI5N, DOAI6N, DOAI7N,	118, 114, 106, 102, 94, 90, 82, 78	Inverted phase (-) digital outputs first phase demultiplexer (channel I) DOAI0N is the LSB. D0AI7N is the MSB
DOBI0, DOBI1, DOBI2, DOBI3, DOBI4, DOBI5, DOBI6, DOBI7	119, 115, 107, 103, 95, 91, 83, 79	In-phase (+) digital outputs second phase demultiplexer (channel I) DOBI0 is the LSB. D0BI7 is the MSB
DOBI0N, DOBI1N, DOBI2N, DOBI3N, DOBI4N, DOBI5N, DOBI6N, DOBI7N	120, 116, 108, 104, 96, 92, 84, 80	Inverted phase (-) digital outputs second phase demultiplexer (channel I) DOBI0N is the LSB. D0BI7N is the MSB
DOAQ0, DOAQ1, DOAQ2, DOAQ3, DOAQ4, DOAQ5, DOAQ6, DOAQ7	136, 140, 4, 8, 16, 20, 28, 32	In-phase (+) digital outputs first phase demultiplexer (channel Q) DOAI0 is the LSB. D0AQ7 is the MSB
DOAQ0N, DOAQ1N, DOAQ2N, DOAQ3N, DOAQ4N, DOAQ5N, DOAQ6N, DOAQ7N	135, 139, 3, 7, 15, 19, 27, 31	Inverted phase (-) digital outputs first phase demultiplexer (channel Q) DOAI0N is the LSB. D0AQ7N is the MSB
DOBQ0, DOBQ1, DOBQ2, DOBQ3, DOBQ4, DOBQ5, DOBQ6, DOBQ7	134, 138, 2, 6, 14, 18, 26, 30	In-phase (+) digital outputs second phase demultiplexer (channel Q) DOBQ0 is the LSB. D0BQ7 is the MSB
DOBQ0N, DOBQ1N, DOBQ2N, DOBQ3N, DOBQ4N, DOBQ5N, DOBQ6N, DOBQ7N	133, 137, 1 ,5, 13, 17, 25, 29	Inverted phase (-) digital outputs second phase demultiplexer (channel Q) DOBQ0N is the LSB. D0BQ7N is the MSB
DOIRI	75	In-phase (+) out-of-range bit input (I phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256
DOIRIN	76	Inverted phase of output signal DOIRI
DOIRQ	34	In-phase (+) out-of-range bit input (Q phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256
DOIRQN	33	Inverted phase of output signal DOIRQ

Table 6-2. AT84AD001B LQFP 144 Pin Description (Continued)

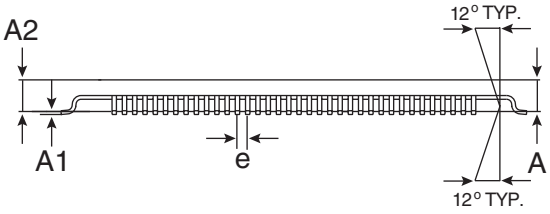
Symbol	Pin number	Function
MODE	74	Bit selection for 3-wire bus interface or nominal setting
CLK	73	Input clock for 3-wire bus interface
DATA	72	Input data for 3-wire bus
LND	71	Beginning and end of register line for 3-wire bus interface
CLKOI	121	Output clock in-phase (+) channel I, 1/2 input clock frequency
CLKOIN	122	Inverted phase (-) output clock channel I, 1/2 input clock frequency
CLKOQ	132	Output clock in-phase (+) channel Q, 1/2 input clock frequency
CLKOQN	131	Inverted phase (-) output clock channel Q, 1/2 input clock frequency
VdacI,VdacQ	52, 53	Test voltage pin for gain setting channels I and Q
Cal	70	Calibration output bit status
Vdiode	35	Positive node of diode used for die junction temperature measurements

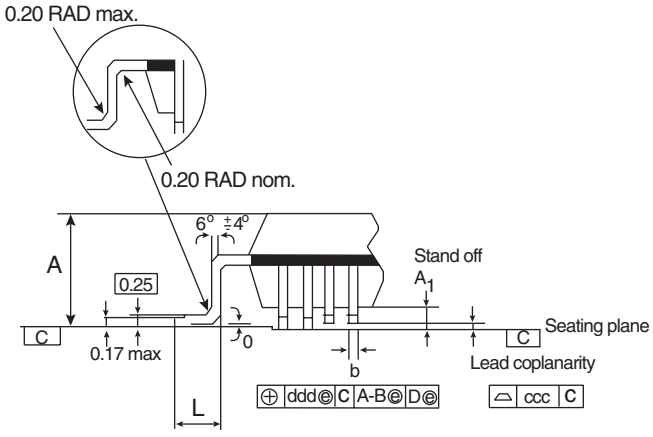
Figure 6-2. AT84AD001B LQFP 144 Package Outline Description



Body +2.00 mm footprint		
Dims.	Tols. Leads	144L
A	max.	1.60
A1		0.05 min./0.15 max.
A2	+/- 0.05	1.40
D	+/-0.20	22.00
D1	+/-0.10	20.00
E	+/-0.20	22.00
E1	+/-0.10	20.00
L	+0.15/-0.10	0.60
e	basic	0.50
b	+/-0.05	0.22
ddd		0.08
ccc	max.	0.08
o		0^o- 5^o

Notes: 1. All dimensions are in millimeters
2. Dimensions shown are nominal with tolerances as indicated
3. L/F: eftec 64T copper or equivalent
4. Foot length: "L" is measured at gauge plane at 0.25 mm above the seating plane





Section 7

Appendices

7.1 RF Pulse Transformer 500 kHz/1.5 GHz TP101: M/A-COM

The RF pulse transformer features 50Ω of either unbalanced or balanced impedance along with a fast rise time of 0.18 ns.

Additionally, it features a low insertion loss of 0.4 dB (typical) and the TP-101 PIN model is available in a flatpack package.

The following tables specify the guaranteed specification and operating characteristics.

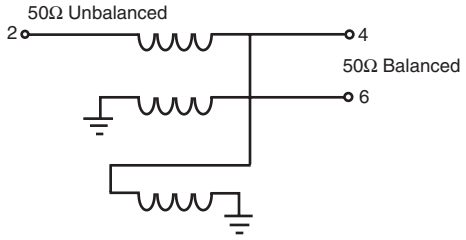
Table 7-1. TP-101 Guaranteed Specification (from -55°C to +85°C)

Feature	Value
Frequency range (1 dB bandwidth)	500 kHz/1.5GHz
Input impedance	50Ω unbalanced
Output impedance	50Ω balanced
Insertion loss 10/50 MHz	0.5 dB maximum
VSWR 1 MHz/1 GHz	1.4:1 maximum
VSWR 750 kHz/1.5 GHz	1.8:1 maximum

Table 7-2. TP-101 Guaranteed Specification (from -55°C to +85°C)

Feature		Value
Input power	750 kHz/1 MHz	1.0 watt maximum
	1 MHz/5 MHz	1.5 watts maximum
	5 MHz/1.5 GHz	3.0 watts maximum
Rise time (10% to 90%)		0.18 ns typical
Droop (10%)		300 ns typical
Environmental		MIL-STD-202 screening available

Figure 7-1. TP 101 Implementation



Note: Pins 1, 3 and 5 are grounded to case.

7.2 Board Layout Schematics

Figure 7-2. Equipped Board (Top)

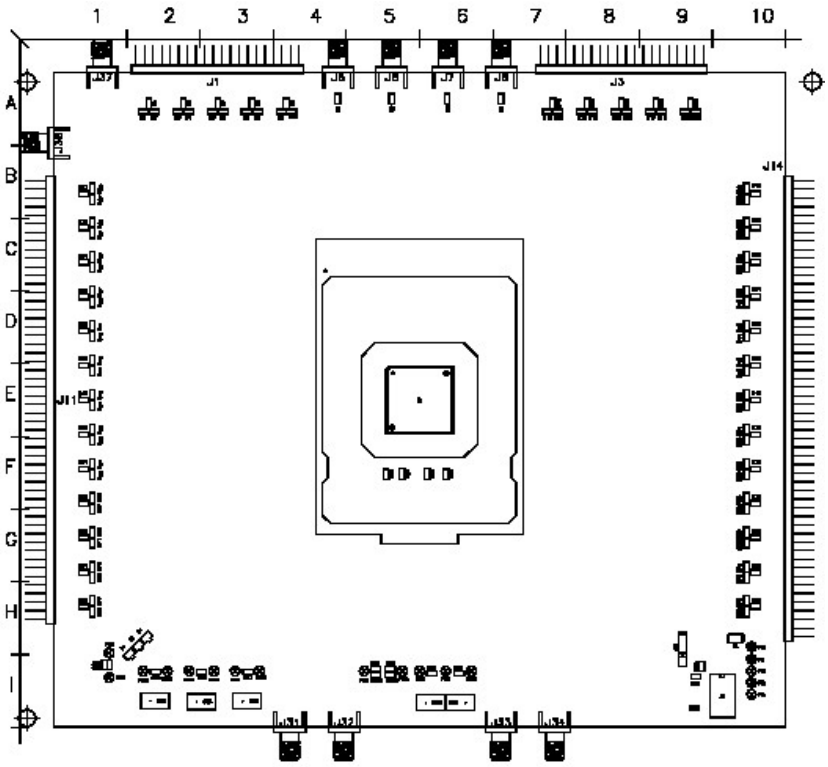


Figure 7-3. Equipped Board (Bottom)

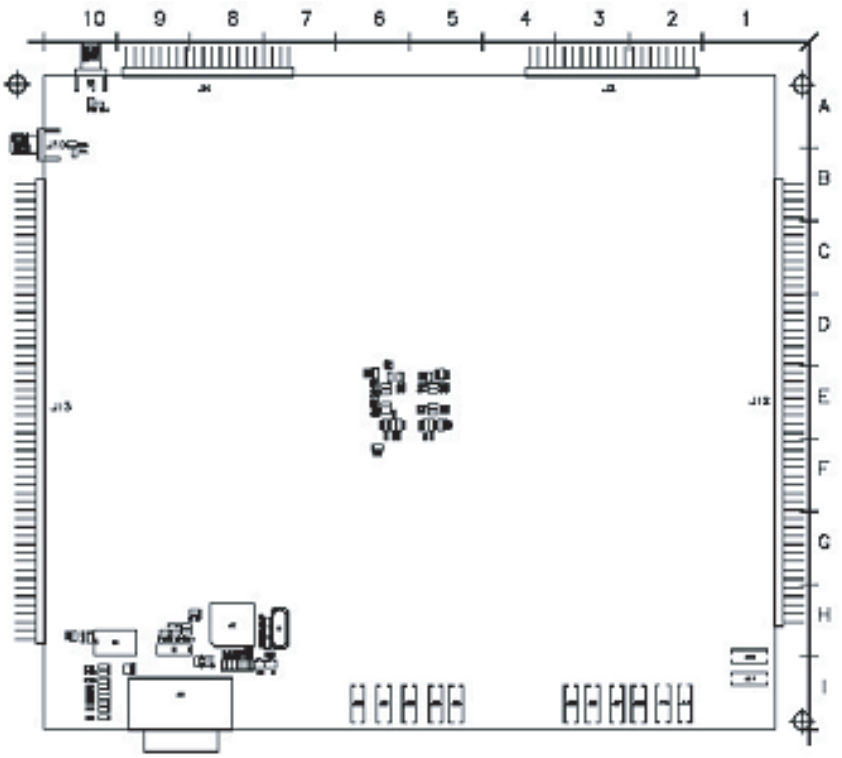


Figure 7-4. Top Layer

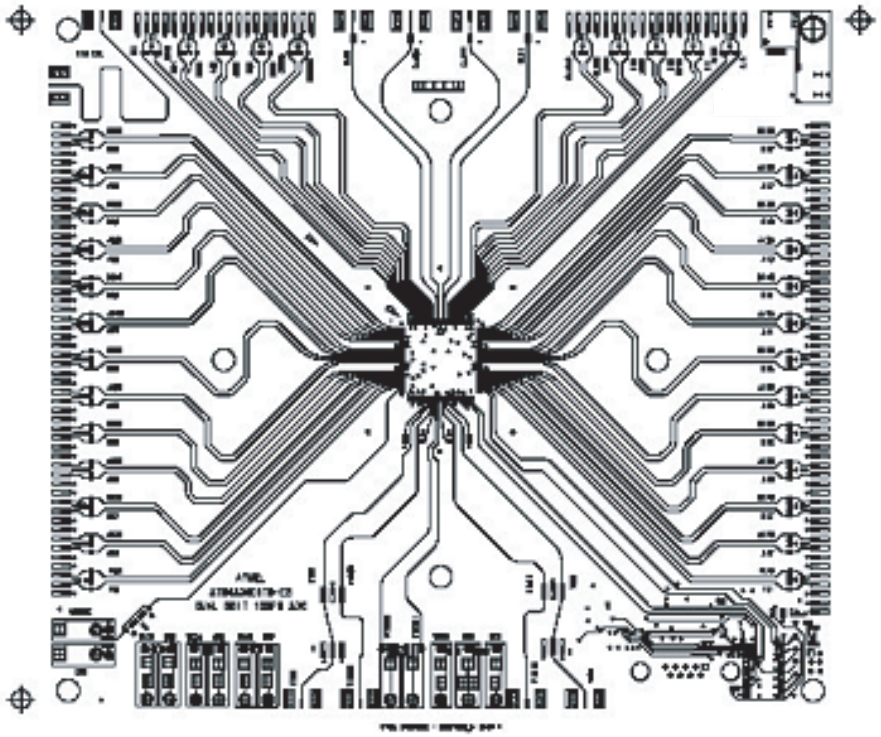
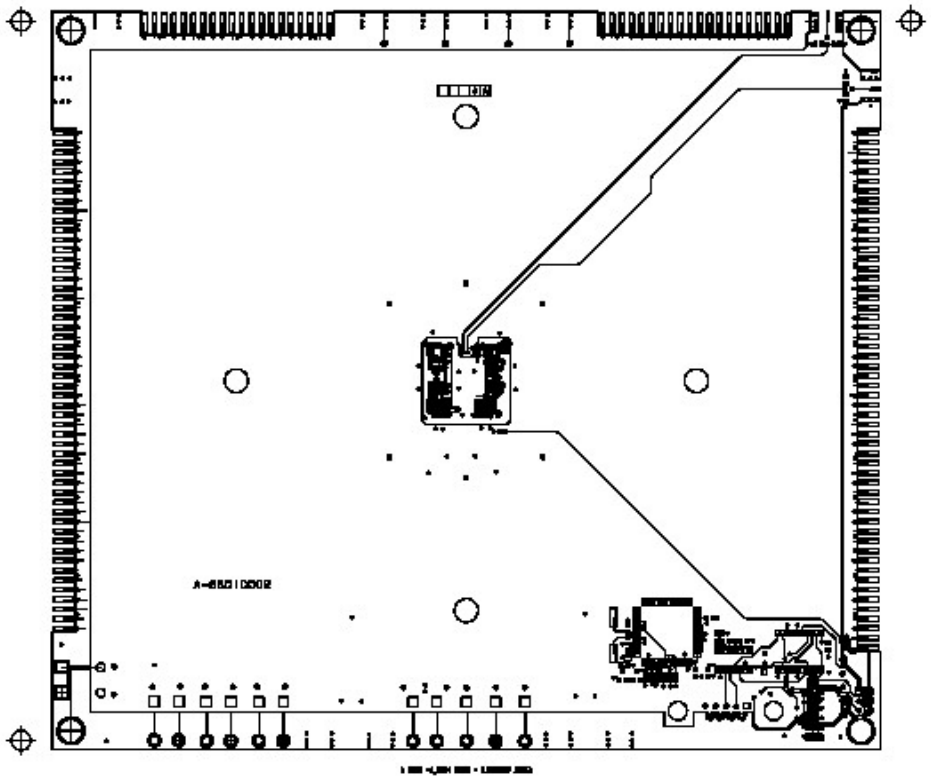


Figure 7-5. Bottom Layer



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