

## Application Note

### 1. Introduction

This application note aims at providing you with a comparison and recommendations to migrate from the existing AT84AS003/004 to the EV10AS003B/004B.

It first compares the two versions including:

- Power supplies
- Analog and digital controls

It also describes board modifications to migrate from the existing version to the B version.

This new B series ADC is designed to ensure minimum board level design modifications and equal electrical performance.

This document applies to the following devices:

- AT84AS003CTP
- AT84AS003VTP
- AT84AS004CTP
- AT84AS004VTP

### 2. Comparing AT84AS003/004 and EV10AS003B/004B 10-bit 1.5/2 Gsps ADC Devices

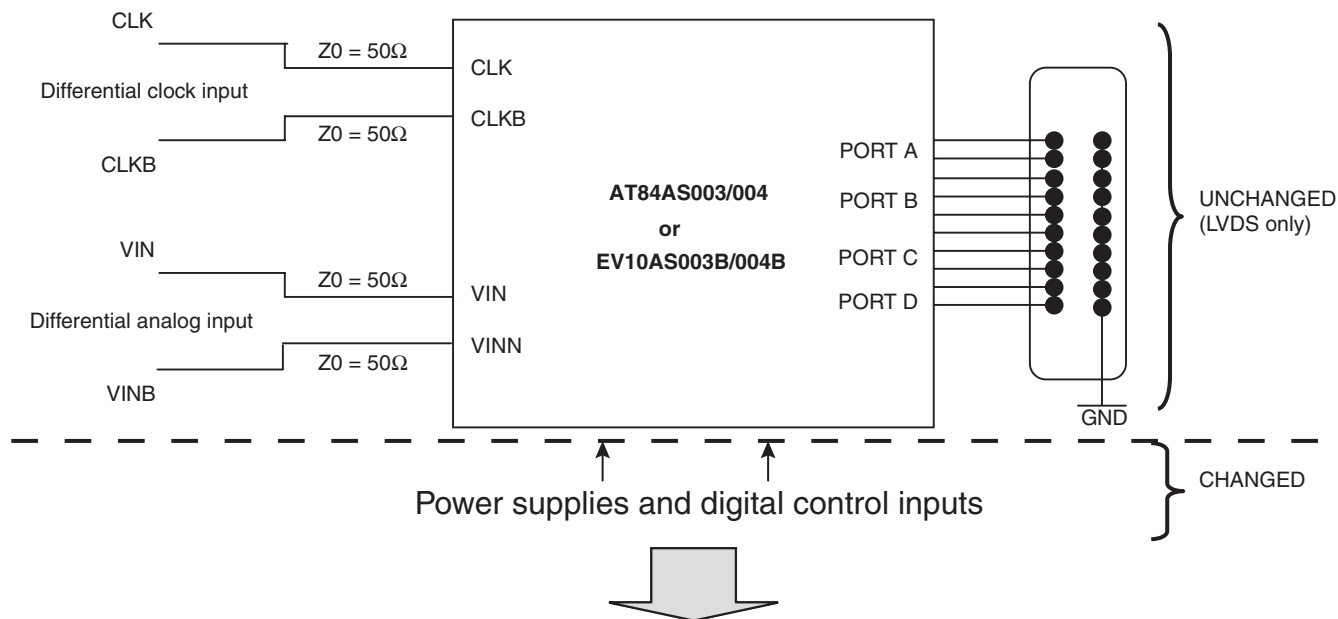
The EV10AS003B/004B is delivered in the same package as the AT84AS003/004, with same footprint, same mechanical and thermal characteristics.

The EV10AS003B/004B has been designed in order to feature the same timing characteristics as the AT84AS003/004 with ascending electrical performance compatibility.

The following section discusses the similarities and differences between the AT84AS003/004 and the EV10AS003B/004B.

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

Figure 2-1. Block Diagram



## 2.1 EV10AS003B/004B versus AT84AS003/004

Highlights of the differences between the two devices:

- Two power supply assignments (lower voltage):
  - Analog power supply:  $V_{EE}$
  - ADC Negative digital power supply:  $V_{MINUSD}$
- Three-digital control input pins active-level change (default mode is unchanged)

Table 2-1. Main Differences Between AT84AS003/004 and EV10AS003B/004B Devices

Function	Symbol	AT84AS003/004	EV10AS003B/004B
Analog power supplies	$V_{EE}$	-5V	-2.2V
Digital power supplies	$V_{MINUSD}$	-2.2V	0V (DGND)
Digital control inputs	DRRB	CMOS 3.3V/LVCMOS	CMOS 3.3V/LVCMOS
	B/GB, PGEB, SDAEN	0/ -5V	CMOS 3.3V/LVCMOS
Output buffers	LVDS	Yes	Yes

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## 2.2 Pinout Differences Summary

Table 2-2 is a description of the pin differences between AT84AS003/004 and AT84AD003/004B. Table 2-2 includes recommendations for forward compatibility. For more details, please refer to “EV10AS003B/004B Pinout (Bottom View, Balls Side)” on page 5.

**Table 2-2.** Pin Differences

Pin	AT84AS003/004	Modification on EV10AS003B/004B
A24, A26, A27, B24, B26, B27, C24, C26, C27, D24, D26, D27, E24, E26, F25, L25, L26, M27, R21, T21, U21	V <sub>CCA</sub>	Unchanged
B21, B23, C21, C23, D21, D23, E21, E23, F21, F23, F26, F27, G25, G26, G27, H25, H26, J25, J26, K27, N25, P25, R22, R23, R24, R25, R26, R27, T22, T23, T24, T25, T26, T27, U22, U23, U24, U25, U26, U27, V21, V23, V24, V26, V27, W22, W25, W26, W27	AGND	Unchanged
C17, C18, D17, D18, F3, F4, H3, H4, M3, M4, P3, P4, R18, T18, U16, U17	DGND	Unchanged
A25, B22, B25, C20, C22, C25, D20, D22, D25, E20; E22, E25, F20, F22, F24, K25, K26, L27, M25, M26, N26, N27, R20, T20	V <sub>EE</sub>	Pin label compatible Voltage change from -5V to -2.2V
D14, D15, R17	SUB	Unchanged (connect to VEE = -2.2V)
C4, C5, C6, C7, C9, C11, C13, C14, C15, C16, C19, D5, D6, D7, D9, D11, D13, D19, E3, E19, F19, J3, J4, L3, L4, N3, N4, R3, R4, R19, T6, T7, T9, T11, T13, T14, T15, T19, U4, U5, U6, U7, U9, U11, U13, U14, U15	V <sub>PLUSD</sub>	Unchanged
C3, C8, C10, C12, D3, D4, D8, D10, D12, D16, E4, E17, G3, G4, K3, K4, R16, T3, T4, T5, T8, T10, T12, T16, T17, U3, U8, U10, U12	V <sub>CCD</sub>	Unchanged
A19, A20, B19, B20, E18, F18, U19, U20	DGND	To be connected to digital ground plane (0V)
V25, W24	VIN	Unchanged
V22, W23	VINN	Unchanged
H27	CLK	Unchanged
J27	CLKN	Unchanged
B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	A0...A9	Unchanged
A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	A0N...A9N	Unchanged
B6, A6	AOR/DRAN, AORN/DRA	Unchanged
B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	B0...B9	Unchanged
B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	B0N...B9N	Unchanged
J2, H1	BOR/DRBN, BORN/DRB	Unchanged
M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	C0...C9	Unchanged
L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	C0N...C9N	Unchanged
V5, W5	COR/DRCN, CORN/DRC	Unchanged
V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	D0...D9	Unchanged
W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	D0N...D9N	Unchanged

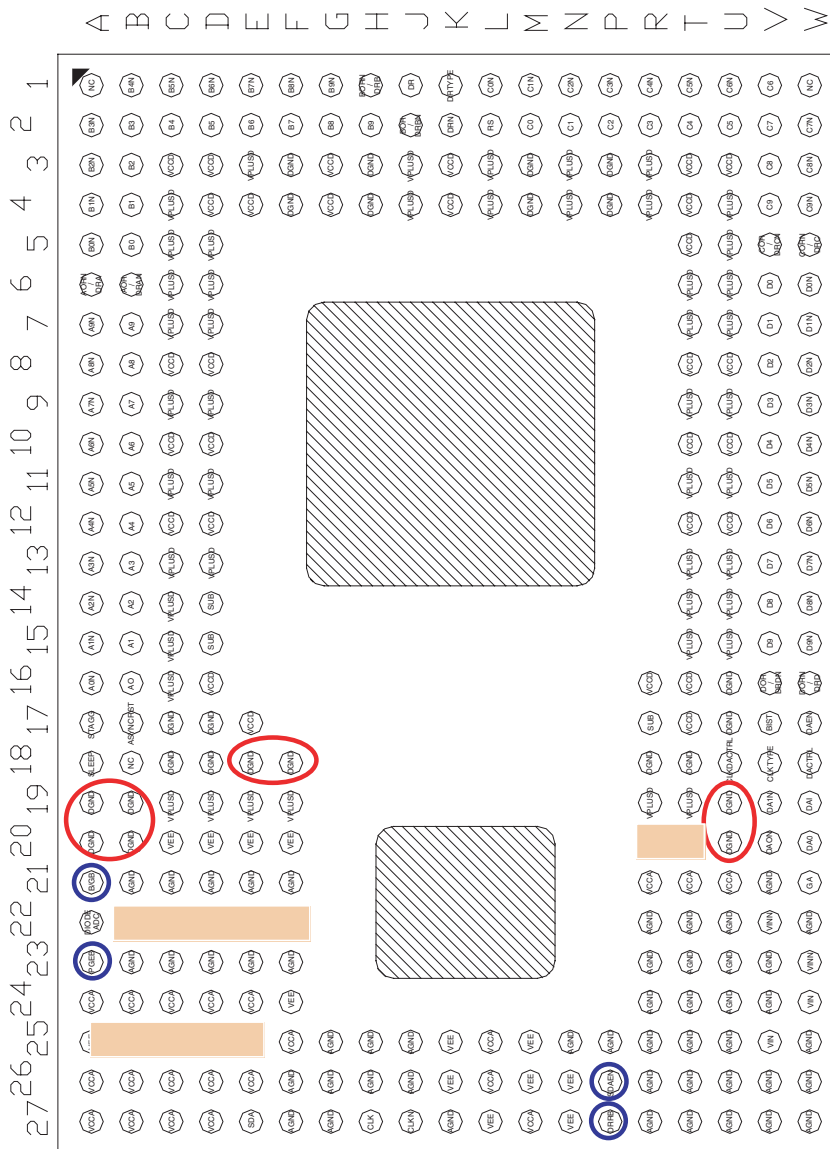
# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

**Table 2-2.** Pin Differences (Continued)

Pin	AT84AS003/004	Modification on EV10AS003B/004B
V16, W16	DOR/DRDN, DORN/DRD	Unchanged
J1, K2	DR, DRN	Unchanged
B17	ASYNCRST	Unchanged
V18	CLKTYPE	Unchanged
A18	SLEEP	Unchanged
A17	STAGG	Unchanged
K1	DRTYPE	Unchanged
L2	RS	Unchanged
V17	BIST	Unchanged
U18	CLKDACTRL	Unchanged
W18	DACTRL	Unchanged
W17	DAEN	Unchanged
W19, V19	DAI, DAIN	Unchanged
A21	B/GB	Binary mode: low level (GND) Gray mode: high level ( $V_{CC}$ instead of $V_{EE}$ )
A22	Diode/DECb	Unchanged
A23	PGEB	Inactive at low level (GND) and active at high level ( $V_{CC}$ instead of $V_{EE}$ )
P27	DRRB	Active low (GND) Unchanged
W21	GA	Unchanged
E27	SDA	Unchanged
P26	SDAEN	Inactive at low level (GND) and active at high level ( $V_{CC}$ instead of $V_{EE}$ )
A1, B18	NC	Full compatible

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

Figure 2-2. EV10AS003B/004B Pinout (Bottom View, Balls Side)



### Analog power supplies:



$V_{EE}$  plane:

$-5V = -2.2V$

### Digital power supplies (LVDS output buffers):



$V_{MINUSD}$  ( $-5V$ ) pin of the AT84AS003/004 becomes DGND ( $0V =$  digital ground plane) on the EV10AS003B/004B. DGND is an independent ground plane dedicated the output buffers.

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## Digital control input pins:



On the EV10AS003B/004B the B/GB, PGEB, SDAEN, digital input control pins are activated at logic high ( $V_{CC} = +3.3V$ , +1.3V threshold) instead of logic low ( $V_{CC} = -5V$ , -1.3V threshold). The inactive level remains at GND = 0V.

## 2.3 Getting Started with the EV10AS003B/004B Using the Existing AT84AS003/004 Evaluation Board

1. Connect all three power supplies ( $V_{EE}$ ,  $V_{CC}$ ,  $V_{PLUSD}$ ) and all ground accesses, as follows:
  - $V_{CC}$  : +3.3V
  - $V_{EE}$ : -2.2V
  - $V_{PLUSD}$ : +2.5V
2. Configure the digital control inputs in default mode (1).
  - B/GB floating or GND (binary mode)
  - PGEB floating or GND (disabled)
  - SDA floating or GND (disabled)
  - DRRB connected to  $V_{CC} = 3.3V$  (free running)
3. Connect the analog signal as formerly (same full-scale and common mode).
4. Connect the clock signal as formerly (same level and common mode).
5. Connect the high-speed acquisition system probes to the board data outputs (LVDS compatible).
6. Switch on the power supplies.
7. Apply the clock and analog signals.

Note: Apply adequate settings if activation is requested as described in [Section 2. on page 1](#).

Example: PGEB threshold becomes +1.3V instead of -1.3V.

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## 3. AT84AS003/004 to EV10AS003B/004B: Application Information

This section discusses the board implementation of the previous changes.

### 3.1 Analog and Digital Power Supplies

Table 3-1. Power Supplies

Power Supplies		AT84AS003/004	EV10AS003B/004B	Recommendations
Analog power supplies	$V_{EE}$	-5V	-2.2V	Change regulator
Digital power supplies	Output buffers $V_{MINUSD}$	-2.2V	0V	To be connected to digital ground plane

### 3.2 Digital Control Inputs Implementation (SDAEN, B/GB, PGEB)

Advantage: Since the input signals are CMOS compatible, the ADC can be connected directly to FPGA or microcontroller devices. The default level remains unchanged at GND.

Summary: The main differences between the AT8AS003/004 and the EV10AS003B/004B are the control levels.

- The active threshold becomes +1.3V instead of -1.3V
- The activated level becomes +3.3V instead of -5V

The following tables outline examples of configurations used for the existing AT84AS003/004 and replacement part EV10AS003B/004B. The implementation describes either pin re-assignments, removal of negative logic transformer or description of forward compatibility for  $V_{EE}$  and  $V_{CC}$  selection.

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## 3.2.1 SDAEN (Sampling Delay Adjust Enable)

	AT84AS003/004 SDAEN	EV10AS003B/004B SDAEN Implementation
Disable	GND (or floating) Default mode	GND (or floating) Default mode
Enable	$V_{EE}$ (-5V) Threshold (-1.3V)	$V_{CC}$ (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test AT84AS003/004 or EV10AS003B/004B Compatible board design		
Electrical schematic for embedded application with microcontroller or FPGA		<p>Note: FPGA connection -Standard LVTTTL I/O (programmable 3.3V bank) -LVDS I/O</p>



# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## 3.2.2 B/GB (Binary or Gray Output Coding)

	AT84AS003/004 B/GB	EV10AS003B/004B B/GB Implementation
Binary mode	GND (or floating) Default mode	GND (or floating) Default mode
Gray mode	$V_{EE}$ (-5V) Threshold (-1.3V)	$V_{CC}$ (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test: AT84AS003/004 or EV10AS003B/004B  Compatible board design		
Electrical schematic for embedded application with microcontroller or FPGA		<p>Note: FPGA connection -Standard LVTTTL I/O (programmable 3.3V bank) -LVDS I/O</p>

# Replacing AT84AS003/004 ADC with EV10AS003B/004B ADC

## 3.2.3 PGEB (Pattern Generator Enable)

	AT84AS003/004 PGEB	EV10AS003B/004B PGEB Implementation
Disable	GND (or floating) Default mode	GND (or floating) Default mode
Enable	$V_{EE}$ (-5V) Threshold (-1.3V)	$V_{CC}$ (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test: AT84AS003/004 or EV10AS003B/004B  Compatible board design		
Electrical Schematic for embedded application with microcontroller or FPGA		<p>Note: FPGA connection -Standard LVTTTL I/O (programmable 3.3V bank) -LVDS I/O</p>



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