Packaging of Atmel Data Conversion Circuits

Introduction

This document aims at highlighting the main issues in thermal management for fast and dense devices such as the Atmel Data Conversion products (ADCs and DMUX). It especially deals with packaging, electrical and thermal considerations in order to put forward the users' main interests in thermal management.

Some suggestions of thermal management used for Atmel Data Conversion Products are then given, such as heat sink assembly profiles, in view of helping users with heat removal.

This document is not exhaustive, nevertheless, it covers an appreciable area in terms of thermal management techniques for Atmel ADCs and DMUX Devices.

TS83xxxxx/
AT84xxx
ADCs
TS81102G0
DMUX

Application Note

Rev. 2192A–BDC–10/03

Packaging Main Considerations

In this section, we give an overview of the main considerations for available package types used for Atmel Data Conversion Products, electrical aspects and thermal characteristics.

The aim of this section is to outline thermal management issues in a global point of view.

Package Types

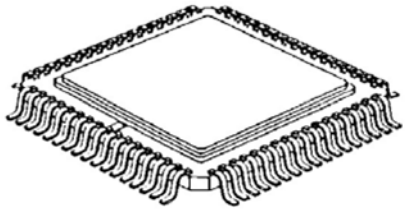
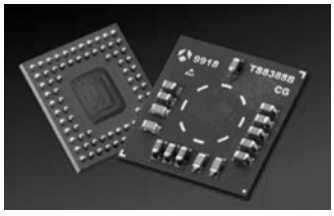
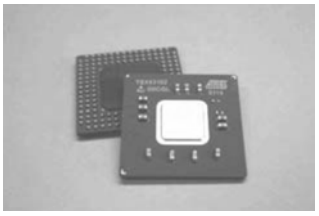
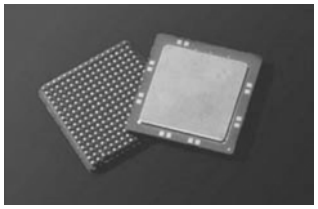
Quad Flat Pack/Ball Grid Array/Column Grid Array Packages

There are three main package types, which are commonly used by Atmel Data Conversion Products (ADCs, DMUX, MUXDAC):

- Quad Flat Pack (QFP) Packages
- Ball Grid Array (BGA) Packages
- Column Grid Array (CGA) Packages

Table 1 illustrates each type of package.

Table 1. Common Package Types

QFP Type	Example: CQFP68 
BGA Type	Example: CBGA72 and CBGA148  
CGA type	Example: CI-CGA255 

The Grid array Package Types are usually preferred to the QFP types when the overall dimensions of the device is a critical parameter. The Ball or Columns allows for distribution of the same number of pins in accordance with two dimensions (matrix of Balls or Columns) whereas the Quad Flat Pack only allow for pads along each side of the package.

In addition, the Grid Array packages allow, in general, a wider input bandwidth than with QFP packages because of the inductance of the QFP leads.

On the other hand, the thermal characteristics are improved with Ceramic QFP packages than with Ceramic Ball Grid Array Packages.

The other main difference between the Grid Array packages and the Quad Flat Packs concerns the way the package is to be soldered on a PCB board: this may be an important issue in some cases (need of special tooling for instance).

Finally, the Column Grid Array Packages are known to be more adapted to military and spatial temperature ranges than the Ball Grid Array Packages.

To sum up, the choice of a type of package is closely related to the application in which the device is to be used:

- Temperature range
- Power dissipation
- Size
- Intrinsic performances

Cavity Up/Down

Each type of package can be differentiated according to the die attachment method used.

The two possibilities are:

- Cavity Up: the die is attached to the bottom of the package (see Figure 1)
- Cavity Down: the die is attached to the inside top of the package (see Figure 2)

Figure 1. Cavity Up Die Assembly

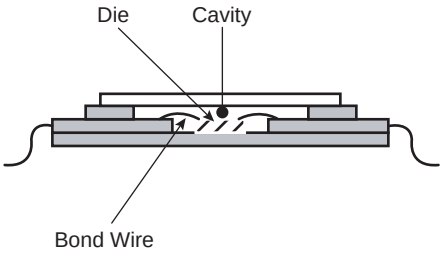
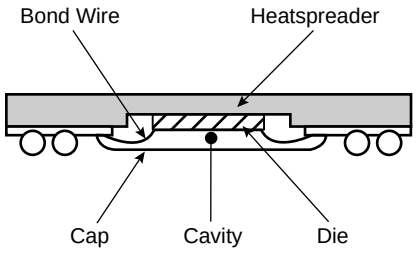


Figure 2. Cavity Down Die Assembly



The choice of a cavity up or down package can be made with respect to the thermal management that can be performed on the application board featuring the device (heat removal possible through the board or only via the air interface).

Table 2 summarizes the type of package used for the Broadband Data Conversion Products.

Table 2. Atmel Products Packages

Device	Package	Cavity Type	Material
8-bit 500 Msps ADC (TS8308500GL)	CBGA68	Down	Ceramic
8-bit 1 Gsps ADC (TS8388BF/BFS)	CQFP68	Up	Ceramic
8-bit 1Gsps ADC (TS8388BGL)	CBGA68	Down	Ceramic
10-bit 2 Gsps ADC (TS83102G0B)	CBGA152	Down	Ceramic
8-bit 4 Gsps ADC (TS83084G0)	CBGA164	Down	Ceramic
1:4/1:8 2 Gsps DMUX (TS81102G0)	TBGA240	Down	Organic + Copper
10-bit 1.2 Gsps MUXDAC (TS86101G2)	CI-CGA255	Up	Ceramic

Electrical Aspects

The previous section reviewed the different general types of package that are commonly used for Atmel Broadband Data Conversion Products. Now, our interest is to lay the emphasis on the physical factors which have to be taken into account to optimize the device performance.

RLC and Characteristic Impedance Parameters

The first factors concern the RLC electrical aspects of a package.

One may already know that the package can be viewed as a parasitic environment for the device. It indeed induces electrical interconnect parasitics through four parameters:

- Resistance
- Capacitance
- Inductance
- Characteristic impedance Zc (for transmission lines)

When implemented in a package, the complete device sees some additional resistance, capacitance and inductance generated by the package itself. These parasites may cause ground bounce and crosstalk phenomena, which, most likely, would lead to disturbances at the device input/output level.

These four parameters have thus to be taken into account in the design of any device and are the subject of detailed and rigorous simulations (at the design level) and tests (at the production level).

Table 3 illustrates the effects of each parameter (alone or in combination with another), on the final behavior of the device in its package.

Table 3. Effects of Each Parameter on the Device Behavior

Parameter	Effects on I/O	Effect on Power Supplies
Large R	RC and RL off-chip delays Power Dissipation Edge rate deterioration	Increase of I x R product drop on power
Large C	RC delays Distortion Crosstalk Edge rate deterioration	If between PWR and GND: better decoupling
Large L	RL delays Ground Bounce (= switching noise) Distortion Crosstalk Edge rate deterioration	Increase of $L \times \frac{di}{dt}$ drop voltage on power
Too Low Zc Too High Zc	Behaves as a distributed capacitor Behaves as a distributed inductor => Reflections occur at high frequencies	N/A

As underlined in Table 3, the parameter, which causes the largest and worst effects, is the inductance induced by the package.

The inductance of a package can be split into two main components:

- The self inductance of the package, which is related to the total electrical current loop in one lead of the package and also comprises the bond wire inductance.
- The mutual inductance, which takes into account the effects of two self inductances on one another in a two lead loop inductances.

The self and mutual inductance of a package depend on the dimensions of the package and the material used. The factor which the package designers concentrate on (in order to reduce the package inductance, once the dimensions and material of the package were chosen) is the bond wire. The shorter the bond wires are, the less voltage drop and noise are induced.

In addition, considering the relation: $V = L \times \frac{di}{dt}$

and having in mind that current spikes may be generated at the output switching, due to the charging and discharging of the load capacitance, we can see that the larger the inductance L, the higher the voltage drop due to current spikes.

In the design of our specific packages, every RLC component of the package has been modeled and simulated (from the inductance of the balls or leads to the coupling between the lines) very accurately. In particular, the package inductance is calculated taking into account the lead width, thickness and length and the position of the ground plane to the bond wire (the effects of the neighboring ground lines are also taken into consideration in the computation of the package inductance).

This usually leads to values of bond wire or lead inductance from 0.5 nH/mm to 0.9 nH/mm.

In addition, it can be underlined that the transmission lines (clock, input and data signal traces) inside the package are treated as transmission lines and not as too simply lumped L-C models. A 2D electromagnetic simulator is used to achieve proper dimensioning of the traces in order to reach Zc = 50 Ω transmission line.

Power Supply Decoupling in Packages

The performance of a package depends on its intrinsic characteristics, (RLC and characteristic impedance, as developed in the previous section) but the way it is going to interface with the rest of a design is also important.

The fact that more and more signals are constrained into small areas makes it harder to isolate the signals from one another. Decoupling schemes are then required to have a good and reliable separation between signals, leading to less-cross talk and less noise.

Ceramic packages can include built-in small capacitors between Power and Ground traces. This is achieved by taking advantage of the dielectric constant of the ceramic used (9.5 typical). Thanks to this material, only a small separation between the power and ground planes allows to go from 50 pF to 200 pF decoupling inside the package, depending on the surface of the plane used.

Our ADC packages are designed using such built-in small capacitor planes allowing high local performance decoupling of power supplies and ground. However, discrete decoupling capacitors (100 pF, 1 nF) should be used on board as close as possible to the package: around the package or even below the package on the other side of the board if possible, to achieve proper decoupling of the power supplies.

Finally, as shown previously, the design of a specific package becomes more and more a limiting factor in the performances of a device, and in particular when we deal with high speed devices such as Atmel ADCs and companion devices which usually feature a large bandwidth, good switching characteristics and reliable noise immunity capabilities.

Note: For confidentiality purpose, our models can not be disclosed in this document.

Thermal Characteristics

The second source of limitations for a packaged device is the way it is going to dissipate the power it consumes. Indeed, the role of the package in the power dissipation of the device is essential for device reliability considerations.

Main Issues

While designs go on minimizing the die and systems sizes, and as the integration of functions results in the need to handle more power, it becomes harder and harder to find a good compromise between keeping the overall dimensions of the device within limits and keeping it within its functional operating temperature range.

Key Parameters

The key parameters helping to evaluate the capability of a package to dissipate the device heat (electrical energy turned into heat) are the following:

Table 4. Thermal Parameters

Parameter	Description
Rth_{JC}	Thermal Resistance from Junction to Case
$Rth_{J\text{-bottom of balls}}$	Thermal Resistance from Junction to Bottom of Balls
Rth_{JA}	Thermal Resistance from Junction to Ambient
Rth_{CA}	Thermal Resistance from Case to Ambient
Rth_{CH}	Thermal Resistance from Case to Heat Sink
Rth_{HA}	Thermal Resistance from Heat Sink to Ambient

These parameters come from the package size, shape, and material it was built with. They give reliable information on the thermal management capabilities of the device in its package as well as a good idea of what would be required to dissipate the power the device consumes in practical applications.

Knowing the power dissipation of the device, these parameters allow to calculate the effective and maximum Junction temperature of the device during operation and to compare it to the maximum junction temperature allowed by the technology before breakdown (each technology features a max junction temperature above which the device reliability is not guaranteed).

Thermal management of the device will then consist in ensuring that the effective junction temperature of the device will never go beyond the maximum junction temperature specified by the technology.

The formula used to calculate T_J is:

$$T_J = Rth_{JC} \times P_D + T_{CASE}$$

This calculation applies with the hypothesis of uniformly distributed power dissipation all over the chip top surface (the power dissipation is performed via the top surface heat spreader of the package).

Example:

- Rth_{JC} = 2.0°C/Watt typical /3.0°C/Watt max
- P_D = 5.0 Watt typical/6.0 Watt max
- T_{CASE} = 75°C

=> T_J = 75°C + 3.0°C/W x 6.0 W = 93°C max

This junction temperature is the theoretical junction temperature of the die if uniformly distributed over the chip surface. In practice, the junction temperature may be greater at some specific spots of the chip (corresponding to the parts of the chip with the maximum power dissipation): the hot spot.

The hottest spot of the chip is calculated as follows:

$$T_{J\text{-hottest point}} = Rth_{JC} \times P_{D\ max} + T_{CASE} + \Delta T\_hot\ spot$$

The ΔT_hot spot value corresponds to the maximum difference between the average junction temperature all over the chip and the hottest spot.

Example:

- ΔT_hot spot = 13°C

$$\Rightarrow T_{J\text{-hottest point}} = Rth_{JC} \times P_{D\ max} + T_{CASE} + \Delta T\_hot\ spot = T_J + 13°C = 106°C$$

This gives the hottest spot of the chip, for a specified case temperature of 75°C in practical conditions of use.

Table 5 gives some thermal conductivity data for typical material used in our packages for information only (the values can be used to make thermal computation or simulation of a whole package from die to external interface).

Table 5. Thermal Data for Thermal Simulation

Material	Thermal Conductivity (Watt/cm/°C)
Al2O3 Alumina	0.17
Ag Filled Glue	0.02
CuW Copper/Tungsten	1.8
Si (at 100°C)	0.95
Thermal grease	0.01
Aluminium	1.5
Copper (in TBGA240)	3.0
Sn63 Pb37 (in BGA balls)	0.5
Pb95 Sn95 (in CGA columns)	0.4

In general, the junction temperature given by the kind of calculation above and considering all parameters is well beyond the allowed junction temperature for device reliability. In order for the junction temperature to stay below its technological limit, thermal management is needed, as described in the following section.

Thermal Management

General Considerations

In the previous section, we gave simple methods to calculate the theoretical junction temperature of a chip, assuming its power consumption and thermal characteristics in specified conditions.

The practical junction temperature of the chip may however be slightly higher or lower than its theoretical value and this is why Atmel ADCs and other Data conversion products were designed and offered with the possibility to monitor the die junction temperature. This is described below.

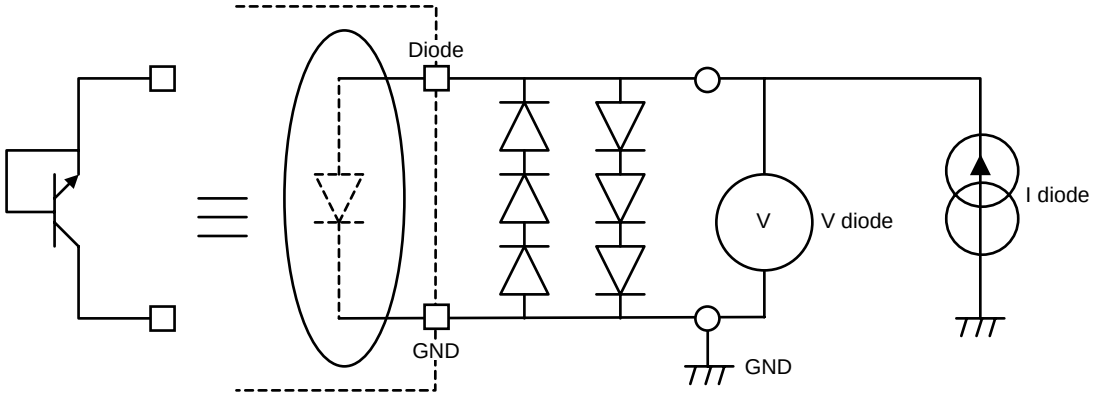
Die Junction Temperature Monitoring Function

Each Atmel Data Conversion Product (ADC, DMUX, DAC) features a Die junction Monitoring function, which allows the user to measure the die junction temperature.

A simple method is used:

The measurement device is constituted of a serial Diode mounted Transistor (CB junction). The association of these transistors is equivalent to a diode as shown in Figure 3.
By forcing a current flowing into the diode mounted transistor, a table of correspondence between the V diode potential of the transistor and the junction temperature can be built.

Figure 3. Die Temperature Monitoring Principle Schematic



Notes:
1. During a temperature measurement, some transient voltage peaks may occur while modifying the current source value. These peaks may irreversibly damage the transistor. That is why we recommend to implement the 2 x 3 head to tail protection diodes of Figure 3.
2. In certain designs, the diode is doubled and consequently, there are 5 instead of only 3 protection diodes. The rule of thumb is to have 2 additional protection diodes than the number of diode mounted transistor in the device (3 protection diodes for 1 internal diode mounted transistor or 5 protection diodes for 2 diode mounted transitors).

Heat Sink Calculation

As underlined in a previous section, the device reliability can be guaranteed for a specific temperature range only. The device specifications always mentions the maximum junction temperature that the device can sustain during operation. As shown in the previous calculations, this maximum junction temperature is generally overridden despite the fact the package has exceptional thermal characteristics. To overcome this, the use of heat sinks becomes mandatory.

In what follows, we describe two methods to be used to choose the right heat sink for a specific device and package.

Let's assume that we have a device with the following characteristics:

- Rth_{JC} = 1.5°C/W
- $\Delta T\_hot\ spot$ = 10°C
- Power dissipation = 4.0 W typical/5.0 W max
- Max T_J allowable = +100°C
- The customer specifies an ambient temperature of T_A = 65°C

The case temperature is given by the following formula:

$$T_{CASE} = T_A + P_D \times \text{Heat sink external thermal resistance}$$

Thus, $$\text{Heat sink external thermal resistance} = (T_{CASE} - T_A)/P_D$$

The case temperature is also linked to the junction temperature in:

$$T_{J\text{-hottest point}} = Rth_{JC} \times P_{D\ max} + T_{CASE} + \Delta T\_hot\ spot$$

$$T_{CASE} = T_{J\text{-hottest point}} - \Delta T\_hot\ spot - Rth_{JC} \times P_{D\ max}$$

Since the max allowable junction temperature specified is 100°C, the max allowable T_{CASE} is:

$$T_{CASE}\ max = 100°C - 10°C - 1.5°C/W \times 5.0\ W$$

$$T_{CASE}\ max = 82.5°C$$

The heat sink max external thermal resistance is therefore:

$$\text{Heat sink External thermal resistance} = (T_{CASE} - T_A)/P_{D\ max}$$

$$\text{Heat sink External thermal resistance} = (82.5°C - 65°C)/5.0\ W$$

=> Heat sink External thermal resistance = 3.5°C/W

A better cooling efficiency than 3.5°C/W is thus required to decrease the chip temperature for reliability considerations or in case of a hotter ambient temperature.

Suggested Solutions

Due to the previous calculations, we know what performances are required for the choice of a proper heat sink for the device. The eventual choice must take into account the different heat sink solutions on the market. As a matter of fact, a wide choice of heat sinks are available from passive heat sink to active heat sink with internal fans.

The final choice for a heat sink depends on the physical characteristics of both the device in its application system and the heat sink itself (size, material, type, assembly method).

Figure 4, Figure 5 and Figure 6 are examples of passive and active heat sinks.

Figure 4. Passive Heat Sink (AAVID)

Figure 5. Active Heat Sink Without Aluminium Block (AAVID)

Figure 6. Active Heat Sink On Aluminium Block (AAVID)

Passive heat sinks are usually used for devices with a power dissipation ranging between 4 and 10 watts while active heat sinks may be used when the device dissipates more than 8 W. For devices with a power consumption below 5 W (typ.), the package should be sufficient for the heat management of the device at ambient temperature (T_A = 25°C).

Table 6 summarizes the parameters to take into account.

Table 6. Parameters for Heat Sink Choice

Parameters	Passive Heat Sink	Active Heat Sink
Thermal Resistance range	X	X
Heat sink size	X	X
Fan size/speed	Not applicable	X
Assembly Method	X	X
Ambient Temperature	X	X

Air Flow Conditions

Before going into the details of the heat sink performance requirements, the first parameter to be defined is the air flow conditions in which the device will operate.

The previous calculations were given in the case of "still" air (natural convection) but in other air flow conditions, the thermal characteristics of the packaged device vary (as shown in Figure 7 giving the example of the thermal resistance of the TS8388BF 8-bit 1 Gsps ADC vs air flow).

Figure 7. Thermal Resistance Characteristics for the TS8388BF ADC With and Without Heat Sink VS Air Flow

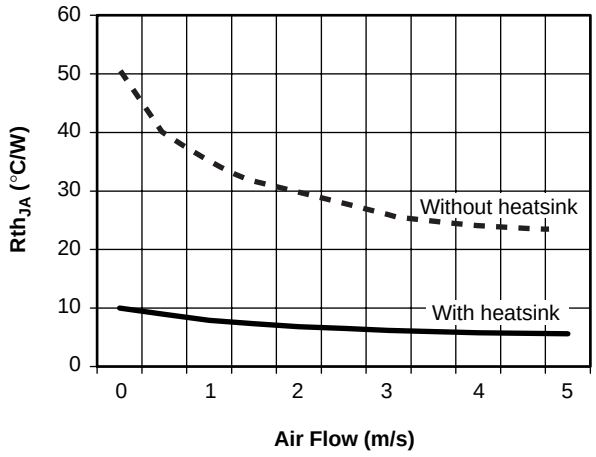


Figure 7 shows that without a heat sink, it is possible to gain about 30% on the thermal resistance of the device by increasing the air flow from 0 m/s to about 2 m/s. In case the device and its board can be ventilated, the requirements for the heat sink will be less demanding. This also shows how the heat sink performance can be enhanced when coupled with forced air fans (see “Fan Size and Speed for Active Heat Sinks” on page 15).

Once the air flow conditions have been clearly defined, the calculation of the thermal resistance requirements for the heat sink can then be led.

Thermal Resistance Range

For what follows, we assume that the device will operate in a still air flow environment.

If we go back to our example, we see that we need a heat sink with a cooling efficiency better than 3.5°C/W. To this figure, we have to add the thermal resistance of the glue or thermal grease used between the heat sink and the top of the package. Manufacturers usually propose thermal pastes or glues with thermal resistance ranging from 0.1°C/W to 1°C/W for each cm^2 depending on the thickness of the interface material.

In our example, assuming the use of a thermal paste featuring 0.01W/cm/°C for a thickness of 100 µm, an additional 1.05°C/W thermal resistance has to be taken into account in the calculation of the thermal resistance of the packaged device from junction to case including the thermal paste.

This concretely means that the heat sink should now feature a thermal resistance below 3.5°C/W - 1.05°C/W = 2.45°C/W.

The heat sink should therefore be chosen with a thermal resistance ranging from 0°C/W to 2.5°C/W.

Heat Sink Dimensions

The choice of the heat sink dimensions also depend on:

1. The available space possibilities in the application:

   It seems obvious that in todays applications, one of the main limitations in a design is the available space the system can occupy. This constraint must also be taken into consideration in the choice of a component itself: it is no use having a small component with exceptional capabilities if the heat sink it requires is too big for the application…

2. The way the heat sink will be fixed on the board and will be in contact with the package of the device:

   Whether the heat sink is to be screwed to the board or fixed with some thermal glue, the heat sink dimensions can vary. In particular, this parameter will help choosing the maximum width and height for the heat sink, which are usually the required information needed by manufacturers to select a first run of heat sinks.

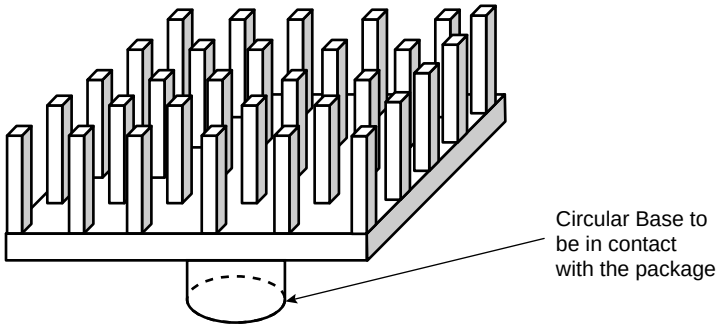
3. Stress on the device and/or the board are important parameters too and give another constraint on the heat sink dimensions:

   Finally, the surface of contact between the package and the heat sink is another factor to take into consideration.

   A trivial example is the TS8388BG 8-bit 1 Gsps ADC device: this device has a cavity down CBGA package and features on-package discrete capacitors and resistors.
   Its thermal management has to be done via the top of the package. Because of the discrete components, the surface in contact between the top of package and bottom of heat sink has to be a disk of 6.8 mm diameter. It will thus not be possible to use a standard flat heat sink, even if it features the required thermal resistance.

   Figure 8 gives an illustration of the kind of heat sink needed in the case of the TS8388BG ADC.

Figure 8. Example of Heat Sink Shape for the TS8388BGL ADC



4. The thermal characteristics of the heat sink:

   The more surface to the ambient air the heat sink has, the more heat it is going to dissipate: consequently, the more power to dissipate, the bulkier the heat sink for optimum performance. For a given heat sink size, better heat management could be achieved with a heat sink made of special material with better thermal characteristics (anodized aluminium…).

Fan Size and Speed for Active Heat Sinks

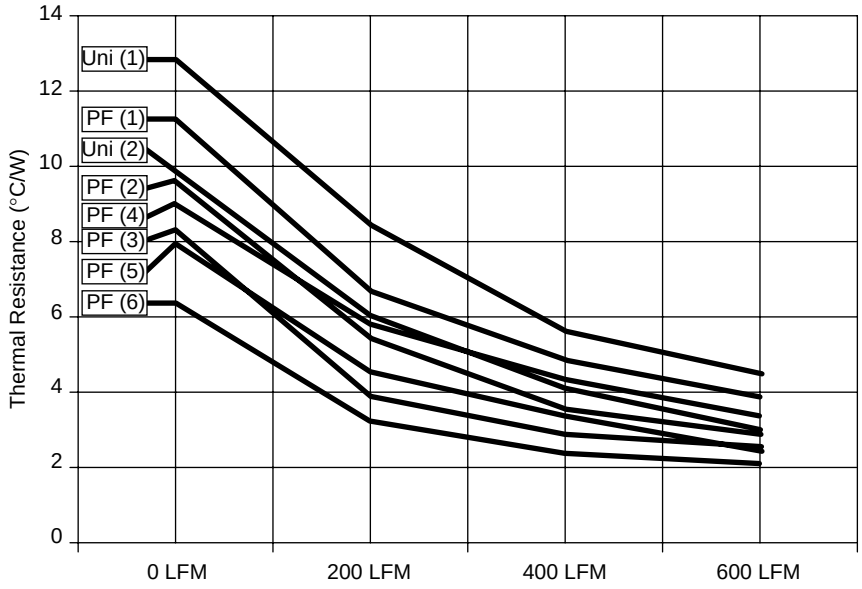
As already underlined previously, the use of active heat sinks increase significantly the heat removal capabilities of a heat sink due to the forced air. Nevertheless, an active heat sink will not be preferred to passive heat sinks at first, when space, mechanical and electrical considerations are at stake. In the case of our ADCs, the choice of active vs. passive heat sink will generally depend upon the power dissipation from a device.

As a rule, we have not used such heat sinks for our products since they stay in the power consumption mid-range. However, the possibility to use active heat sinks still exists and gives an alternative to the heat management by passive heat sinks.

Similarly to passive heat sinks, the requirements for active heat sinks are based on the package's thermal characteristics and device power consumption. In addition to this, the intrinsic characteristics of the active heat sink in relation to its forced air capabilities.

Figure 9 gives an example of active heat sink capabilities.

Figure 9. Thermal Resistance VS Air Flow (Device from ChipCoolers)



Note: 200 LFM are equivalent to 1.0 m/s.

Assembly Methods

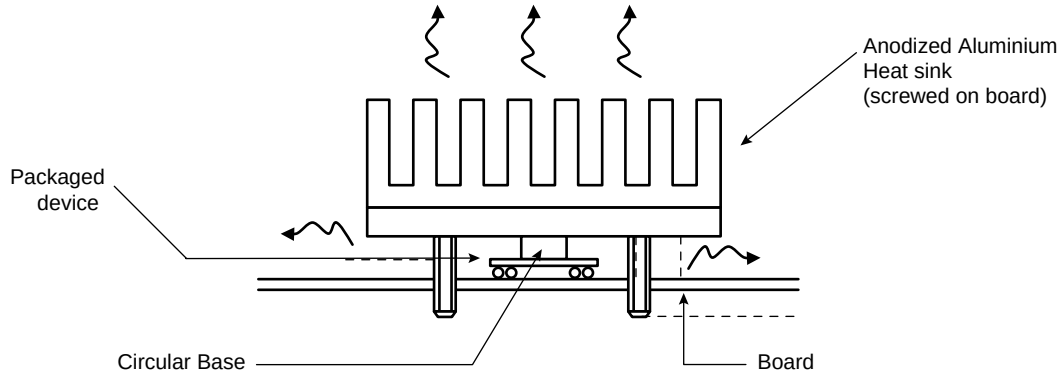
The last factor to be mentioned in this section is the heat sink assembly method, which can be benefited from in order to optimize the heat management of the device on its application board. As a matter of fact, the characteristics of the device package may be completed by the characteristics of the board on which the device is going to sit. An important fraction of the heat removal is indeed achieved via the board, depending on:

- the board size
- the number of copper layers of the board and the fraction of copper on each layer
- the board heat conduction capabilities

Different board layouts can be proposed here, depending on the type of package:

- Heat removal via a heat sink on top of package

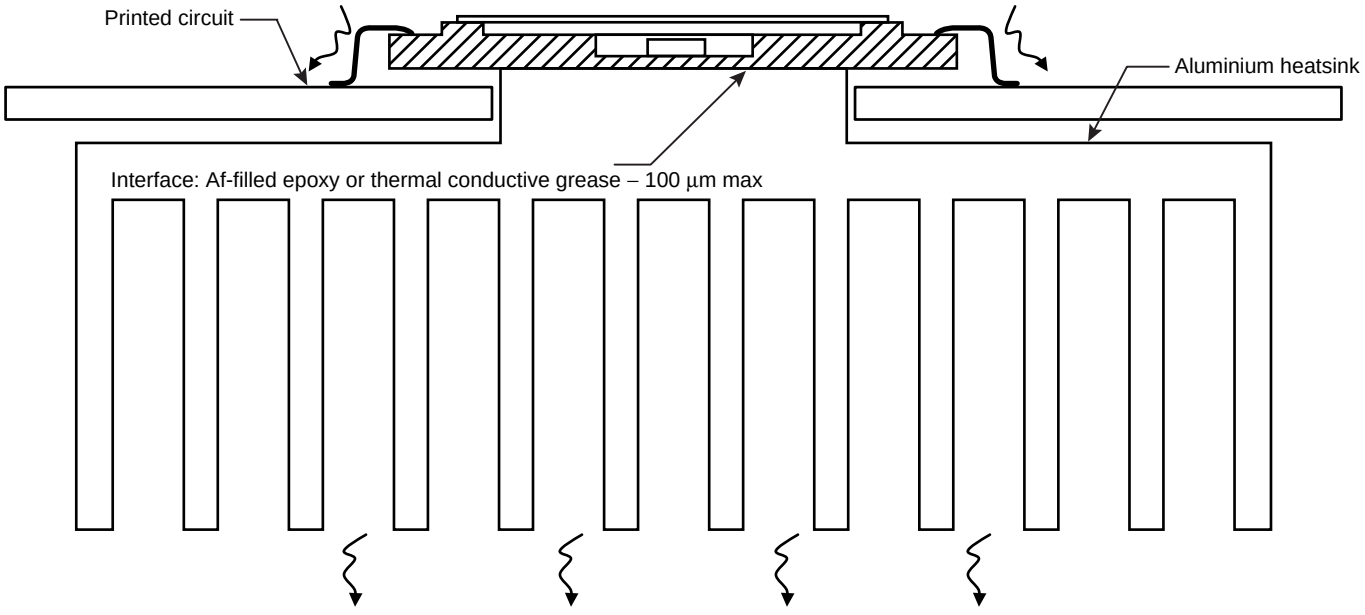
Figure 10. TS8308500GL/TS8388BGL/TS83102G0BGL Heat Sink Assembly Method



Note: Too much pressure on top of package will stress the SnPb balls too much: a reliability problem can occur. Do not load the balls more thn 1 Newton per ball (or 15 Kg force on top of package for CBGA152 or 24 Kg for TBGA240).

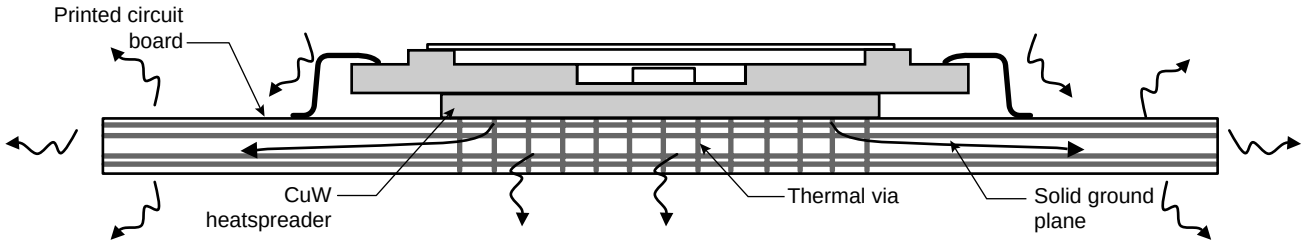
- Heat removal via a heat sink under the board

Figure 11. TS8388BF Heat Sink Assembly Method



- Heat removal with on-package heat spreader and thermal vias

Figure 12. TS8388BFS Heat Sink Assembly Method



References

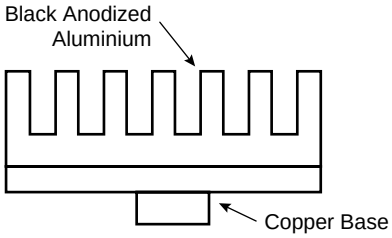
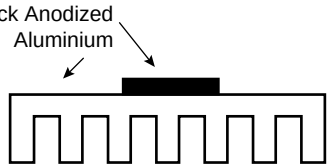
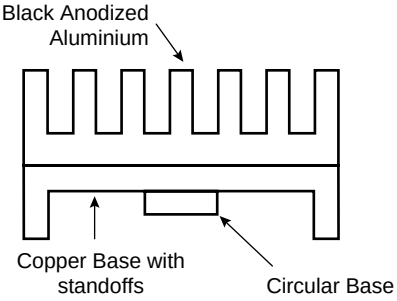
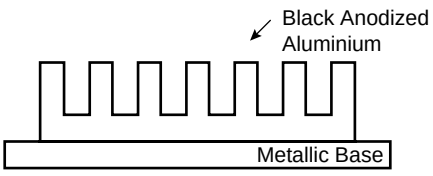
Here are listed some heat sink manufacturer references:

- http://www.AAVID.com
- http://www.malico.com.tw
- http://www.chipcoolers.com
- http://www.coolermaster.com
- http://www.fischerelektonik.de

Useful sites for papers, Application Notes and list of suppliers about thermal topics:

- http://www.electronics-cooling.com
- http://www.coolingzone.com

Appendix: Atmel Broadband Data Conversion Package Offer

Device Description	Package Description	Heat Sink Requirements
TS8308500GL ADC 8-bit 500 Msps TS8388BGL ADC 8-bit 1 Gsps	CBGA68 Case material: Al2O3 Substrate: Al2O3 Ceramic Lid Balls: Sn/Pb 63/67	Heat sink with circular base (Ø 6.8 mm) 50 x 50 x 25 mm; Black anodized Aluminium; Screwed on board 
TS8388BF ADC 8-bit 1 Gsps	CQFP68 Substrate: Al203	Heat sink with circular base (Ø 15 mm) 50 x 50 x 16 mm; Black anodized Aluminium; Screwed on board 
TS8388BFS ADC 8-bit 1 Gsps	CQFP68 With CuW heat spreader Substrate: Al203 AlN interface between die and CuW	Same Heat sink as for the TS8388BF OR Direct attachment to Board
TS83102G0B ADC 10-bit 2 Gsps	CBGA152 CuW heat spreader Case material: Al2O3 Substrate: Al2O3 Kovar with Nickel hermetic Lid Balls: Sn/Pb 63/67	Heat sink with circular base (Ø 8.5 mm) 50 x 50 x 22 mm; Black anodized Aluminium heat sink glued on a copper base; Screwed on board 
TS81102G0GTP DMUX 8/10-bit, 1:4/1:8, 2 Gsps	TBGA 240 Copper Heat spreader Balls: Sn/Pb/Ag 62/36/2 Eutectic Balls	Black anodized Aluminium glued on a metallic base; 50 x 50 x 20 mm; Screwed on board 

Note: Please refer to the associated product and evaluation board data sheets for more information on each product.

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