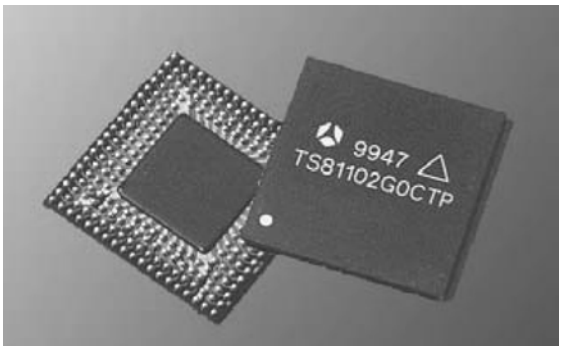
Atmel DMUX
Operating Features

Introduction

This document is an aid to take advantage of all the different features and functions available in the Atmel DMUX device. It highlights and describes the operating mode of the DMUX with the aim of facilitating the use of this product. It also gives relevant information on how to interface this DMUX with typical loading circuits.



TS81102G0 DMUX TBGA 240
Package Device

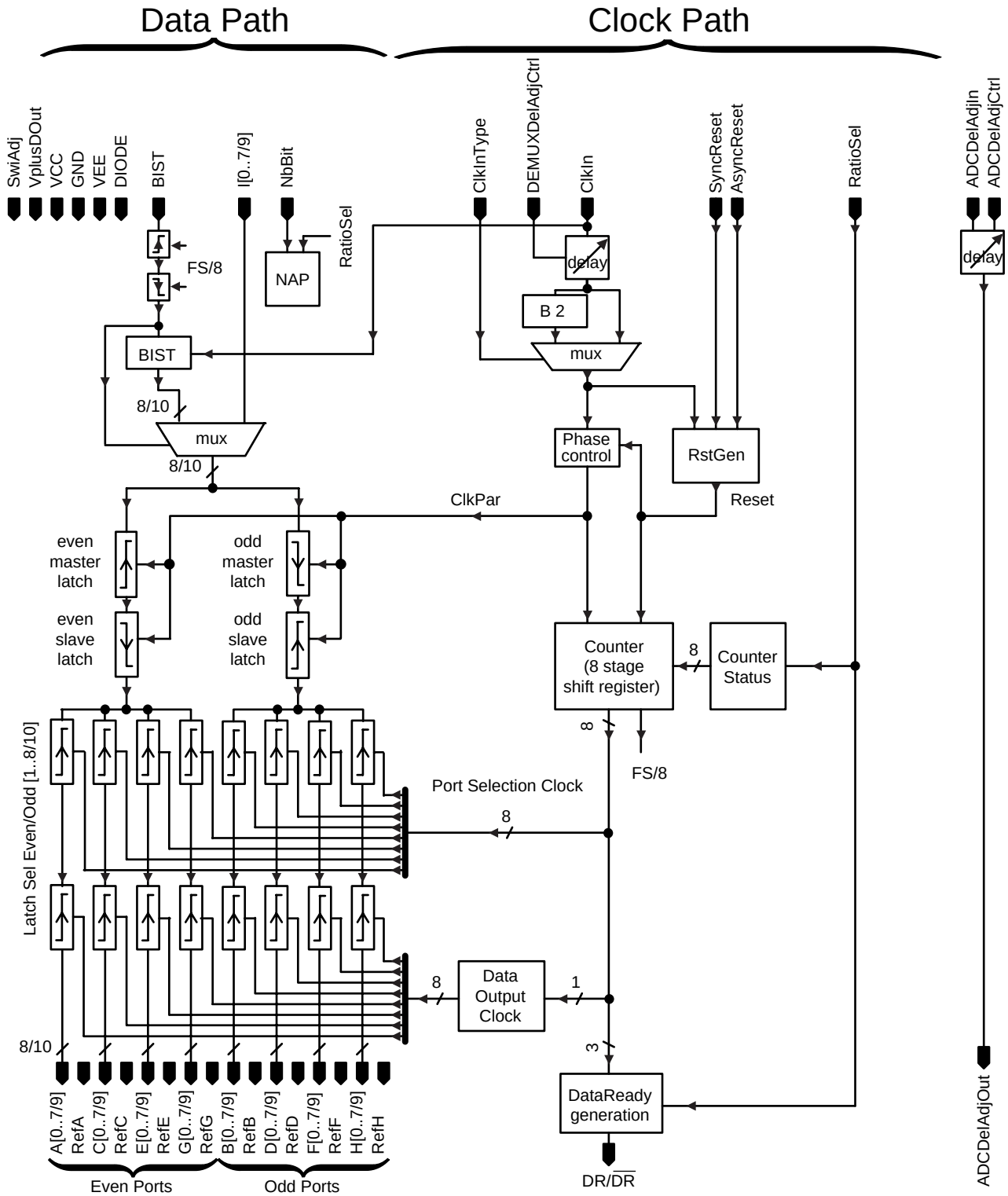
TS81102G0
DMUX

Application Note

Rev. 2168A–BDC–10/03

TS81102G0 DMUX Block Diagram

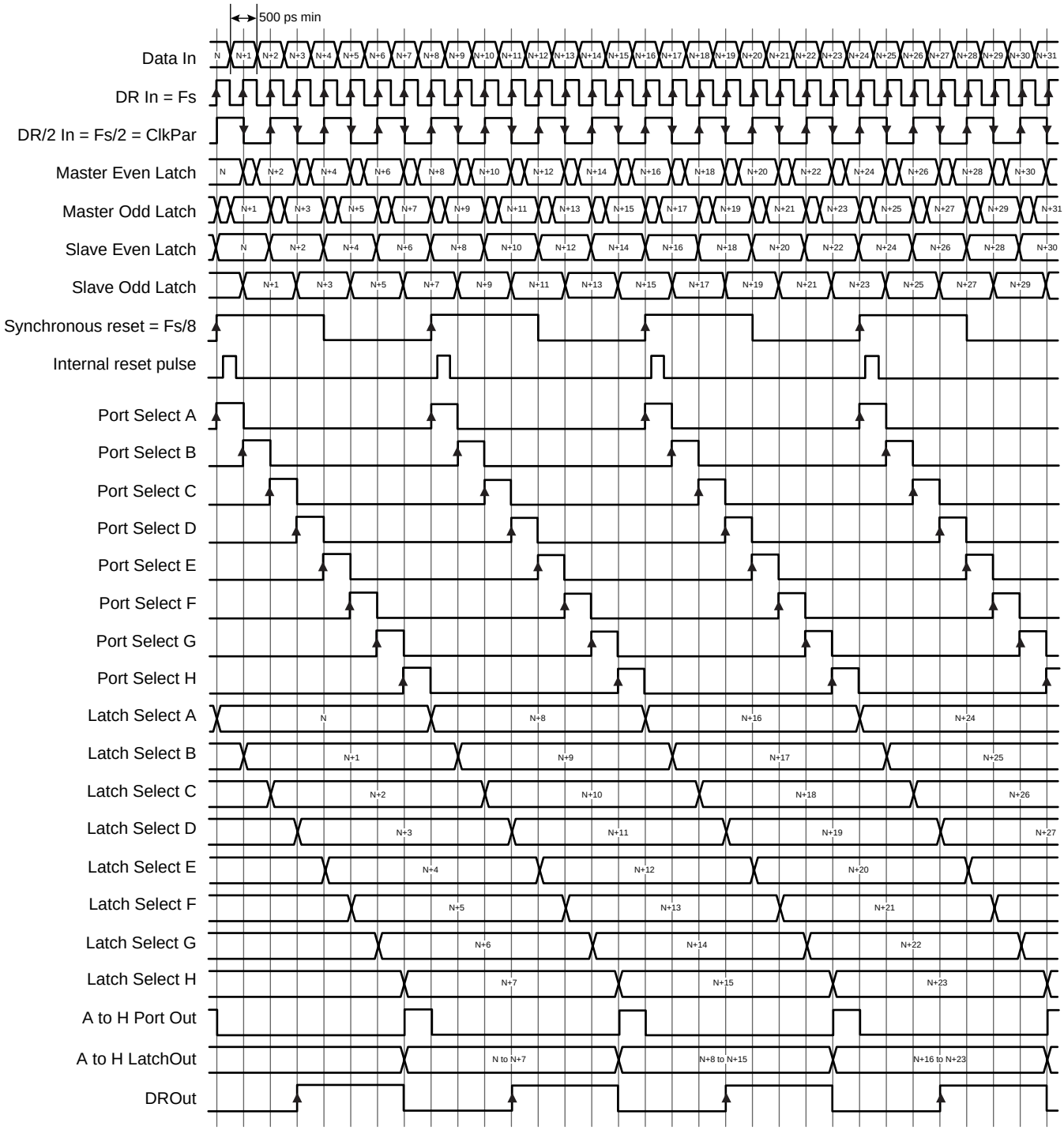
Figure 1. TS81102G0 DMUX Block Diagram



DMUX Internal Timing Diagram

This diagram corresponds to an established operation of the DMUX with Synchronous Reset.

Figure 2. DMUX Timing Diagram



How To Use the DMUX Reset ?

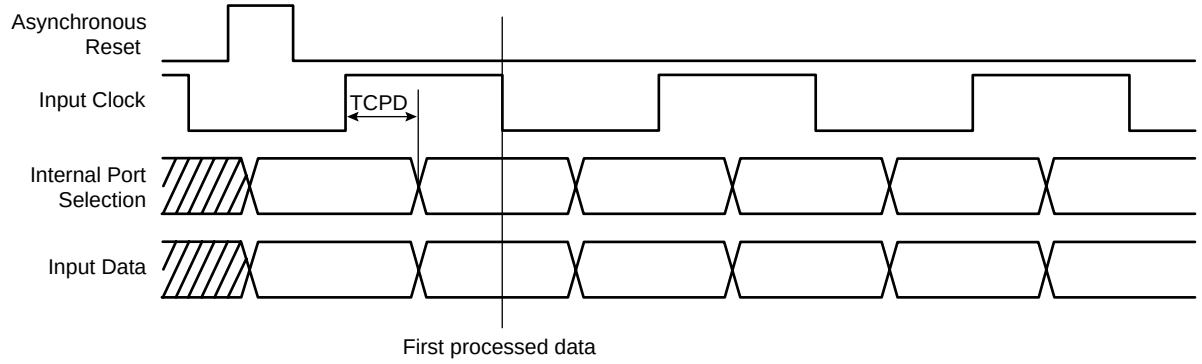
There are two available Resets on the Atmel DMUX, which have different advantages and aims:

- On the one hand, the Asynchronous Reset is necessary to start the DMUX and can be considered as the Master Reset of the device.
- On the other hand, the Synchronous Reset is recommended during operation of the DMUX. This Synchronous reset has the main role of guaranteeing that whenever a de-synchronization occurs within the internal stages of the DMUX (loss of synchronization at the internal port selection), causing the DMUX to lose data, each new cycle in the output port selection restarts on port A. This is done internally at each new port selection cycle through a reset of the internal counters managing the port selection. Thanks to the Synchronous Reset, any possible loss of data due to de-synchronization is greatly reduced.

In the following sections, each reset of the DMUX is described in detail. The focus is, in particularly, on the methods to be used for proper operation of the DMUX.

Asynchronous Reset

Figure 3. Asynchronous Reset



At power up of the DMUX the sequence to be followed is:

- Supply the DMUX
- Apply the input clock signal
- Perform an Asynchronous reset (see below)

The Asynchronous Reset works according to TTL mode and is active in the high level.

When the DC power and the input clock have been supplied to the DMUX, the Asynchronous Reset pin is tied to the TTL high level (active). To de-activate the Asynchronous reset and consequently start the DMUX, it is recommended to connect the Asynchronous pin to ground. This pin should remain at ground level during operation of the DMUX.

When the Asynchronous Reset is active, the outputs are paralyzed to their respective levels (output clock and output data remain to the level they had before the asynchronous reset).

When the Asynchronous Reset comes back to its low level, the DMUX starts, the outputs are then active and available at the DMUX output ports, beginning at port A.

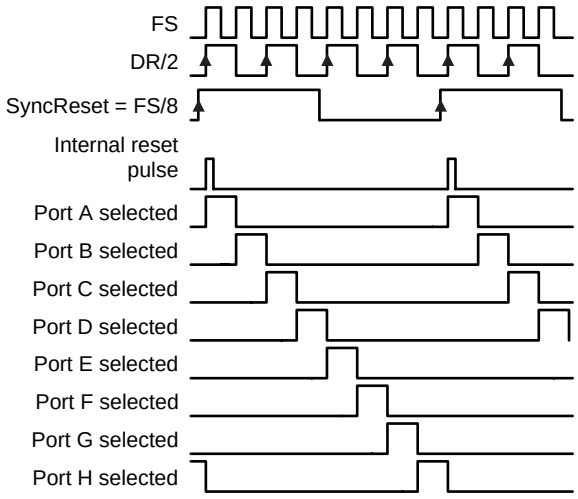
When the Asynchronous Reset is to be used while the DMUX is already supplied by V_{CC}, V_{EE} and V_{PLUSD} (for any reason), the Asynchronous Reset has then to be tied to a TTL high level during a minimum duration of a 500 ps pulse.

Synchronous Reset

As previously mentioned, the Synchronous Reset cannot start the device, it is useful only once the device is running.

Figure 4 illustrates the utility of the Synchronous Reset.

Figure 4. Synchronous Reset



The Synchronous Reset Signal must be a signal of frequency (Fs/4 x N) in 1:4 mode and (Fs/8 x N) in 1:8 mode to ensure the right sequencing of the data.

In fact, each rising edge of this signal induces a re-initialization of the internal counters of the DMUX, that control the port selection. Consequently, each rising edge of the Synchronous Reset causes the port selection to restart from port A to port H, with the right sequence of data and synchronization.

In case of de-synchronization of the port selection, the output data will become correct again within a maximum of N x 7 clock periods thanks to the Synchronous Reset.

Note: N must be an integer.

Output Level Compatibility Setting

The DMUX outputs are compatible with various digital standards such as ECL, PECL, LVDS and TTL.

This was made possible by the VplusD independent and adjustable power supply and to the fine tuning function "Swing Adjust".

There are three types of output signals (Data Ready, digital data and Reference voltage) but they have exactly the same behavior when adjusting both the VplusD and Swing Adjust parameters.

The Data Ready output signal is a differential signal and there is only one for all the ports.

There are 80 digital data outputs and 8 Reference voltages (10 digital data outputs and 1 reference per port). They are all single-ended signals.

Figure 5. Data Ready Differential Output Buffer Schematic

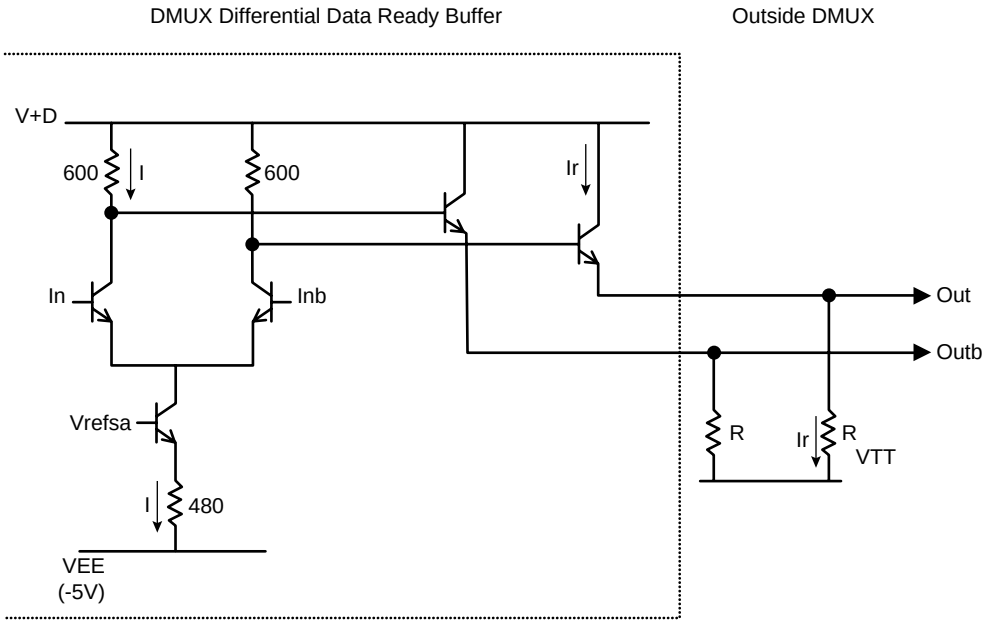


Figure 6. Data Output Buffer Schematic

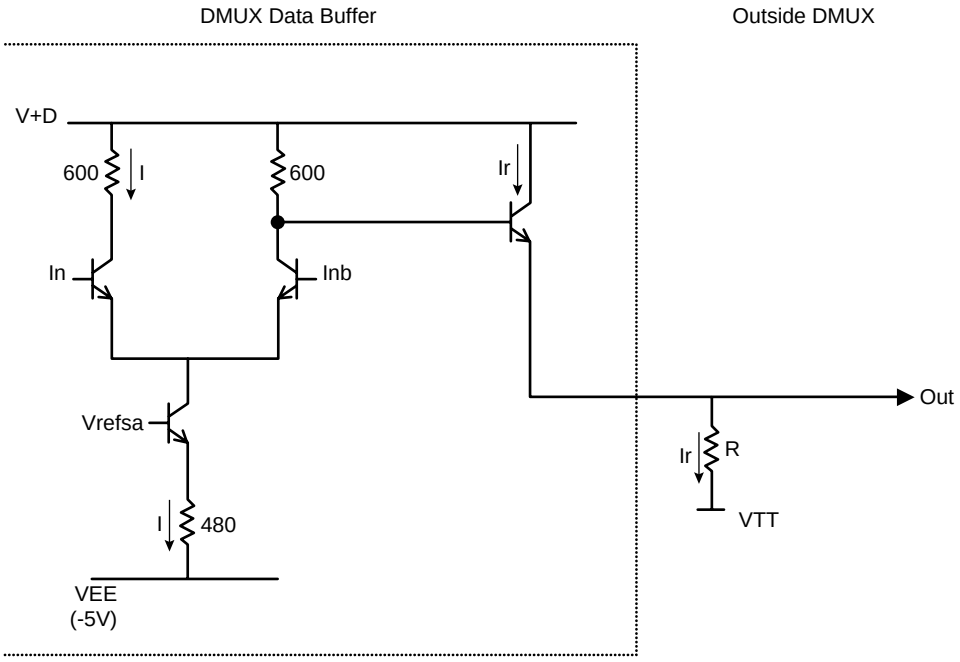
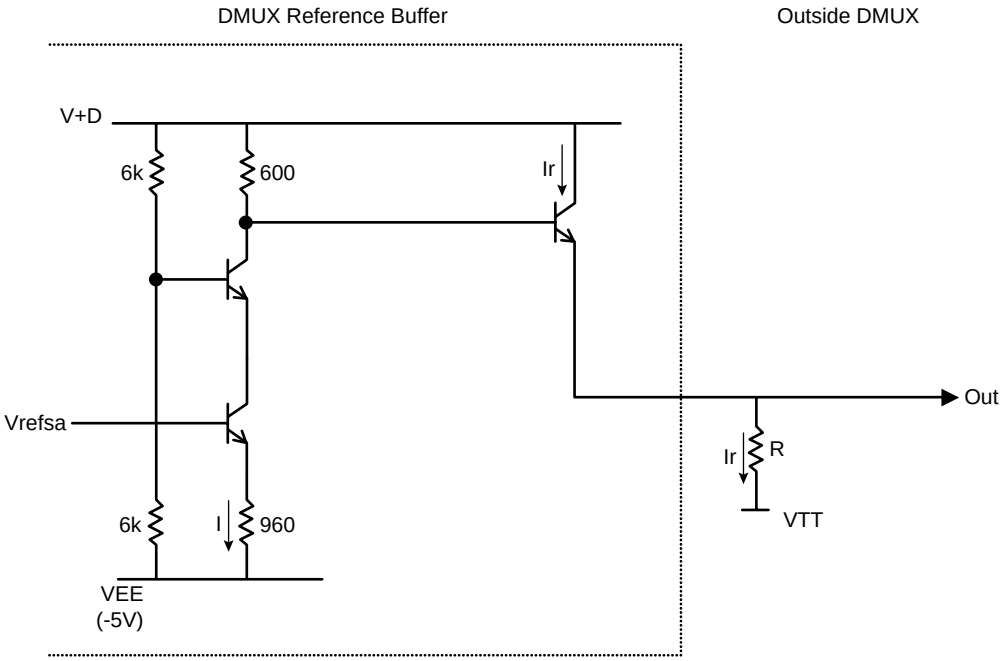


Figure 7. Reference Output Buffer Schematic



These buffers have three tunable parameters:

- V+D power supply
- Vtt power supply
- the value of the resistors R

This allows the users to tune the output voltage levels, using the formulas:

$$Voh = Vplusd - 0.9$$

$$Vol = Vplusd - 0.9 - \frac{600}{480}(4.1 + Vrefsa)$$

$$Vref = Vplusd - 0.9 - \frac{600}{960}(4.1 + Vrefsa)$$

The value of Vrefsa depends on the value of SWIADJ and on the temperature. Tests gave the following results.

Note: The 0.9 V term in the above equations should, ideally, be replaced by 0.6 V in normal operation of the device.

Table 1. Test Results

Temperature	SWIADJ (V)	Vrefsa (V)
-55°C	-0.5	-3.8
	0	-3.0
	0.5	-2.0
+25°C	-0.5	-4.0
	0	-3.0
	0.5	-1.9
+125°C	-0.5	-4.2
	0	-3.1
	0.5	-2.0

Note: These results may be linearly interpolated.

Then, to avoid a saturation on the low level you need to define a value for Vtt so that Vol > Vtt.

To choose the Vtt and R values, it is necessary to respect one important rule:

The current I_r must never exceed 36 mA, because of the reliability linked to the electromigration in the transistors.

I_r is given by the formula:

$$Ir = \frac{Vout - Vtt}{R}$$

ECL Connection at DMUX Input

The DMUX clock and data inputs are ECL inputs.

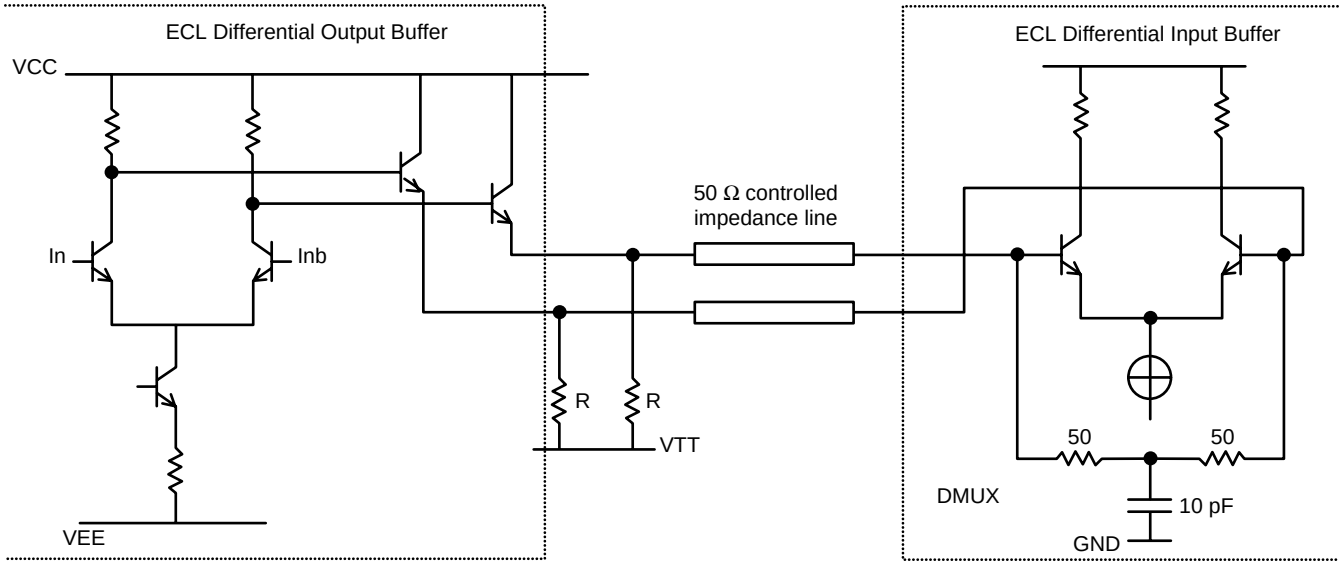
Preferably, the DMUX is used with Atmel ADC (TS8388B or TS83102G0B) and there is no compatibility issue. The device has been specifically designed to work with these ADCs.

The DMUX can indeed be connected directly to the ADC. Please refer to the "ADC and DMUX Application Note" for more information.

When the DMUX is not used with Atmel ADC, any potential compatibility issues can be solved by interfacing the device and the DMUX with an ECL translator.

Generally, the ECL translator buffers are open-emitter buffers so they need a specific interface with the DMUX input buffers. An example is given below with the PECL/ECL translator.

Figure 8. Connection Between DMUX and a Standard ECL Driver



Typically the value of the termination resistors R is 50 Ω and $V_{TT} = V_{CC}$ -2 V.

Connection Between DMUX Output and Equivalent Load

The DMUX output buffers are single-ended open-emitter buffers in order to reduce the power dissipation on the chip. This involves a particular configuration when connecting the DMUX to the load. The following is the example of 8 ports, 10 bits and ECL mode configuration.

There are two schematics: a global view of the transmission lines and a zoom on the port A transmission lines.

In some applications, a reference signal is required:

- Most of the ASIC loads have a reference input which allows to process internally the signals as pseudo-differential signals.
- The acquisition systems (such as HP16500) have an internal reference that can be tuned and which corresponds to the common mode voltage of the input signals. The common mode voltage of the DMUX outputs signals is given by the DMUX reference outputs.

The benefits of using the reference generated by the DMUX is that both the data outputs and the reference outputs suffer from the same external perturbations (for example a glitch on the power supply). So the difference of potential between the data signal and the reference signal is quite constant.

It is recommended to use the DMUX reference outputs, when possible:

- Terminate the line (for example with 50 Ω resistor)
- Avoid connecting the reference outputs of several ports (there is one reference per port): the reference voltages are not exactly identical for all the ports so there would be a surplus of current in one transistor and it will exceed the limitation of 36 mA. This may consequently damage the buffer (electro-migration for long term reliability).

If the application does not allow the user to connect all the reference outputs to its FPGA or ASIC, it is then recommended to use at least one reference from one port for all outputs (or an external reference).

In all cases, if the user does not plan to connect the reference outputs, it is mandatory to connect them to V_{TT} through a termination resistor (for example 50 Ω resistor).

Note: When the DMUX is operated in 1:4 mode or with 8 bits only, the unused ports or output data can be left floating.

Figure 9. Global View of the Transmission Lines

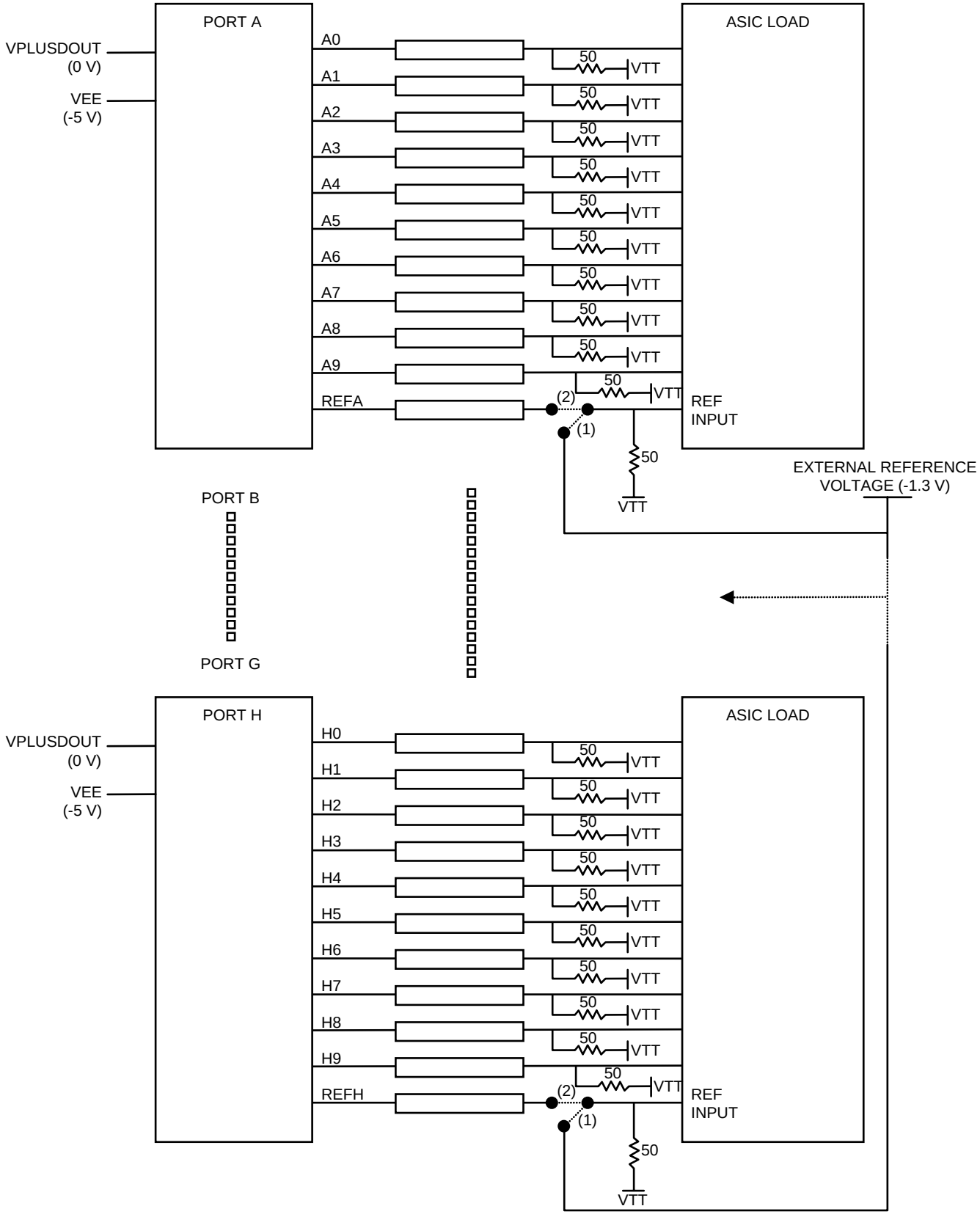
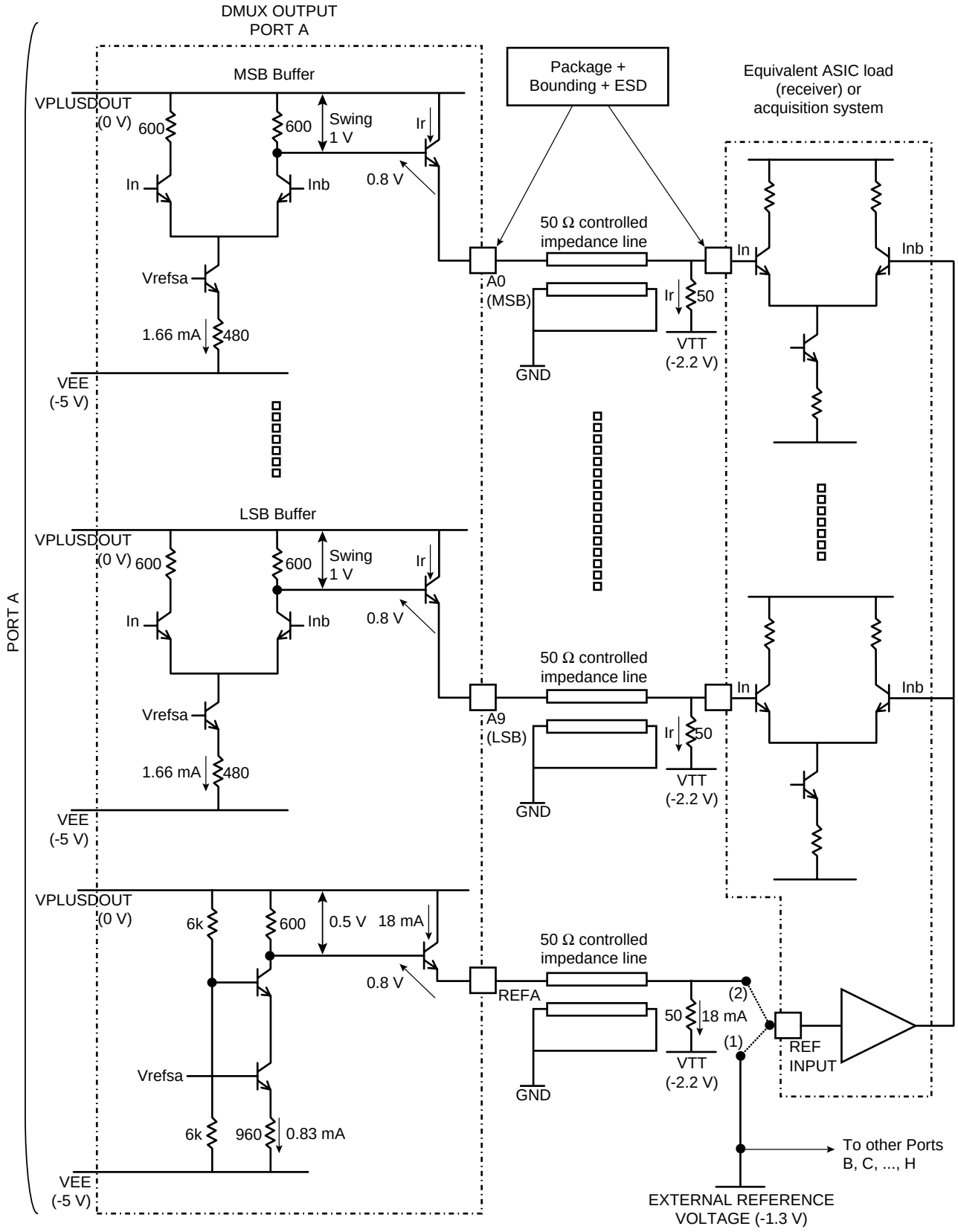


Figure 10. Zoom on the Port A Transmission Lines

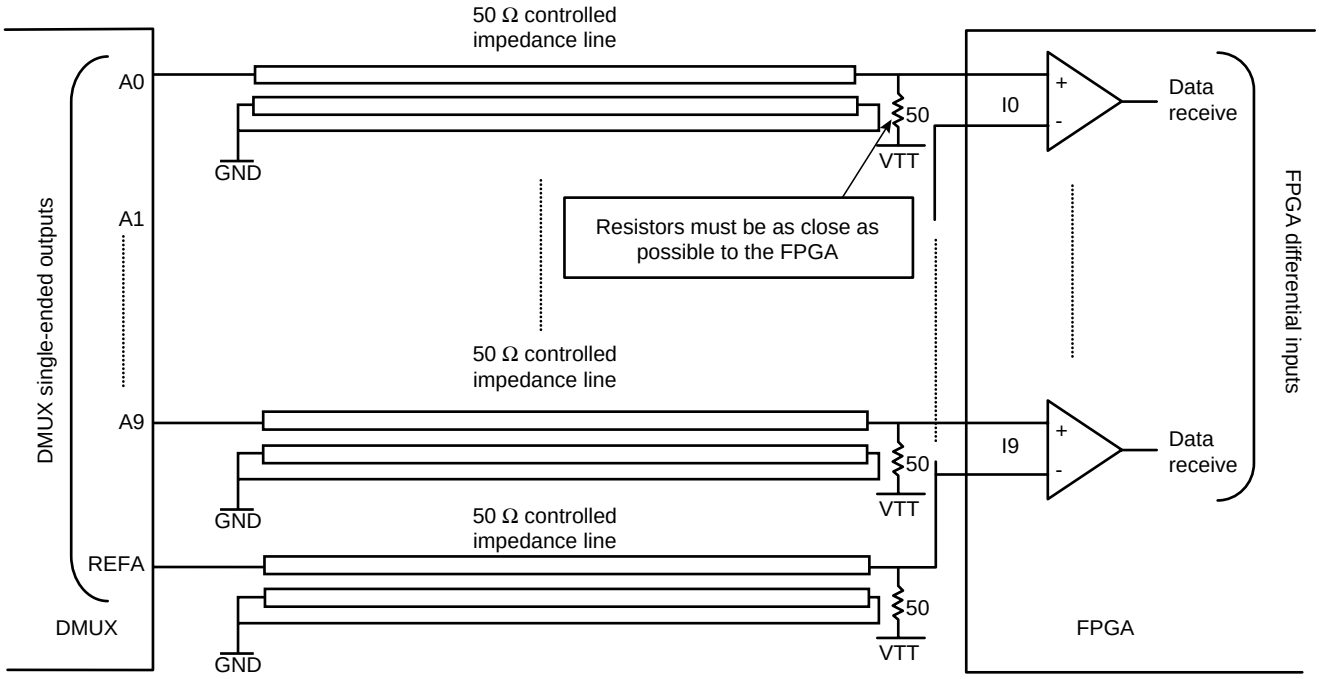


Connection Between DMUX Outputs and FPGA

Typical DMUX application: the connection to an FPGA.

Only one DMUX port is represented.

Figure 11. Principle Connection with an FPGA



Note that in case of the use of Xilinx Virtex II devices, it is possible to use the DCI feature of the FPGA and then to get rid of the termination resistors.

The typical configuration for each device is the following:

– DMUX: VPLUSD set to 2.5 V for SSTL2 class 1 output level setting
– FPGA Virtex II: SSTL2 class1 input level (2.5 V supply)

In this configuration, direct lines can be used between the DMUX output data and the FPGA inputs.

DMUX Power Supplies

In certain conditions of use of the DMUX outputs, special care should be taken as regards the configuration used for the power supplies.

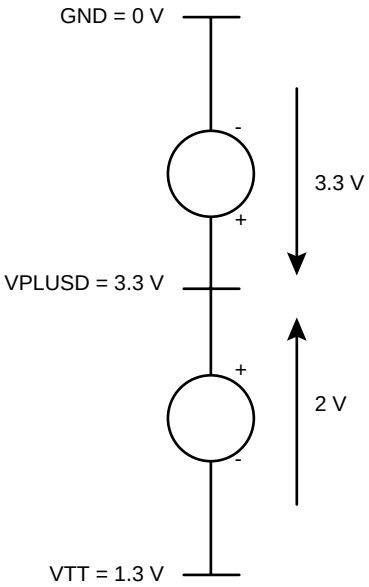
This is the case when V+D and Vtt power supplies are both different from GND.

In this configuration, there could be some conflict between the power supplies, that is why a specific method is described here to avoid such an issue.

What we recommend then is to use two power supplies. In this case, the design of the DMUX output buffers involves the V+D power supply providing the current while Vtt power supply absorbs this current.

This particular configuration is described in Figure 12, in the case of the PECL output mode.

Figure 12. DMUX Power Supplies



Current Consumption and Power Dissipation

Caution:

In the datasheet, one finds:

- The supply currents which are "worst case", which include all the currents consumed by the whole evaluation board and which must help you to size your power supplies.
- The power dissipation which takes into account only the power dissipation of the chip and which must help you to size the heatsink.

Therefore, it is not recommended to use the supply currents given in the datasheet to calculate the power dissipation of the chip. Here is a detailed calculations of the power dissipation in PECL configuration:

- power dissipation due to the logical circuitry: (31 mA x 5) + (719 mA x 5) = 3.75 W
- power dissipation due to the output buffers (see the calculation below)

Typically, V_{refsa} = -3 V

and in PECL: V+D = 3.3 V; V_{TT} = 1.3 V; V_{OL} = 1.5 V; V_{OH} = 2.5 V; V_{REF} = 2 V.

Moreover, we have the relations:

$I = (4.2 - V_{refsa})/480$ for data buffers

$I = (4.2 - V_{refsa})/960$ for reference buffers and $I_r = (V_{OUT} - V_{TT})/R$

I = 2.5 mA for data buffers and I = 1.25 mA for reference buffers

In the worst case, all the bits are at the high level: V_{OUT} = 2.5 V and each data buffer consumes a current I_r = 24 mA.

In the best case, all the bits are at the low level: V_{OUT} = 1.5 V and each data buffer consumes a current I_r = 4 mA.

Moreover the reference buffer (in the chip) consumes a constant current I_r = 14 mA.

So the power dissipation for each data buffer is:

- in the worst case: $P = (I \times 8.3\ V) + (I_r \times (V+D - V_{OH})) = 40$ mW
- in the best case: $P = (I \times 8.3\ V) + (I_r \times (V+D - V_{OL})) = 28$ mW
- in average: P = 34 mW

And the power dissipation for each reference buffer is:

- $P = (I \times 8.3\ V) + (I_r \times (V+D - V_{REF})) = 29$ mW

Finally the power dissipation due to output buffers is:

- in the worst case: P = (66 x 40 mW) + (8 x 29 mW) = 2.87 W
- in the best case: P = (66 x 28 mW) + (8 x 29 mW) = 2.08 W
- in average: P = (66 x 34 mW) + (8 x 29 mW) = 2.48 W

So the global power dissipation in the chip is:

- in the worst case: P = 2.87 W + 3.75 W = 6.62 W
- in the best case: P = 2.08 W + 3.75 W = 5.83 W
- in average: P = 2.48 W + 3.75 W = 6.23 W

Similarly, we can calculate the power dissipation and the current consumption for all the DMUX configurations.

Table 2. Power Dissipation

Output Mode	Number of Ports	Number of Bits	Calculation Results		
			Worst Case	Best Case	Average
ECL	4 ports	8 bits	4.25 W	3.86 W	4.06 W
		10 bits	4.72 W	4.22 W	4.47 W
	8 ports	8 bits	6 W	5.23 W	5.61 W
		10 bits	6.86 W	5.89 W	6.38 W
PECL	4 ports	8 bits	4.55 W	4.15 W	4.35 W
		10 bits	5.07 W	4.58 W	4.83 W
	8 ports	8 bits	6.62 W	5.83 W	6.23 W
		10 bits	7.61 W	6.63 W	7.12 W
TTL	4 ports	8 bits	5.14 W	4.65 W	4.9 W
		10 bits	5.8 W	5.19 W	5.5 W
	8 ports	8 bits	7.74 W	6.78 W	7.26 W
		10 bits	9.01 W	7.81 W	8.41 W

Table 3. Current Consumption

Output Mode	Number of Ports	Number of Bits	Calculation Results		
			Worst Case	Best Case	Average
ECL (50 Ω load)	4 ports	8 bits	0.91 A	0.27 A	0.59 A
		10 bits	1.12 A	0.32 A	0.72 A
	8 ports	8 bits	1.82 A	0.54 A	1.18 A
		10 bits	2.24 A	0.64 A	1.44 A
PECL (50 Ω load)	4 ports	8 bits	0.91 A	0.27 A	0.59 A
		10 bits	1.12 A	0.32 A	0.72 A
	8 ports	8 bits	1.82 A	0.54 A	1.18 A
		10 bits	2.24 A	0.64 A	1.44 A
TTL (75 Ω load)	4 ports	8 bits	1.22 A	0.38 A	0.81 A
		10 bits	1.51 A	0.45 A	0.88 A
	8 ports	8 bits	2.44 A	0.76 A	1.61 A
		10 bits	3.01 A	0.9 A	1.77 A

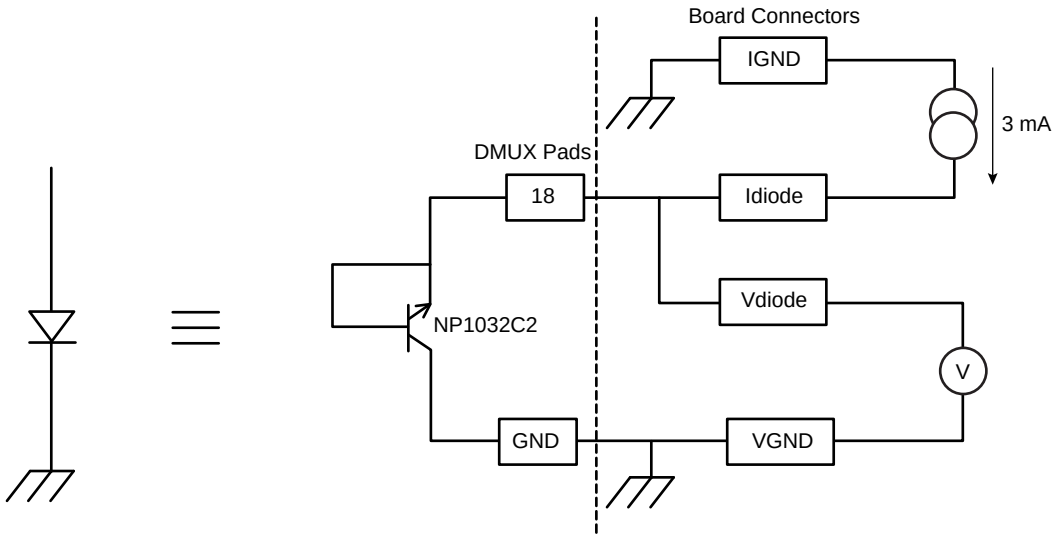
Table 4. Standard Levels

	ECL	PECL	TTL
V_{OH}	-0.8 V	+2.5 V	+2.5 V
V_{OL}	-1.8 V	+1.5 V	+0.5 V

DMUX Temperature Monitoring

The diode temperature measurement may be performed as explained in Figure 13.

Figure 13. DMUX Temperature Monitoring Diagram

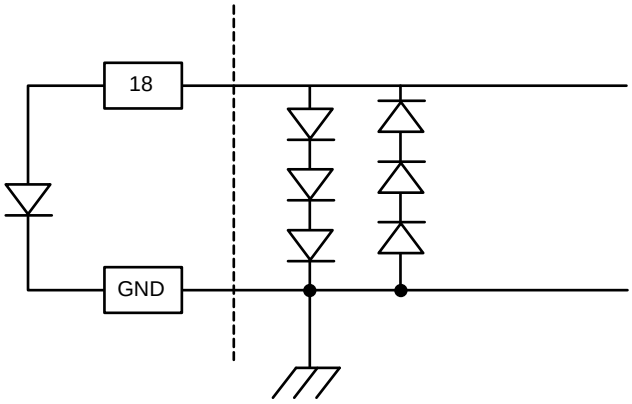


The measurement method consists in forcing a 3 mA current flowing into a diode-mounted transistor (shorted base-emitter), connected between DIODE pad and GND pad.

Be cautious with the current source polarity. The maximum Vcb for the diode is 12 V. Thus, make sure that the maximum voltage compliance of the current source is limited to a maximum of 12 V (we advise 5 V).

During a temperature measurement, some transient voltage peaks may appear while modifying the current source value. These peaks, which may not be detected with an oscilloscope (they are just too quick) may irreversibly damage the diode. That is why we strongly recommend to implement the following diodes (standard diodes) on your test board (these diodes have been implemented on the TSEV81102G0 DMUX Evaluation Board).

Figure 14. Hardware Implementation with Protection Diodes



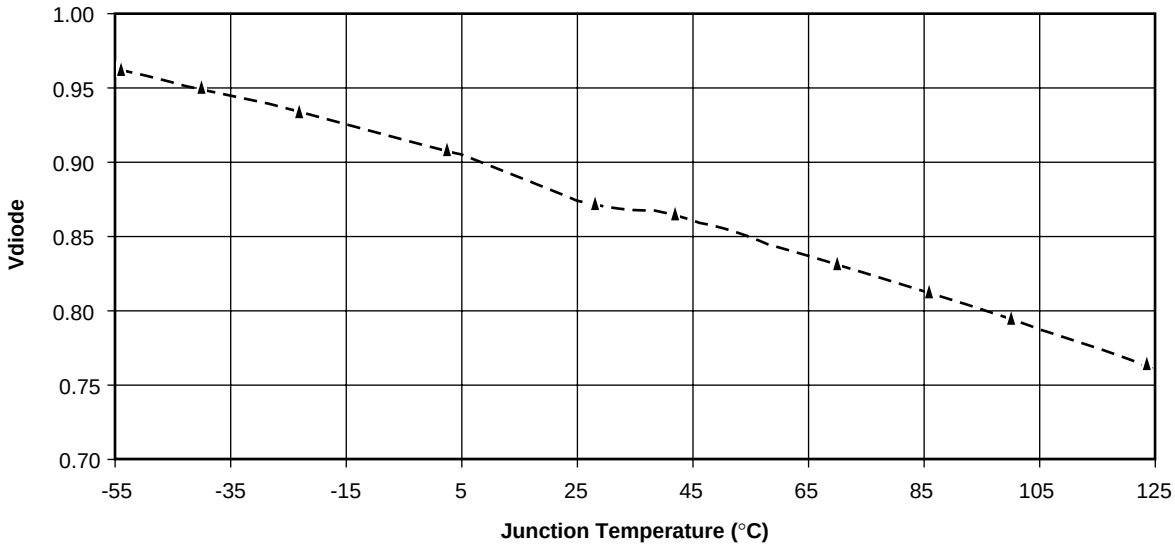
The influence of these diodes on the temperature measurement is insignificant.

The results given in Table 5 have been obtained by measuring the diode characteristic (the supplies of the DMUX were turned off).

Table 5. Diode Measurement Results with Ic = 3 mA

Junction Temperature (°C)	Vdiode
-54	0.963
-40	0.95
-23	0.934
2.5	0.908
28	0.872
42	0.865
70	0.832
86	0.813
100	0.795
123.5	0.765

Figure 15. Diode Measurement Results



Built-In Self Test (BIST)

BIST Sequence

This is a pseudo-random 10-bit generator, implemented in the DMUX. It generates a 10-bit signal at the output of the DMUX, with a period of 512 input clock. It allows to test the functionality of the DMUX without using a pattern generator or an ADC.

Only power supplies and a clock generator are needed.

For complementary information, the algorithm for this sequence is the following:

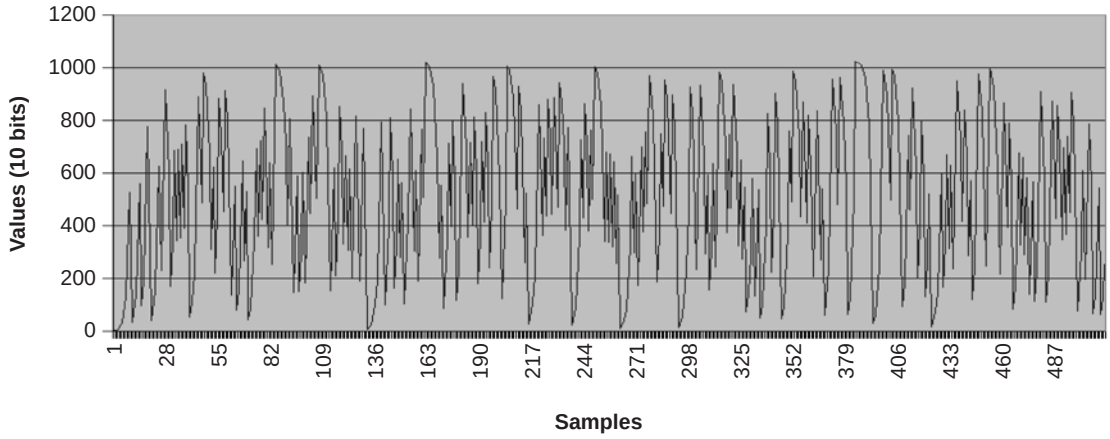
$$N(i) = \left[2 \times N(i-1) + \left[\left[\text{int}\left(\frac{N(i-1)}{256} \right) \% 2 \right] + \left[\text{int}\left(\frac{N(i-1)}{16} \right) \% 2 \right] \right] \% 2 \right] \% 1024$$

where % means "modulo".

Note: start with N(0) = 2, i = 1

Here is the BIST sequence:

Figure 16. Built-In Self Test Values



DMUX Setting in BIST Mode

here are the different required settings, in order to activate the BIST mode in the DMUX.

Table 6. DMUX Setting in BIST Mode

Function	Setting	Description
BIST	Logic 0	BIST Active
CLKINTYPE	Logic 1	DR mode
NBBIT	Logic 1	10-bit mode
RATIOSEL	Logic 0	1:8 ratio

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311, USA
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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Fax: (33) 4-42-53-60-01

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Colorado Springs, CO 80906, USA
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Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
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74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

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