Replacing AT84AS008 ADC with EV10AS008B ADC

Application Note

1. Introduction

This application note aims at providing you with a comparison and recommendations to migrate from the existing AT84AS008GL to the EV10AS008BGL.

It first compares the two versions including:

- Power supplies
- Analog and digital controls

It also describes board modifications to migrate from the existing version to the B version.

This new B series ADC is designed to ensure minimum board level design modifications and equal electrical performance.

This document applies to the following:

- AT84AS008CGL
- AT84AS008VGL
- AT84AS008MGS

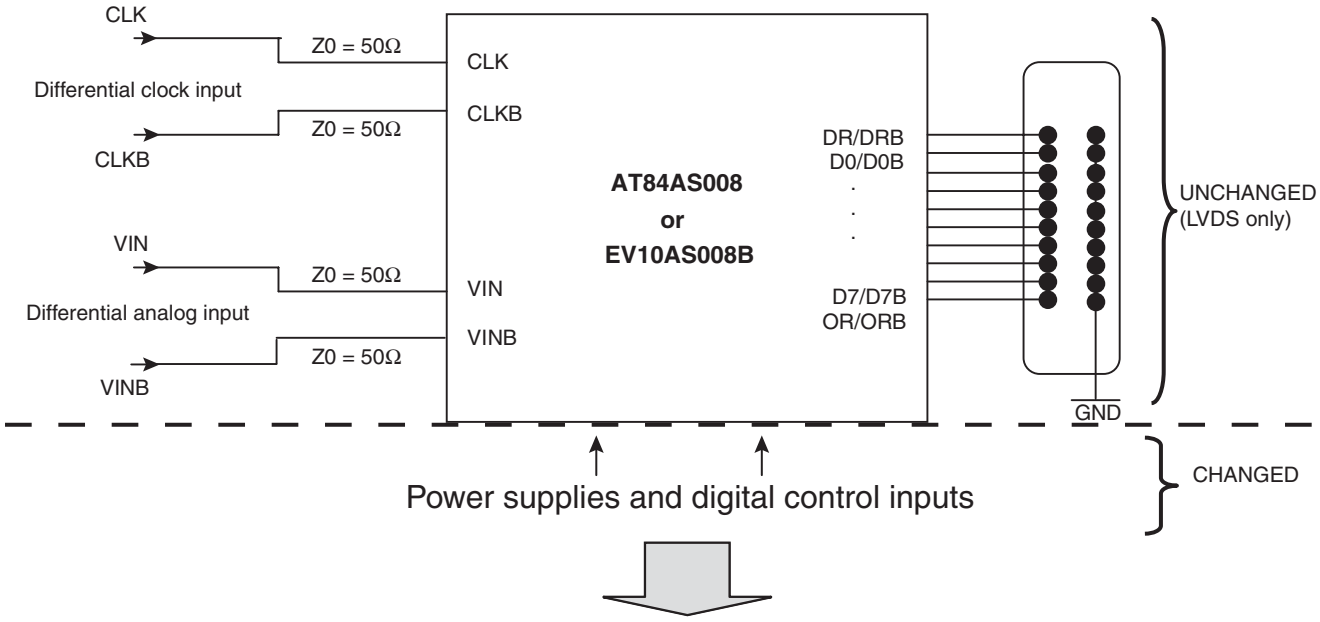
2. Comparing EV10AS008B and AT84AS008 10-bit 2.2 Gsps ADC Devices

The EV10AS008B is delivered in the same package as the AT84AS008, with same footprint, same mechanical and thermal characteristics.

The EV10AS008B has been designed in order to feature the same timing characteristics as the AT84AS008 with ascending electrical performance compatibility.

The following section discusses the similarities and differences between the AT84AS008 and the EV10AS008B.

Figure 2-1. Block Diagram



2.1 EV10AS008B Versus AT84AS008

Highlights of the differences between the two devices:

- Four power supply assignments (lower voltage):
  - ADC positive analog power supply:V_{CC}
  - ADC negative analog power supply:V_{EE}
  - ADC positive digital power supply:V_{PLUSD}
  - ADC digital ground: D_{GND}
- Four digital-control input pins active-level change (default mode is unchanged)

Table 2-1. Main Differences Between AT84AS008 and EV10AS008B Devices

Function	Symbol	AT84AS008	EV10AS008B
Analog power supplies	V_{CC}	+5V	+3.3V
	V_{EE}	–5V	–2.2V
Digital power supplies	V_{PLUSD}	+1.45V to –0.8V	+2.5V
	D_{VEE} / D_{GND}	–5V	D_{GND}
Digital control inputs	DRRB	ECL	CMOS 3.3V/LVCMOS (active low)
	B/GB, PGEB, SDAEN	0/ –5V	CMOS 3.3V/LVCMOS
Output buffer	ECL	Yes	No
	LVDS	Yes	Yes

2.2 Pinout Differences Summary

Table 2-2 is a description of the pin differences between AT84AS008 and EV10AS008B. Table 2-2 includes recommendations for forward compatibility. For more details, please refer to "EV10AS008B Pinout (Bottom View, Balls Side)" on page 4.

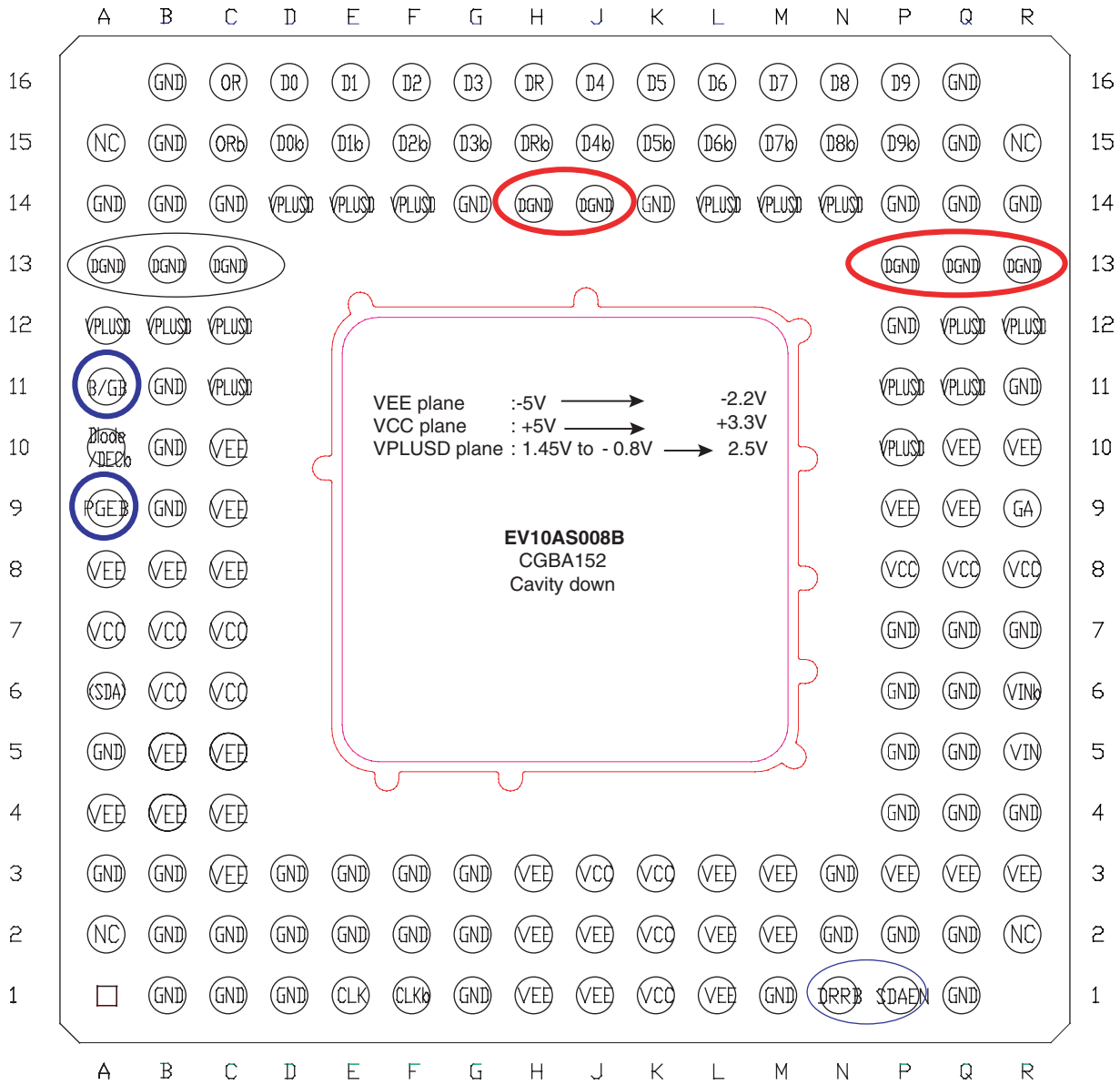
Table 2-2. Pin Differences

Pin	AT84AS008	Modification on EV10AS008B
K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	V_{CC}	Pin label compatible Voltage change from 5V to 3.3V
B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	GND	Unchanged
H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	V_{EE}	Pin label compatible Voltage change from–5V to –2.2V
P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	V_{PLUSD}	Pin label compatible Voltage change from 1.45V to 2.5V (LVDS compatible)
A13, B13, C13, P13, Q13, R13, H14, J14	D_{VEE}	To be connected to digital ground plane (0V) D_{VEE} becomes D_{GND}
R5	VIN	Unchanged
R6	VINB	Unchanged
E1	CLK	Unchanged
F1	CLKB	Unchanged
D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	Unchanged
D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	Unchanged
C16	OR	Unchanged
C15	ORB	Unchanged
H16	DR	Unchanged
H15	DRB	Unchanged
A11	B/GB	Binary mode: low level (GND) Gray mode: high level (V_{CC} instead of V_{EE})
A10	Diode/DECb	Activation of the de decimation mode with VEE –2.2V instead of –5V as in the AT84AS008
A9	PGEB	Inactive at low level (GND) and *active at high level (V_{CC} instead of V_{EE})*
N1	DRRB	Inactive at high level (VCC), *active at low level (ground)*
R9	GA	Unchanged

Table 2-2. Pin Differences

Pin	AT84AS008	Modification on EV10AS008B
A6	SDA	Unchanged
P1	SDAEN	Inactive at low level (GND) and *active at high level (V_{CC} instead of V_{EE})*
A15, R15, A2, R2	NC	Unchanged

Figure 2-2. EV10AS008B Pinout (Bottom View, Balls Side)



Analog power supplies:

- V_{EE} plane: –5V= –2.2 V
- V_{CC} plane: +5V = +3.3V

Digital power supplies (LVDS output buffers):

- D_{VEE} (–5V) pin of the AT84AS008 becomes D_{GND} (0V = digital ground plane) on the EV10AS008B. D_{GND} is the digital ground plane and should be separated from the GND plane.
- V_{PLUSD} plane +1.45V (for LVDS) to –0.8V (for ECL) becomes +2.5V for LVDS compatibility only. V_{PLUSD} is an independent power plane dedicated to ADC output buffers

Digital control inputs pins:

On the EV10AS008B the B/GB, PGEB, SDAEN, digital input control pins are activated at logic high (V_{CC} = +3.3V, +1.3V threshold) instead of logic low (V_{CC} = –5V, –1.3V threshold). The inactive level remains at GND = 0V except for DRRB.

DRRB is still active low (ground instead of VEE). It is inactive at logic high (VCC).

2.3 Getting Started with the EV10AS008B Using the Existing AT84AS008 Evaluation Board

1. Connect all three power supplies (V_{CC}, $V_{EE,}$ V_{PLUSD}) and all ground accesses, as follows:
   – V_{CC}: +3.3V
   – V_{EE} : –2.2V
   – V_{PLUSD}: +2.5V
2. Configure the digital control inputs in default mode (1).
   – B/GB floating or GND (binary mode)
   – PGEB floating or GND (disabled)
   – SDA floating or GND (disabled)
   – DRRB connected to VCC (free running)
3. Connect the analog signal as formerly (same full-scale and common mode).
4. Connect the clock signal as formerly (same level and common mode).
5. Connect the high-speed acquisition system probes to the board data outputs (LVDS compatible).
6. Switch on the power supplies.
7. Apply the clock and analog signals.

Note: Apply adequate settings if activation is requested as described in Section 2. on page 1.

Example given: DRRB (Data Ready Reset) with negative pulse (+1.3V threshold).

3. AT84AS008 To EV10AS008B: Application Information

This section discusses the board implementation of the previous changes.

3.1 Analog and Digital Power Supplies

Table 3-1. Power Supplies

Power Supplies		AT84AS008	EV10AS008B	Recommendations
Analog power supplies	V_{CC}	+5V	+3.3V	Change regulator
	V_{EE}	–5V	–2.2V	Change regulator
Digital power supplies	V_{PLUSD}	–0.8V to 1.45V	+2.5V	Change regulator
	Output buffers	D_{VEE} (–5 or –2.2V)	D_{GND} (0V)	To be connected to digital ground plane

3.2 Digital Control Inputs Implementation (DRRB, SDAEN, B/GB, PGEB)

Advantage: since the input signals are CMOS compatible, the ADC can be connected directly to FPGA or microcontroller devices. The default level remains unchanged at GND except for DRRB which is active at low level (ground) and inactive at high level (VCC).

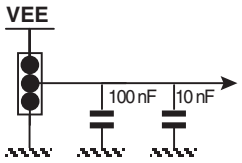
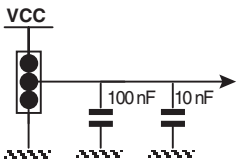
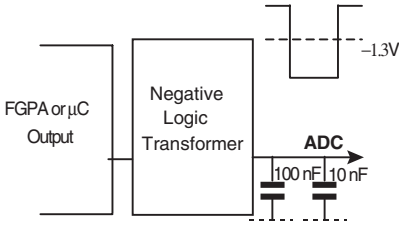
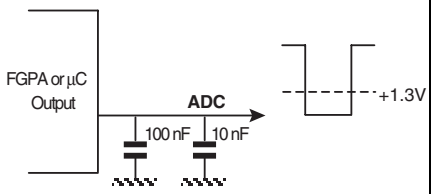
Summary: The main differences between the AT8AS008 and the EV10AS008B are the control levels.

- The threshold becomes +1.3V instead of –1.3V
- The activated level becomes +3.3V instead of –5V

The following tables outline examples of configurations used for the existing AT84AS008 and replacement part EV10AS008B. The implementation describes either pin re-assignments, removal of negative logic transformer or description of forward compatibility for V_{EE} and V_{CC} selection.

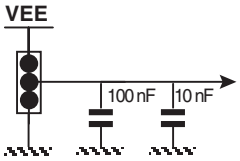
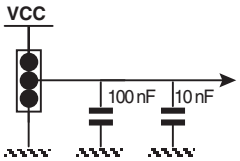
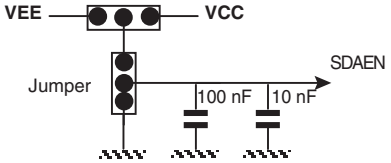
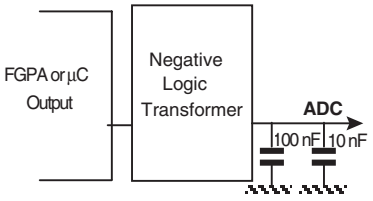
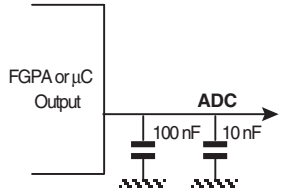
3.2.1 DRRB (Data Ready Reset)

Table 3-2.

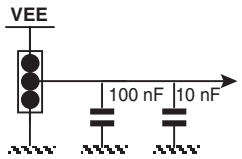
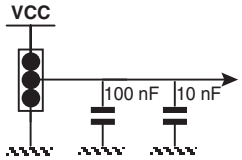
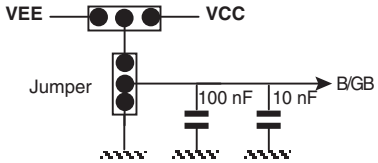
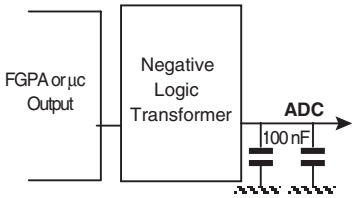
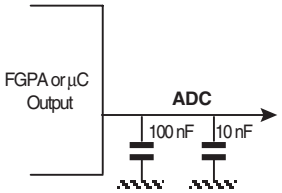
	AT84AS008 DRRB	EV10AS008B DRRB Implementation
Output clock is free-running	GND (or floating)	VCC
Output clock is in reset mode	V_{EE} (–5V) Threshold (-1.3V)	GND Threshold (+1.3V)
Electrical schematic for evaluation test Static reset		
Electrical Schematic for embedded application with microcontroller or FPGA Dynamic reset		 Note: FPGA connection -Standard LVTTL I/O (programmable 3.3V bank) -LVDS I/O

3.2.2 SDAEN (Sampling Delay Adjust Enable)

Table 3-3.

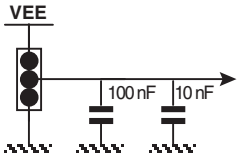
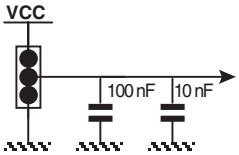
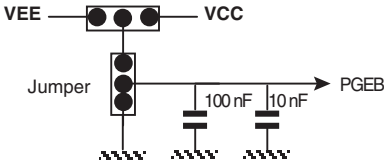
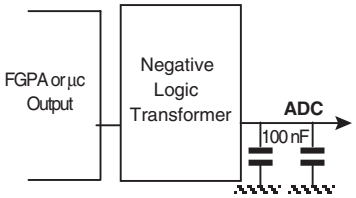
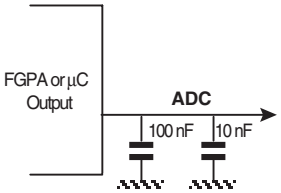
	AT84AS008 SDAEN	EV10AS008B SDAEN Implementation
Disable	GND (or floating) Default mode	GND (or floating) Default mode
Enable	V_{EE} (–5V) Threshold (–1.3V)	V_{CC} (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test AT84AS008 or EV10AS008B compatible board design		
Electrical schematic for embedded application with microcontroller or FPGA		 Note: FPGA connection -Standard LVTTL I/O (programmable 3.3V bank) -LVDS I/O

3.2.3 B/GB (Binary or Gray Output Coding)

	AT84AS008 B/GB	EV10AS008B B/GB Implementation
Binary mode	GND (or floating) Default mode	GND (or floating) Default mode
Gray mode	V_{EE} (–5V) Threshold (–1.3V)	V_{CC} (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test: AT84AS008 or EV10AS008B compatible design		
Electrical schematic for embedded application with microcontroller or FPGA		 Note: FPGA connection -Standard LVTTL I/O (programmable 3.3V bank) -LVDS I/O

3.2.4 PGEB (Pattern Generator Enable)

Table 3-4.

	AT84AS008 PGEB	EV10AS008B PGEB Implementation
Disable	GND (or floating) Default mode	GND (or floating) Default mode
Enable	V_{EE} (–5V) Threshold (–1.3V)	V_{CC} (+3.3V) Threshold (+1.3V)
Electrical schematic for evaluation test		
Electrical schematic for evaluation test: AT84AS008 or EV10AS008B compatible board design		
Electrical schematic for embedded application with microcontroller or FPGA		 Note: FPGA connection -Standard LVTTL I/O (programmable 3.3V bank) -LVDS I/O

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