Application Note

1. Introduction

This application note aims at providing you some recommendations to help you interface the AT84CS001 DMUX to e2v ADCs (TS83102G0B 10-bit 2 Gsps ADC and AT84AS008 10-bit 2.2 Gsps ADC). It first presents how to connect the DMUX to these ADCs and then how to set each DMUX and ADC to offer the best performance for each device.

This document applies to the:

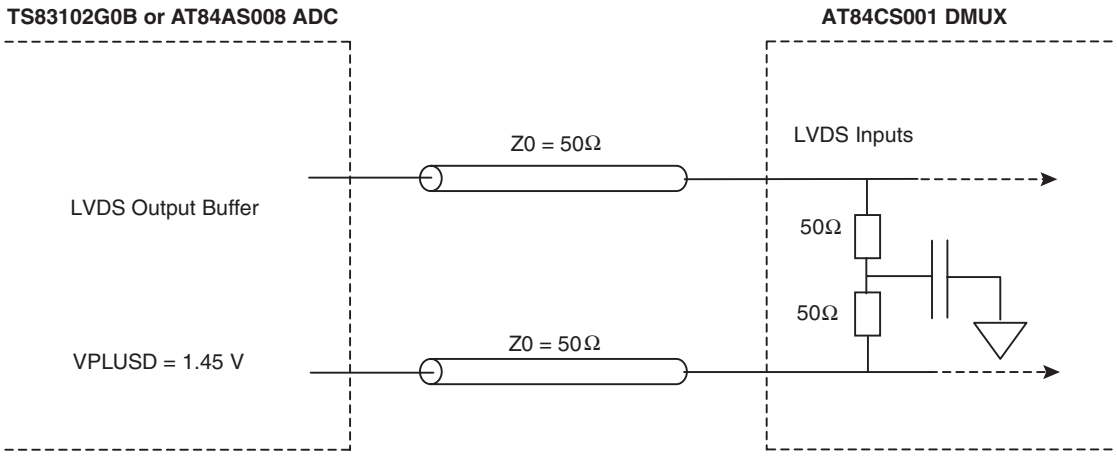
- AT84CS001 10-bit 2.2 Gsps DMUX
- TS83102G0B 10-bit 2 Gsps ADC
- AT84AS008 10-bit 2.2 Gsps ADC

2. AT84CS001 DMUX and e2v ADC Interface

When used with e2v AT84CS001 DMUX, e2v TS83102G0B 10-bit 2 Gsps and AT84AS008 10-bit 2.2 Gsps ADCs have to be set in LVDS output mode. This requires to set the V_{PLUSD} output power supply of the ADC to 1.45V.

Once the ADC is set in LVDS, it can be directly connected to the DMUX as the DMUX data and clock input buffers are already on-chip 2 x 50Ω terminated as described in Figure 2-1 on page 1.

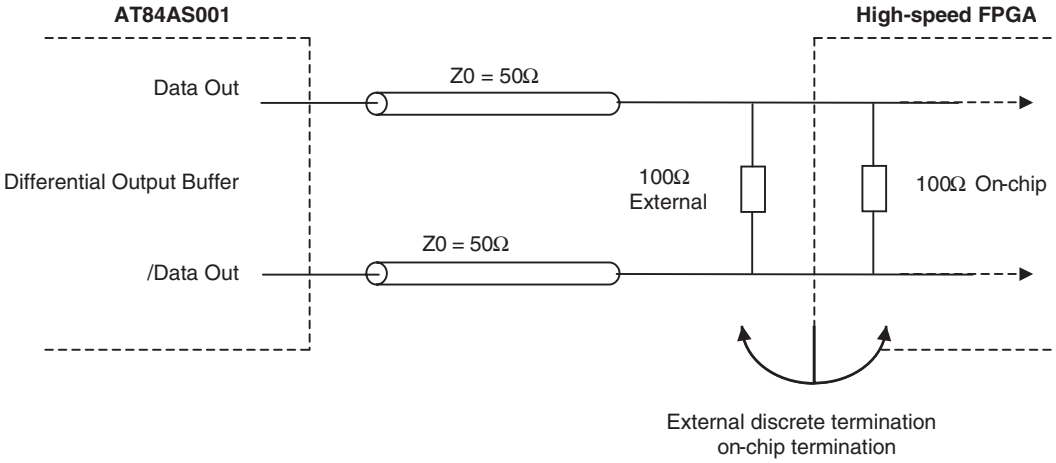
Figure 2-1. AT84CS001 DMUX and TS83102G0B or AT84AS008 ADC Interface



3. AT84CS001 DMUX High-speed FPGA Interface

The output data and clock of the AT84CS001 DMUX devices are LVDS and needs to be 100Ω terminated (either by discrete 100Ω resistors or inside the FPGA if this feature is available in the FPGA).

Figure 3-1. AT84CS001 Output Data and Clock Interface to a High-speed FPGA in LVDS



4. AT84CS001 DMUX Settings

4.1 ASYNCRST Reset signal

The ASYNCRST signal frequency should be 200 MHz maximum and the reset pulse should be 1 ns minimum. ASYNCRST is active high.

The ASYNCRST reset is not necessary to start the DMUX but it is required when the settings of the DMUX are changed during operation (STAGG, SLEEP, CLKTYPE, DRTYPE). It is also required when you need to ensure that the first data will be output on port A. It is the case when several DMUXes have to be synchronized to one another. If the AT84CS001 DMUX device is used with the AT84AS008 ADC, it is possible to perform the resets on both devices using the same differential signal with the true signal used for the ASYNCRST of the DMUX and the false signal used for DRRB.

Please refer to the “ADC and DMUX Synchronization Application note” (reference 5442) for more information.

4.2 Double Data Rate

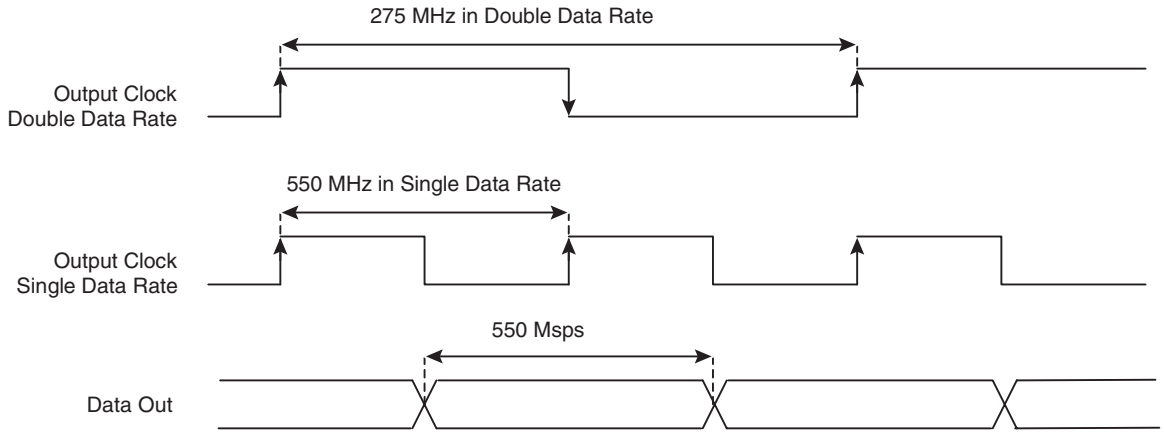
4.2.1 CLKTYPE

The TS83102G0B and AT84AS008 ADCs provide a double data rate output clock (the output clock is half the sampling clock frequency). This requires the DMUX to be also set in double data rate at its input (CLKTYPE = *1*, left floating or connected to ground via a 10 kΩ resistor or connected to V_{CCD}).

4.2.2 DRTYPE

The AT84CS001 works either in single data rate (DR mode, DRTYPE connected to V_{CCD} or left floating or connected to ground via a 10 kΩ resistor) or in double data rate (DR/2 mode, DRTYPE connected to ground via 10Ω).

Figure 4-1. AT84CS001 Single or Double Data Rate Timings (Examples)



4.3 CLKDACTRL

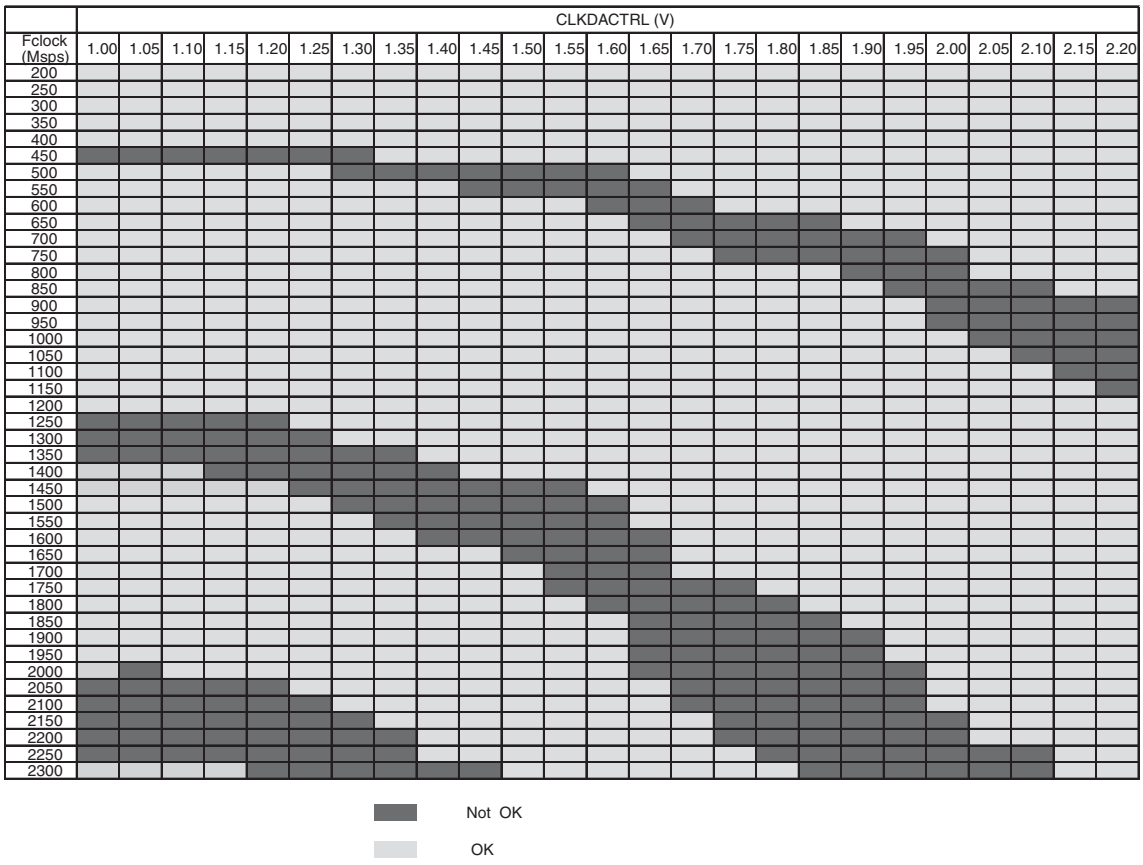
A delay cell is implemented on the DMUX input clock path to allow the user to adjust the timings between the data and the clock at the DMUX input. Given a sampling frequency, there are allowed and forbidden values for CLKDACTRL for which the DMUX will work properly. The mapping between the clock frequency and the CLKDACTRL value is given in Figure 4-2 on page 4. This table shows explicitly the values of CLKDACTRL which ensure a proper operation of the device with respect to a given sampling frequency (assuming the clock is centered on the middle of the data).

For example, if you intend to use the AT84AS008 device at 2.2 Gsps fixed data rate, CLKDACTRL can be set to 1.4V to 1.65V or 2.05V to 2.2V for proper operation. If you intend to use the AT84AS008 device at 2 Gsps, then CLKDACTRL should be set to 1.1V to 1.55V or 2V to 2.2V.

Finally, if your application requires to sweep the sampling frequency, you may have to use two or more values of CLKDACTRL for given frequency subranges. For example, if you intend to use the ADC with a sampling clock frequency ranging from 200 MHz to 2.2 GHz, any value of CLKDACTRL works for the operation from 200 MHz to 400 MHz. Then for operation from 400 MHz to 850 MHz, CLKDACTRL can be set to 2.2V. For operation from 850 MHz to 1800 MHz, CLKDACTRL can be set to 1.85V. And finally, from 1800 MHz to 2200 MHz, CLKDACTRL can be set to 1.55V.

If you set CLKDACTRL to 1.5V for example and sweep the ADC clock frequency from 200 MHz to 2.2 GHz, you will see a significant degradation of the performance of the ADC between 500 MHz and 550 MHz and between 1450 MHz and 1650 MHz.

Figure 4-2. CLKDACTRL Operating Range versus the Sampling Clock Frequency (Ambient Temperature and Typical Power Supplies)

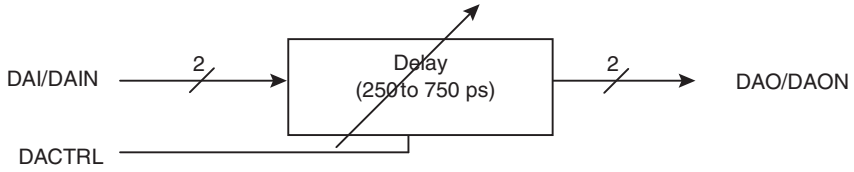


4.4 DACTRL

The AT84CS001 features a standalone delay cell which is only an additional function in case a delay cell may be required in the application (for clock monitoring for example). It is not necessary to use this function in most of the applications. However, if this function is of help, it is very easy to implement:

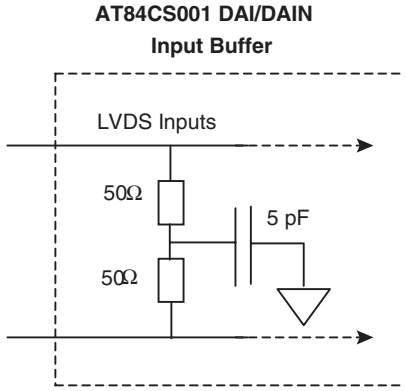
- DAI/DAIN is the differential input (LVDS)
- DACTRL is used to control the delay (from 250 ps to 800 ps for DACTRL varying from V_{CCD} / 3 to (2 x V_{CCD}) / 3
- DAO/DAON is the differential delayed output signal (LVDS)

Figure 4-3. Standalone Delay Cell Block Diagram



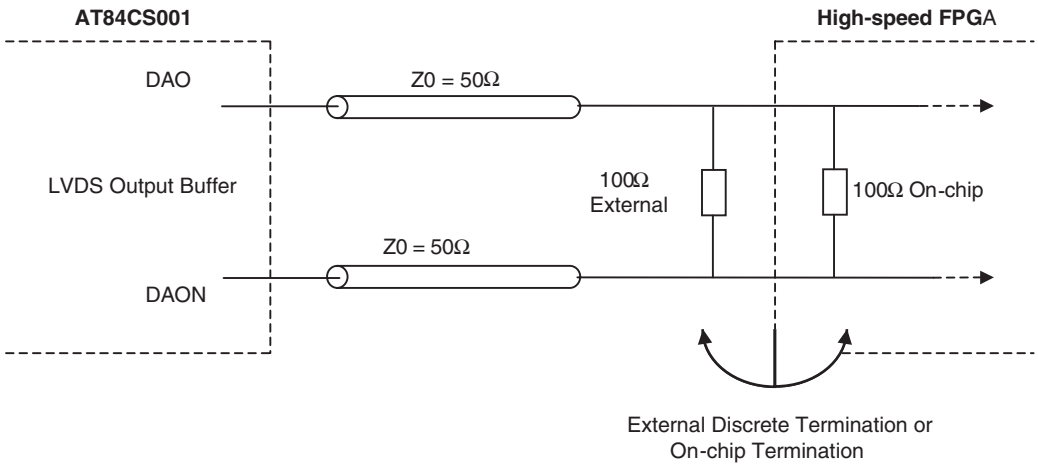
The input buffer for DAI/DAIN is described in Figure 4-4. As it is on-chip already +2 x 50Ω terminated the 100Ω LVDS external termination is not required.

Figure 4-4. DAI/DAIN Input Buffer



The output buffer for DAO/DAON is the same as for the output data and clock. As it is LVDS, a 100Ω LVDS external termination is required as described in Figure 4-5.

Figure 4-5. DAO/DAON Output Buffer Termination



4.5 SLEEP, STAGG, RS, BIST

Table 4-1. AT84AS001 Mode Settings

Table 4-2.

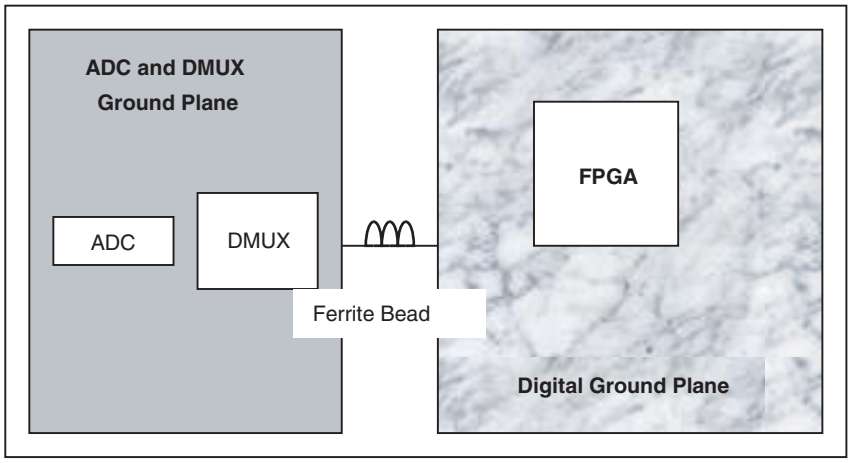
Function	Logic Level	Electrical Level	Description
SLEEP	0	10Ω to ground	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10kΩ to ground	Normal conversion
		N/C	
STAGG	0	10Ω to ground	Staggered mode
	1	10 kΩ to ground	Simultaneous mode
		N/C	
RS	0	10Ω to ground	1:2 ratio
	1	10 kΩ to ground	1:4 ratio
		N/C	
BIST	0	10Ω to ground	BIST
	1	10 kΩ to ground	Normal conversion
		N/C	

5. Grounding and Power Supplies

5.1 Common Ground Plane

It is recommended to use the same common ground plane for both the ADC and the DMUX but to separate this common plane from the digital ground plane used for the digital part of the system (FPGA for example). These two ground planes will have to be reunited by one point (via a ferrite bead, see Figure 5-1 on page 6.

Figure 5-1. Schematic View of the System Board Ground Plane (Example)



5.2 Power Supply Planes

The ADC (TS83102G0B or AT84AS008) require 3 power supplies:

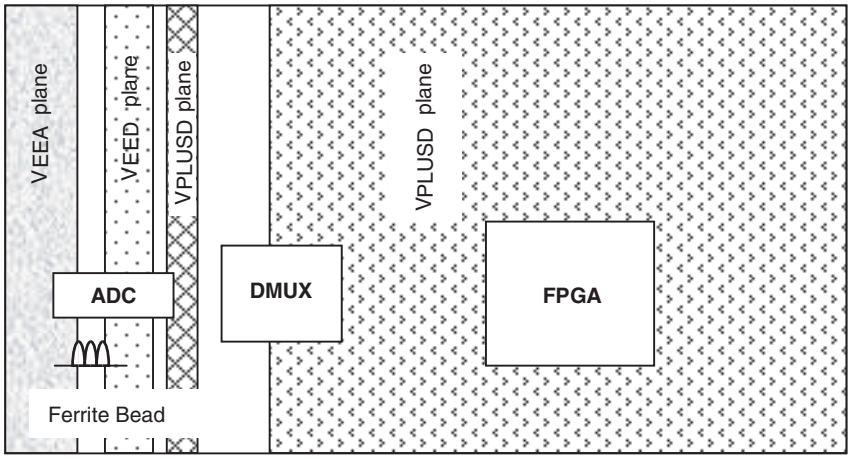
- V_{EE} = -5V analog and V_{EED} = -5V digital
- V_{CC} = 5V
- V_{PLUSD} = 1.45V

The AT84CS001 DMUX requires two power supplies:

- V_{CC} = 3.3V
- V_{PLUSD} = 2.5V

Five different planes are required for the ADC and the DMUX. It is recommended to use the same layer for both V_{EE} and V_{EED} separate planes which can be reunited by a ferrite bead (as illustrated in Figure 5-2).

Figure 5-2. Schematic View of the ADC -5V Planes (Example)



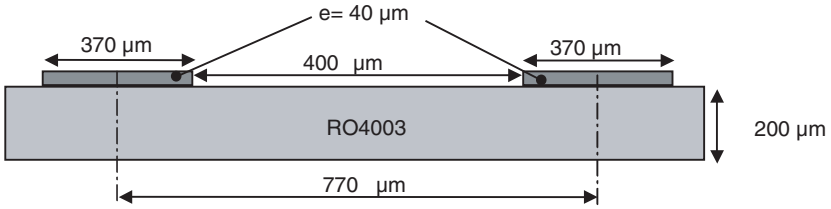
For more information concerning the power supplies decoupling and bypassing, please refer to the device datasheet (reference 5404 and 5402 for the AT84AS008 and AT84CS001 devices respectively).

5.3 Board Layout Recommendations

It is necessary to ensure that all the lines at the input of the ADC and at the output of the DMUX are matched to within 2 mm. As all data lines are differential, it is also necessary that each line of a differential pair is matched in length within 1 mm.

Figure 5-3 gives the layout rule used on RO4003 for differential signals.

Figure 5-3. 50Ω Matched Line on RO4003 Layout (Differential Signal)



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