Input/Output Termination Techniques

Introduction

This document provides the Atmel ADCs and DMUX users with the different termination techniques to be used with Atmel products. A wide panel of configurations for the analog and clock inputs as well as for the data outputs are described in detail.

The principles of each technique are also presented so that one can eventually choose the proper implementation at the input and output of our products, considering one's application.

Finally, this document is not exhaustive. Nevertheless, it covers a wide area in terms of IO termination techniques.

Input/Output Termination Techniques

Application Note

TS83 ADC Family

TS81 DMUX Family

Rev. 2169A–BDC–07/02

Analog Input Termination Techniques

There are many different termination techniques, which can be used to reduce the impact of the transmission line effects. An overview of the Standard Input termination methods, which can be used for Atmel ADCs analog inputs, is provided in the following sections.

Since Atmel ADCs are both single-ended and differential-compatible, both cases will be treated in the next sections.

Single-ended Configuration

The following figure illustrates two input configurations, when the single-ended mode is chosen for the analog input. Here, the common mode of the driving system is assumed to be the same as the one for the analog input of the ADC (Ground).

Figure 1. Configuration without Additional Termination Resistor

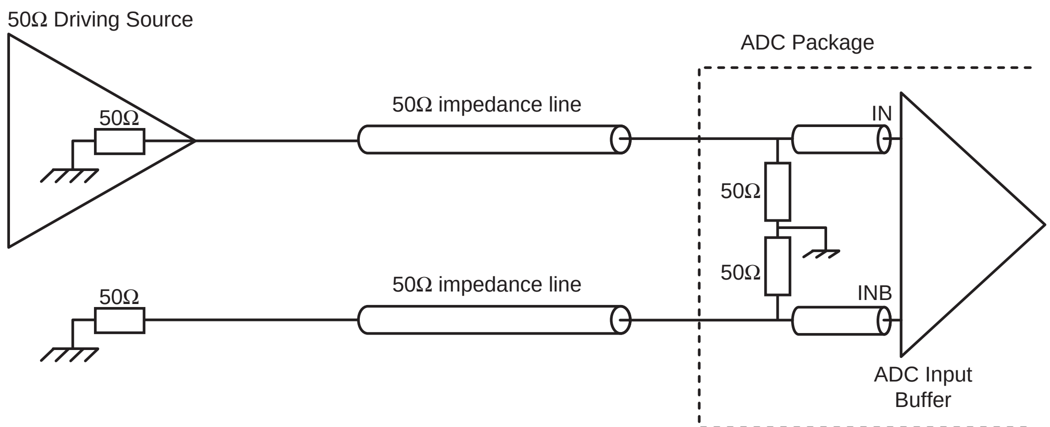
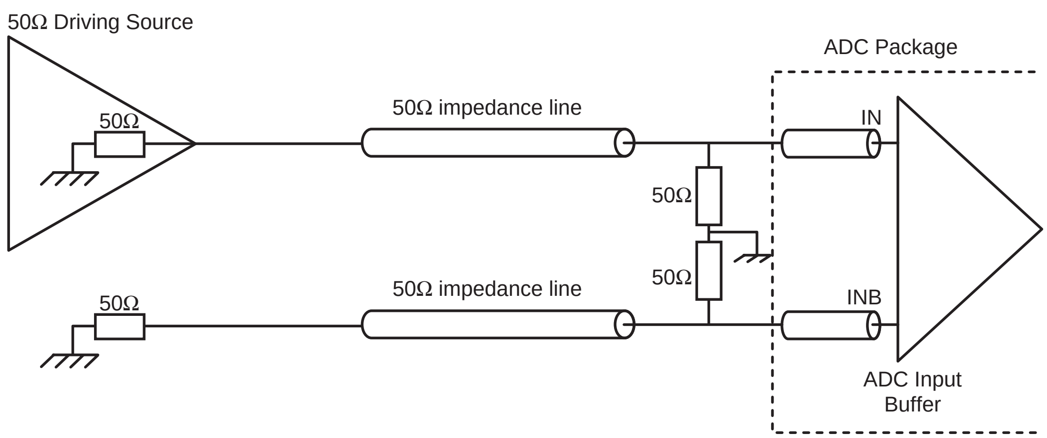


Figure 2. Configuration with 50Ω Termination Resistor



The first configuration may well be used in the case of an ADC device featuring an internal 50Ω termination (inside the cavity for the TS83102G0 10-bit 2 Gsps ADC and on package for the TS8388BG 8-bit 1 Gsps ADC).

The second configuration should be used when the differential analog input of the device is not already 50Ω terminated.

If the system, which is driving the analog input, needs to be terminated externally, the termination techniques are the following.

Figure 3. Configuration without Additional Termination Resistor

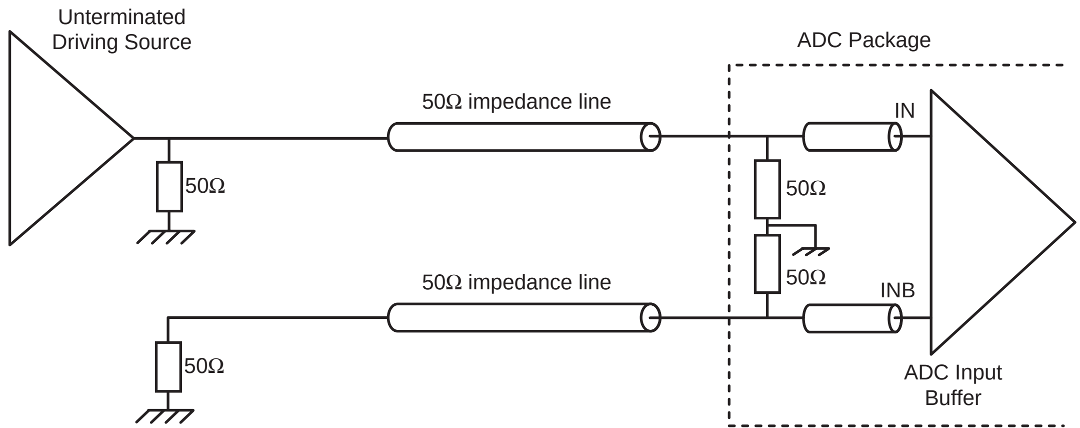
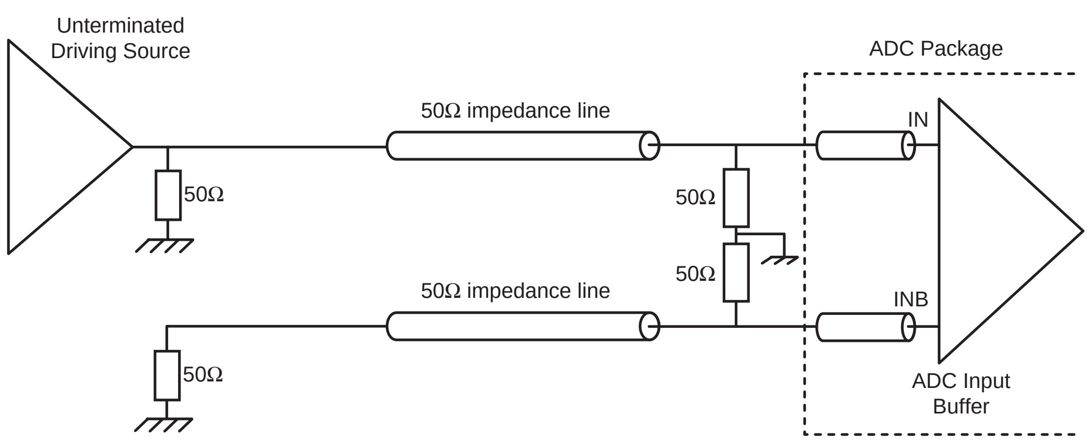
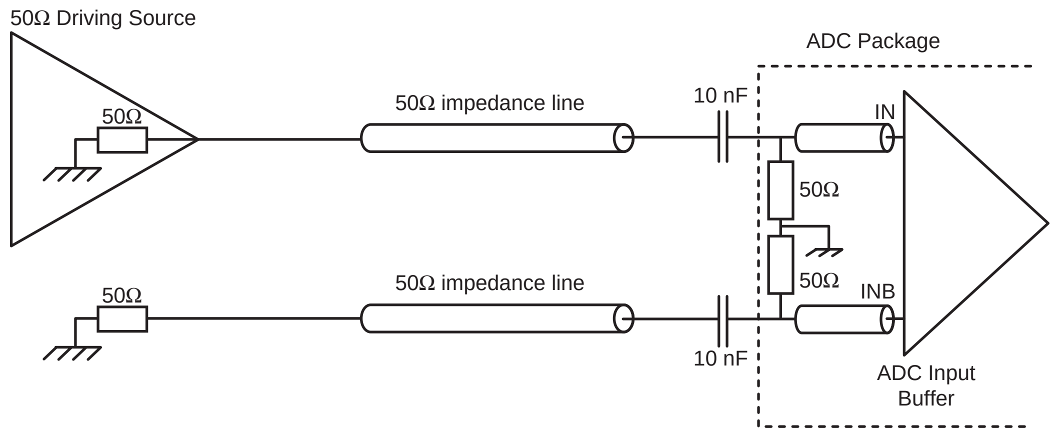


Figure 4. Configuration with 50Ω Termination Resistor



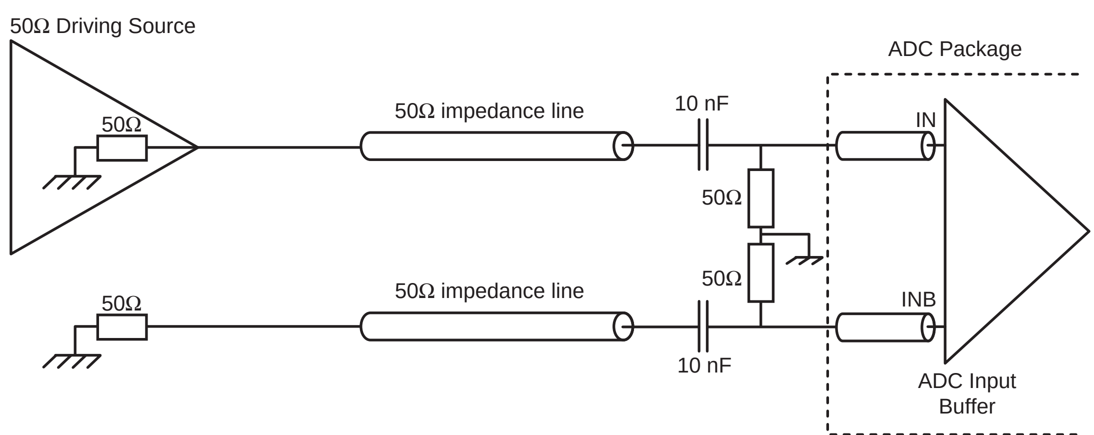
In all the previous configurations, it was assumed that there was no need to adjust the common mode (CM). If the common mode from the driving device is not the same as the one specified for the analog input of the ADC (GROUND), the user may have to choose between the configurations illustrated below.

Figure 5. Configuration without Additional Termination Resistor and with Coupling Capacitor



Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

Figure 6. Configuration with 50Ω Termination Resistor and with Coupling Capacitor



If the driving system has to be terminated, a 50Ω resistor has to be connected between the output of the system and the ground, as already described in the previous sections.

Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

Differential Configuration

When the analog input is to be used in differential mode and assuming that the common mode of the driving system is the same as the one for the input of ADC (Ground), the possible configurations are the following:

Figure 7. Configuration without Additional Termination Resistor

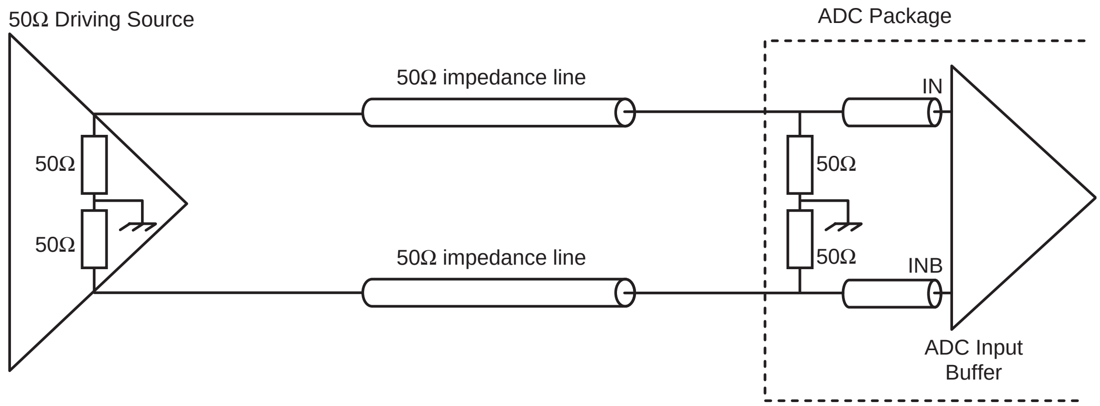


Figure 8. Configuration with Differential 50Ω Termination Resistors and with Grounded Middle Point

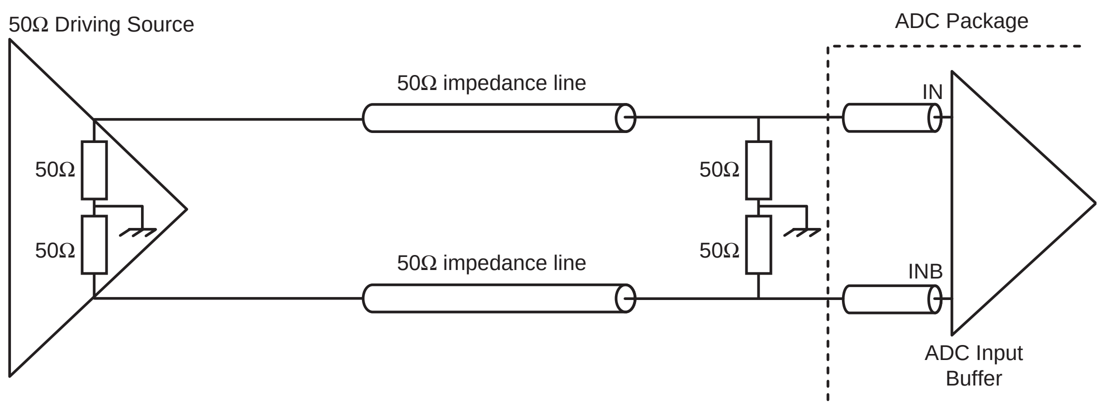
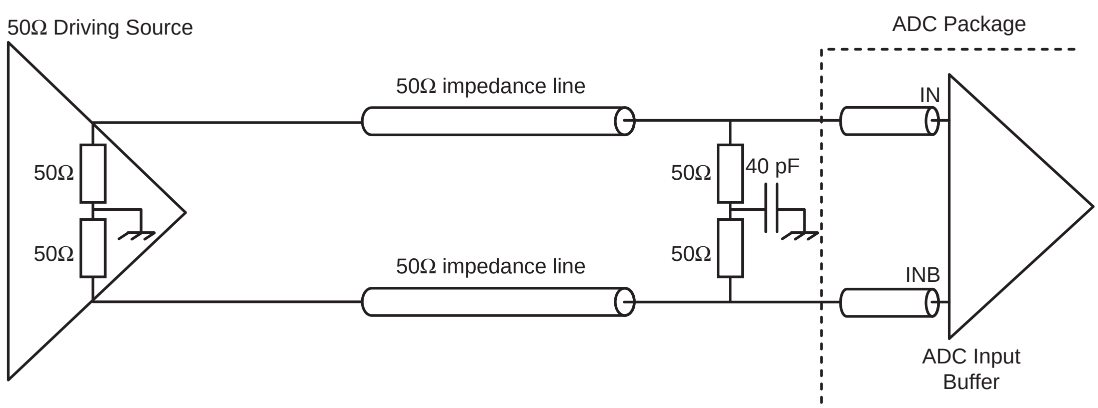
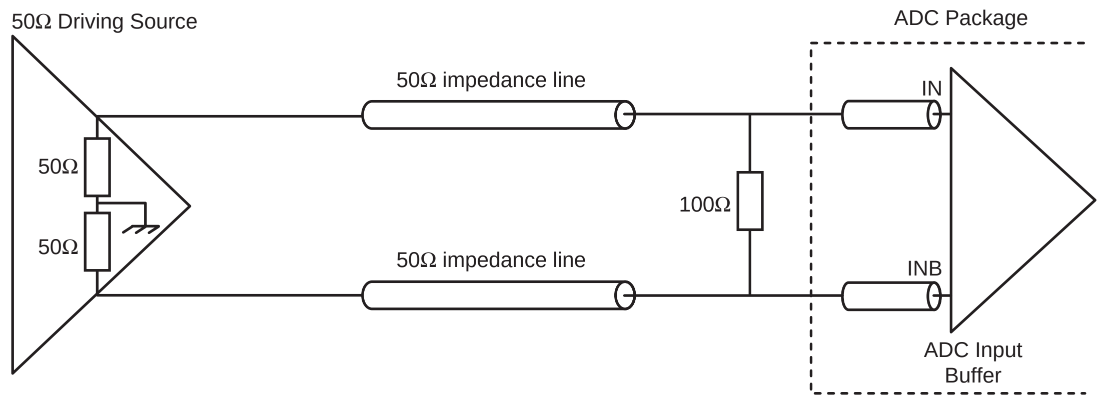


Figure 9. Configuration with Differential 50Ω Termination Resistors and with Decoupled Middle Point



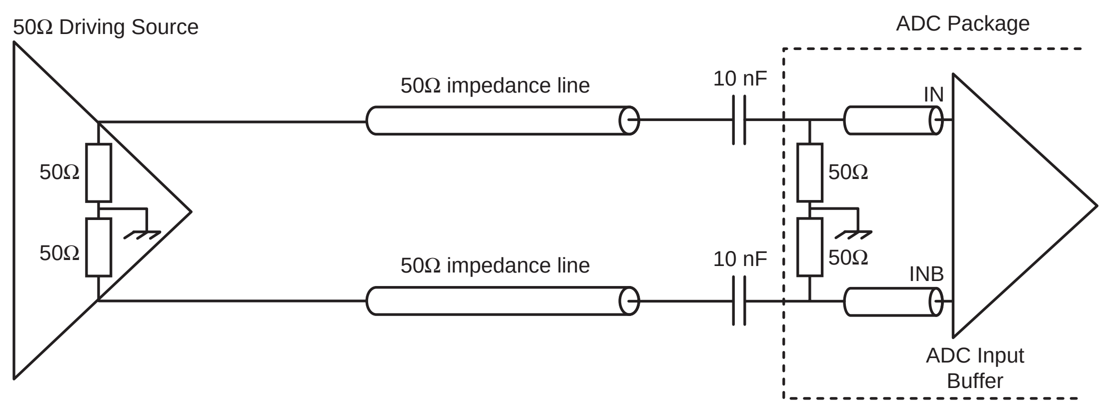
Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

Figure 10. Configuration with Differential 100Ω Termination Resistors and with Floating Middle Point



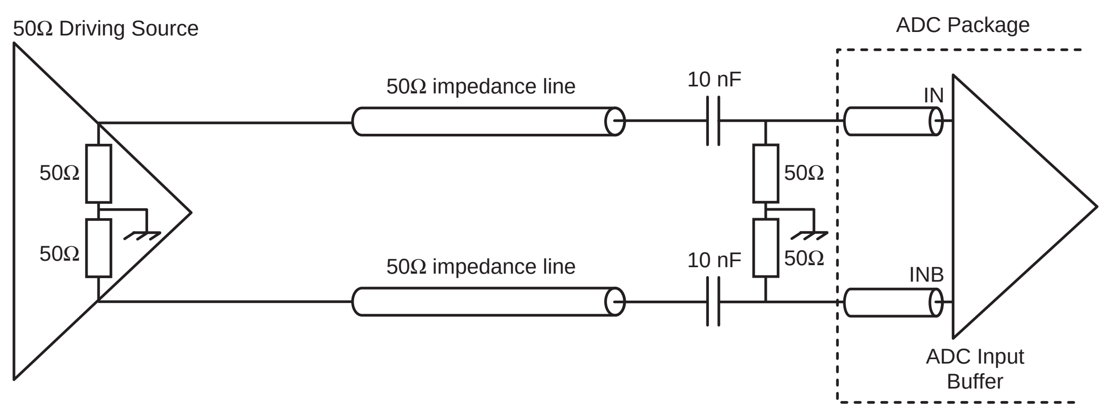
If the common mode of the driving system is not the same as the one of the input of the ADC, the previous configurations become.

Figure 11. Configuration without Additional Termination Resistor



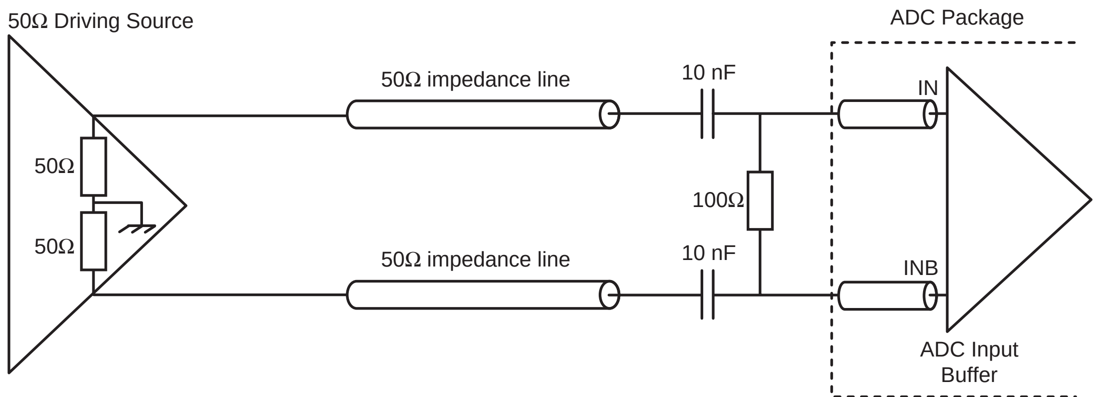
Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

Figure 12. Configuration with Differential 50Ω Termination Resistors and with Coupling Capacitors



Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

Figure 13. Configuration with Differential 100Ω Termination Resistors and with Coupling Capacitors



Note: The values of the coupling capacitors are given for information only. They may change depending on the input frequency.

The same schemes are valid when the driving system is not terminated. In these cases, the user only has to add the external 50Ω resistors on both outputs of the driving system in the schemes.

The user may only have a single-ended generator to drive the ADC input differentially (preferred way at high sampling rates). In this case, the user still has the opportunity to use a balun. The different configurations in this mode of operation are described in the next section.

Configuration with a Balun

The following section only represents the three general cases illustrating the use of a balun to convert the single-ended signal from the generator into a differential signal for the ADC input. The different cases with an unterminated driving system have not been presented.

The user can refer to the schemes given previously for these configurations.

Figure 14. Configuration without Additional Termination Resistor

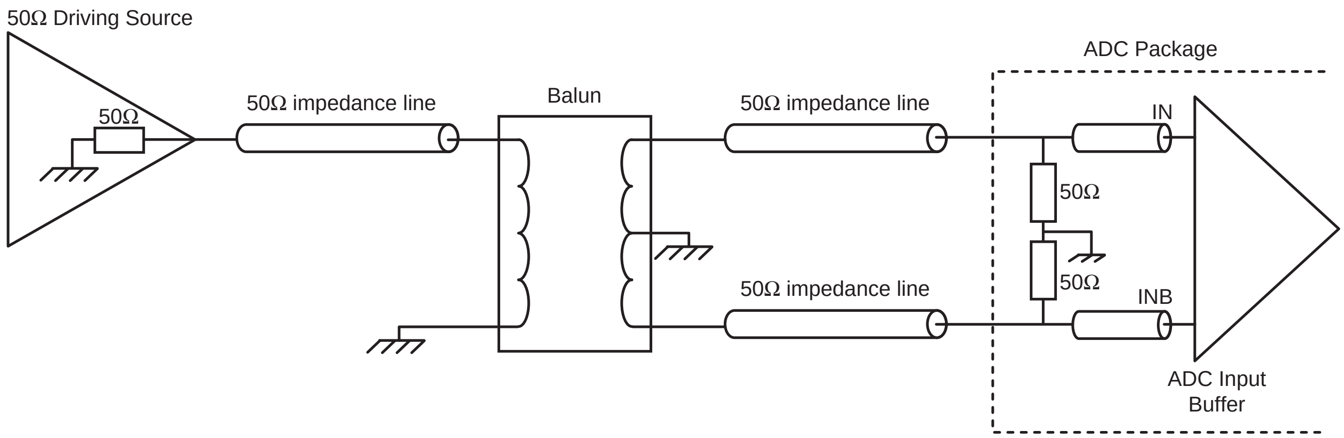


Figure 15. Configuration with Differential 50Ω Termination Resistors and with Grounded Middle Point

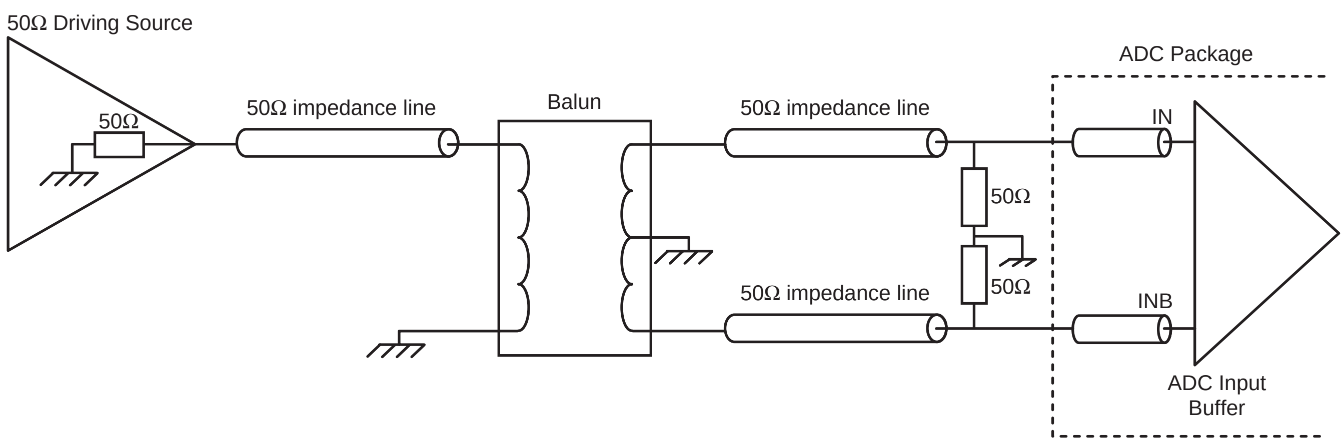
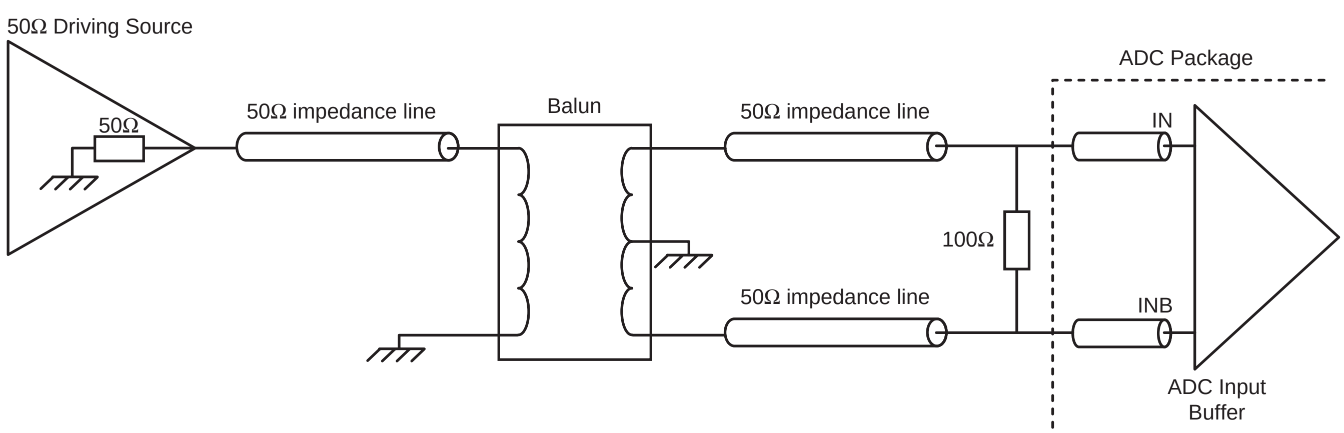


Figure 16. Configuration with Differential 100Ω Termination Resistors and with Floating Middle Point



Clock Input Termination Techniques

In the case when the clock input of the ADC is not used in ECL levels but is centered around 0V, the configurations presented for the analog inputs (ground common mode voltage), **except the AC coupled cases**, can be transferred to the input clock.

ECL Single-ended Configuration

With a clock in ECL level, the main idea to abide by is to connect the negative clock to the common mode voltage of the positive clock input: -1.3V (ECL) through a 50Ω termination resistor (if not already implemented).

Figure 17. Configuration without Additional 50Ω Termination Resistor

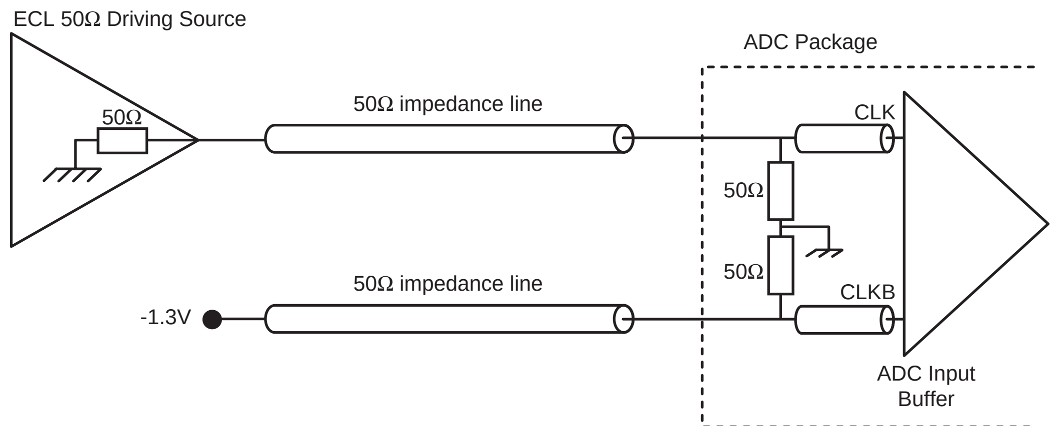
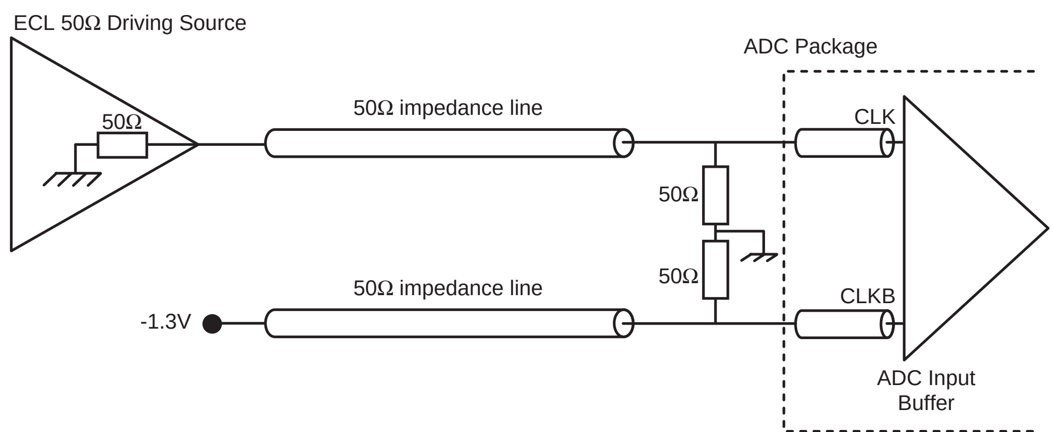


Figure 18. Configuration with 50Ω Termination Resistor



ECL Differential Configuration (ADCs Only)

When the clock is used in differential mode with ECL levels, two cases can be taken into consideration:

- the ADC is 50Ω on-package (or internally) terminated;
- the ADC needs an external termination.

Each configuration is described in what follows.

Figure 19. ADC Configuration with External Termination

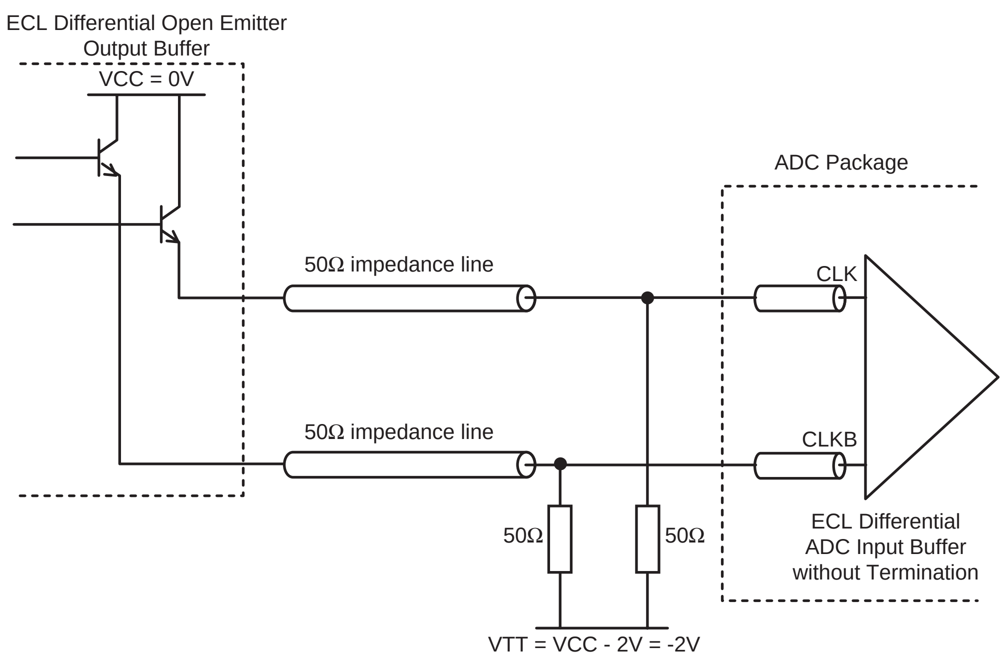
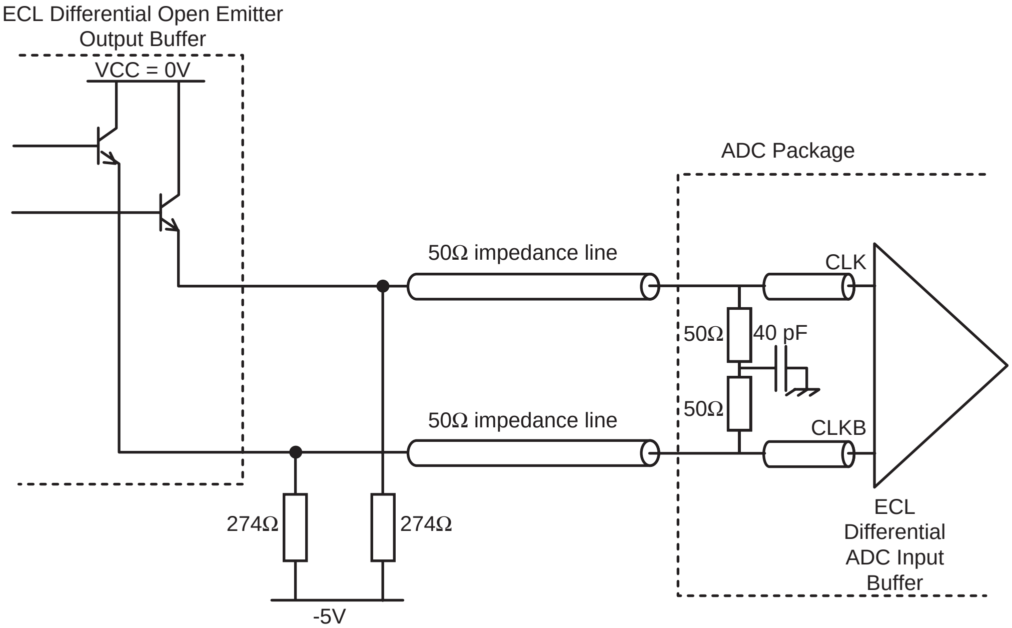


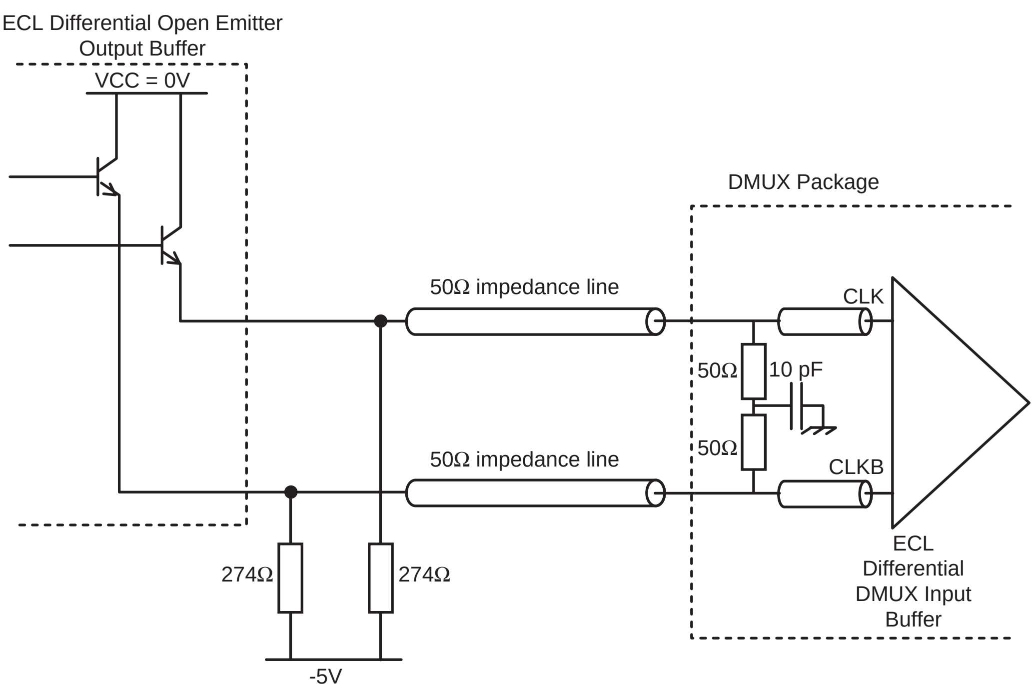
Figure 20. ADC Configuration with 50Ω On-package (or internal) Termination



Note: Since the ADC is already terminated, the standard termination scheme for the ECL driver (V_{TT} = V_{CC} - 2V with R_t = 50Ω) does not apply here. The Figure 20 is an equivalent termination scheme.

ECL Differential Configuration (DMUX Only)

Figure 21. DMUX Configuration with ECL Differential

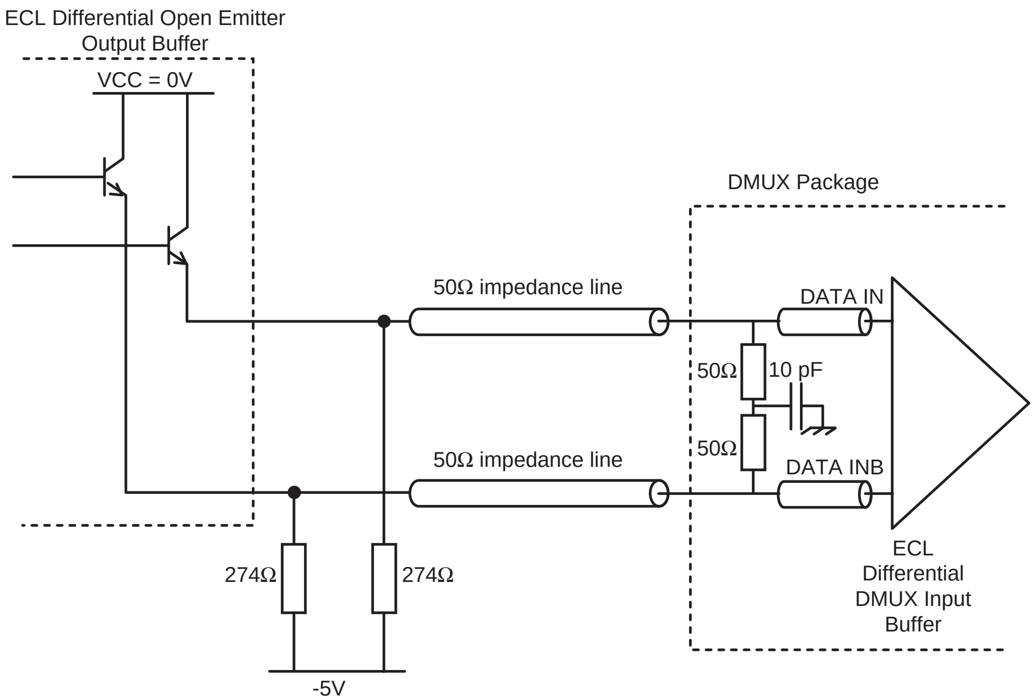


Note: Since the ADC is already terminated, the standard termination scheme for the ECL driver (V_{TT} = V_{CC} - 2V with R_t = 50Ω) does not apply here. The Figure 21 is an equivalent termination scheme.

Digital Input Termination Techniques for the DMUX

The termination technique recommended for the DMUX Data inputs is similar to the one used for the DMUX input clock, since all the DMUX input buffers have been designed according to the same architecture.

Figure 22. Digital Input Configuration



Note: Since the ADC is already terminated, the standard termination scheme for the ECL driver (V_{TT} = V_{CC} - 2V with R_t = 50Ω) does not apply here. The Figure 22 is an equivalent termination scheme.

Data Output Termination Techniques

Open Loaded Termination (ADCs)

Figure 23. TS8388Bx and TS8308500 Open Loaded Output Termination

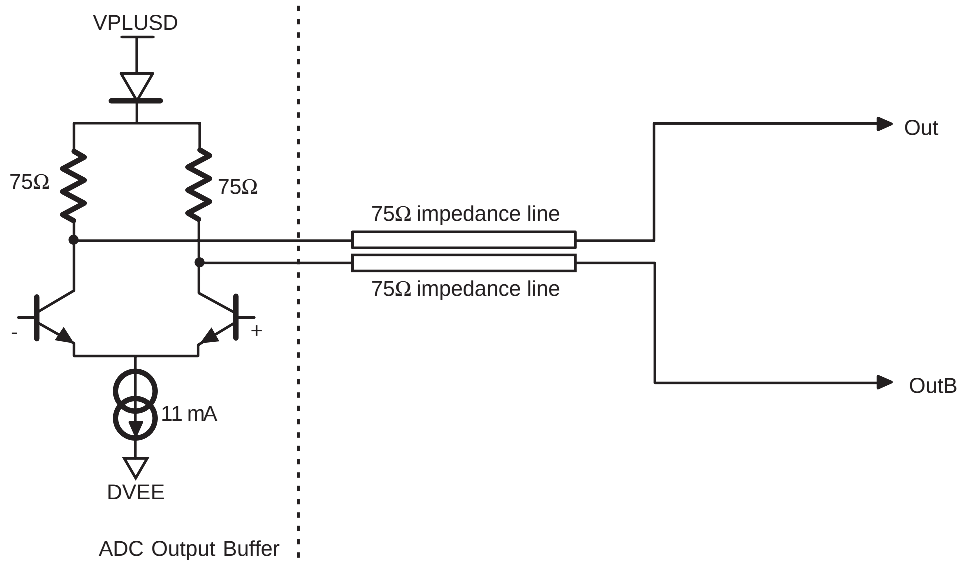
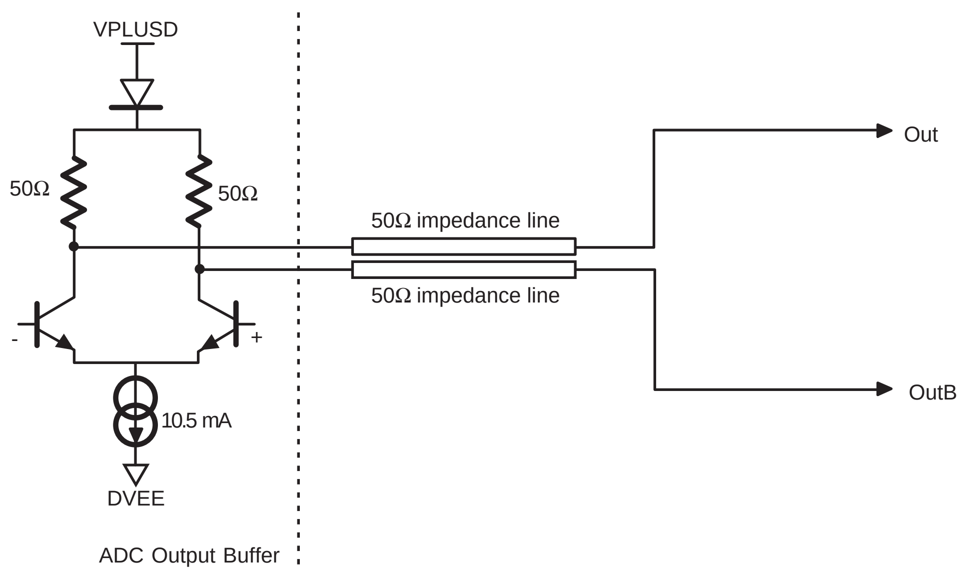


Figure 24. TS83102G0 Open Loaded Output Termination

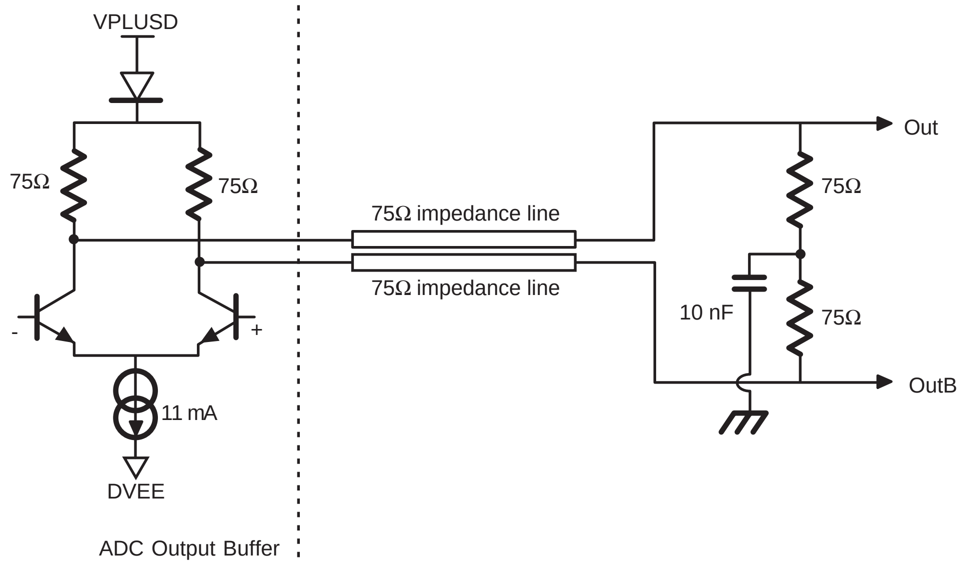


In the previous configurations, the output level is determined by V_{PLUSD}: ECL/LVDS modes are available (refer to the product data sheets for more information).

75Ω Termination

For TS8388Bx and TS8308500 Only

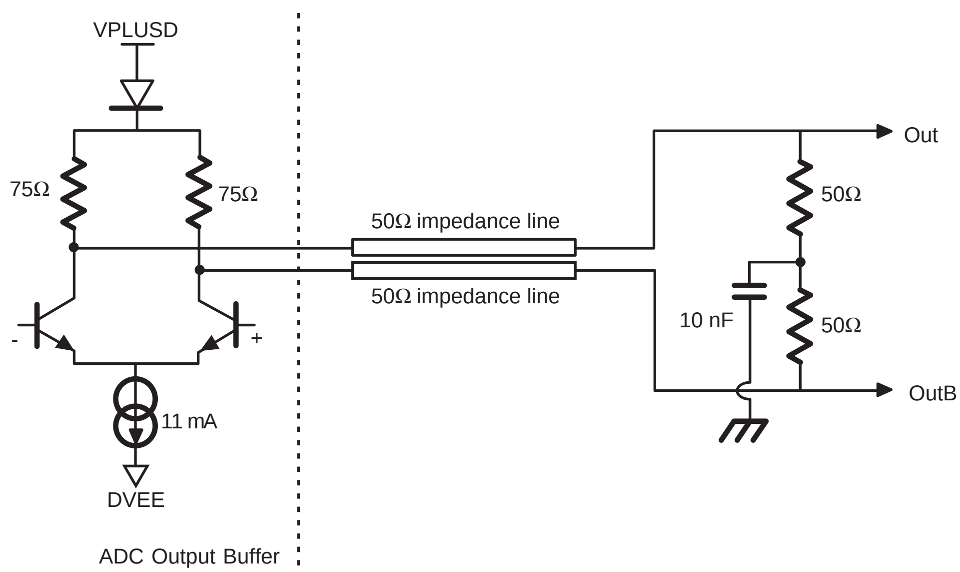
Figure 25. TS8388Bx and TS8308500 75Ω Termination



50Ω Termination

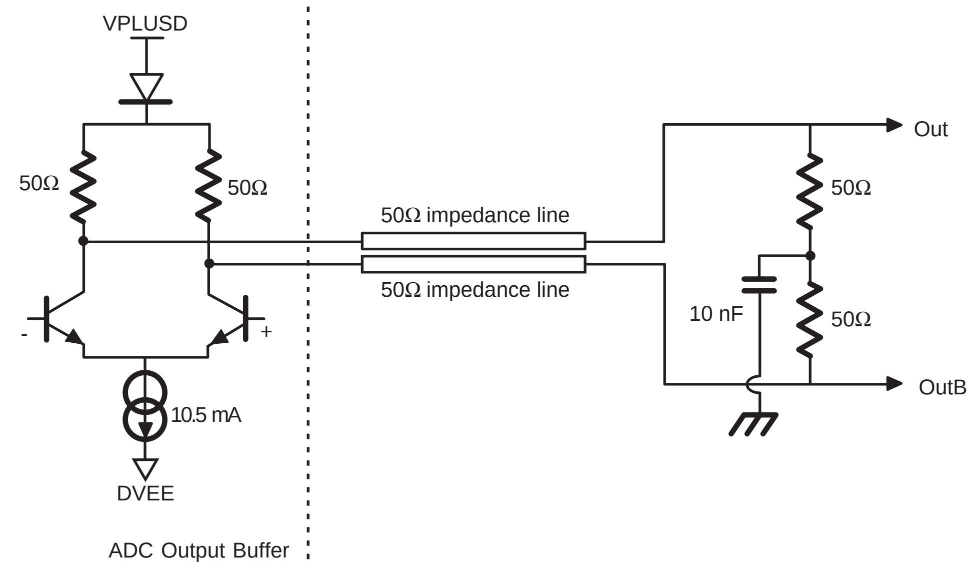
For the TS8388BX and TS8308500 ADCs

Figure 26. TS8388Bx and TS8308500 50Ω Termination



For the TS83102G0 ADC

Figure 27. TS83102G0 50Ω Termination



(VTT + R) Termination (DMUX Only)

In the specific case of the Atmel DMUX, the output buffers need to be terminated with a "VTT + R" termination (see the different schematics) because the DMUX output buffers are in open-emitter configuration.

There are three types of output signals for the DMUX: Data Ready, Digital Output Data and Reference Voltage. All of them have the same behavior against V_{PLUSD} and Swing Adjust, and their associated buffers are similar.

Figure 28. DMUX Differential Data Ready Output Buffer

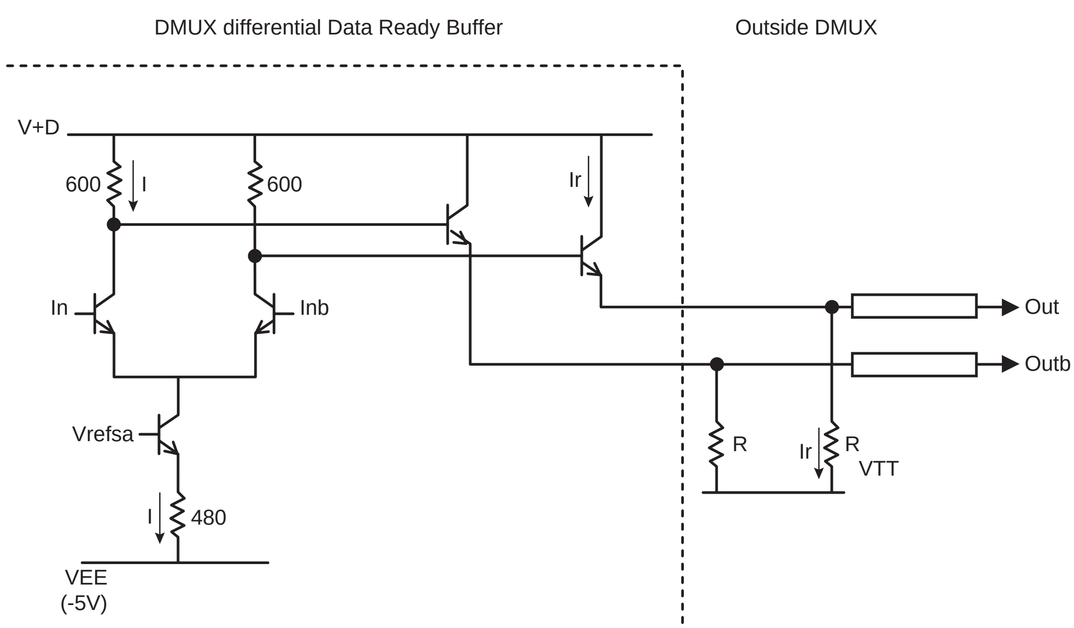


Figure 29. DMUX Digital Output Data Buffer

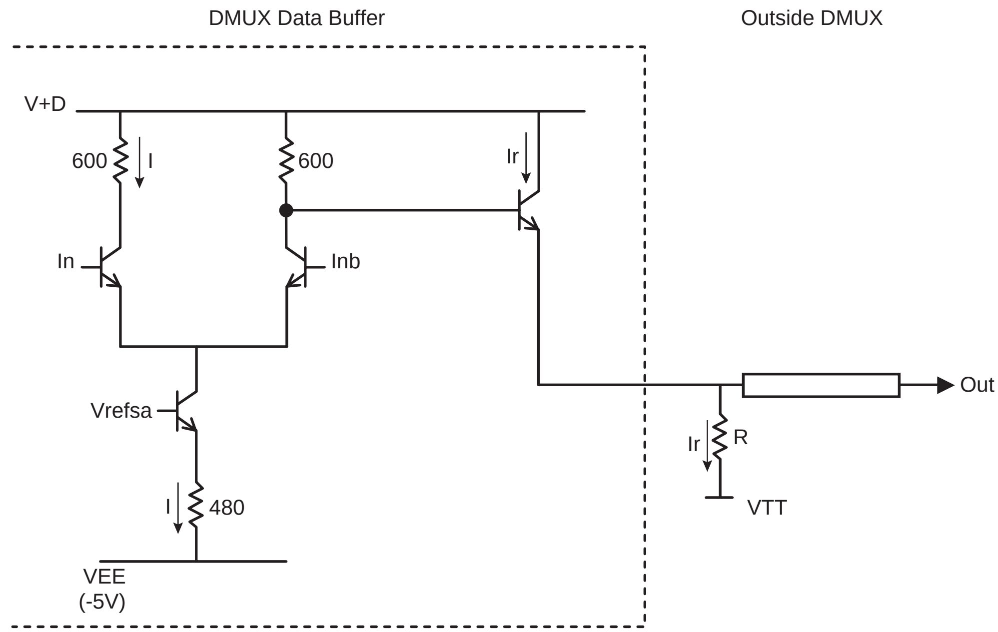
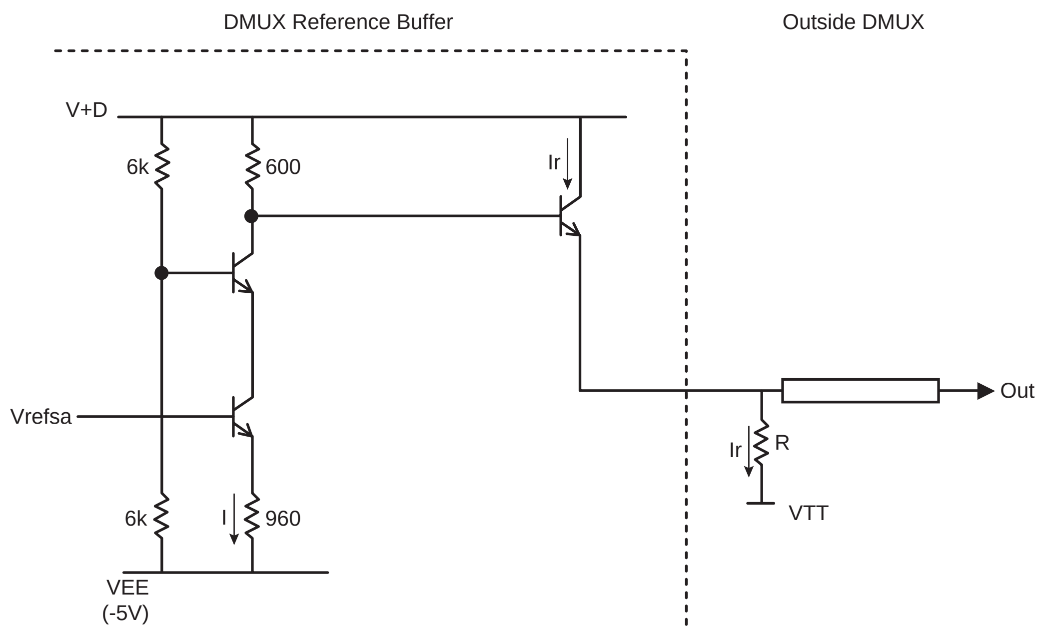


Figure 30. DMUX Reference Buffer



The only care to be taken to terminate these output buffers properly is to make sure that the output current **Ir never exceeds 36 mA**.

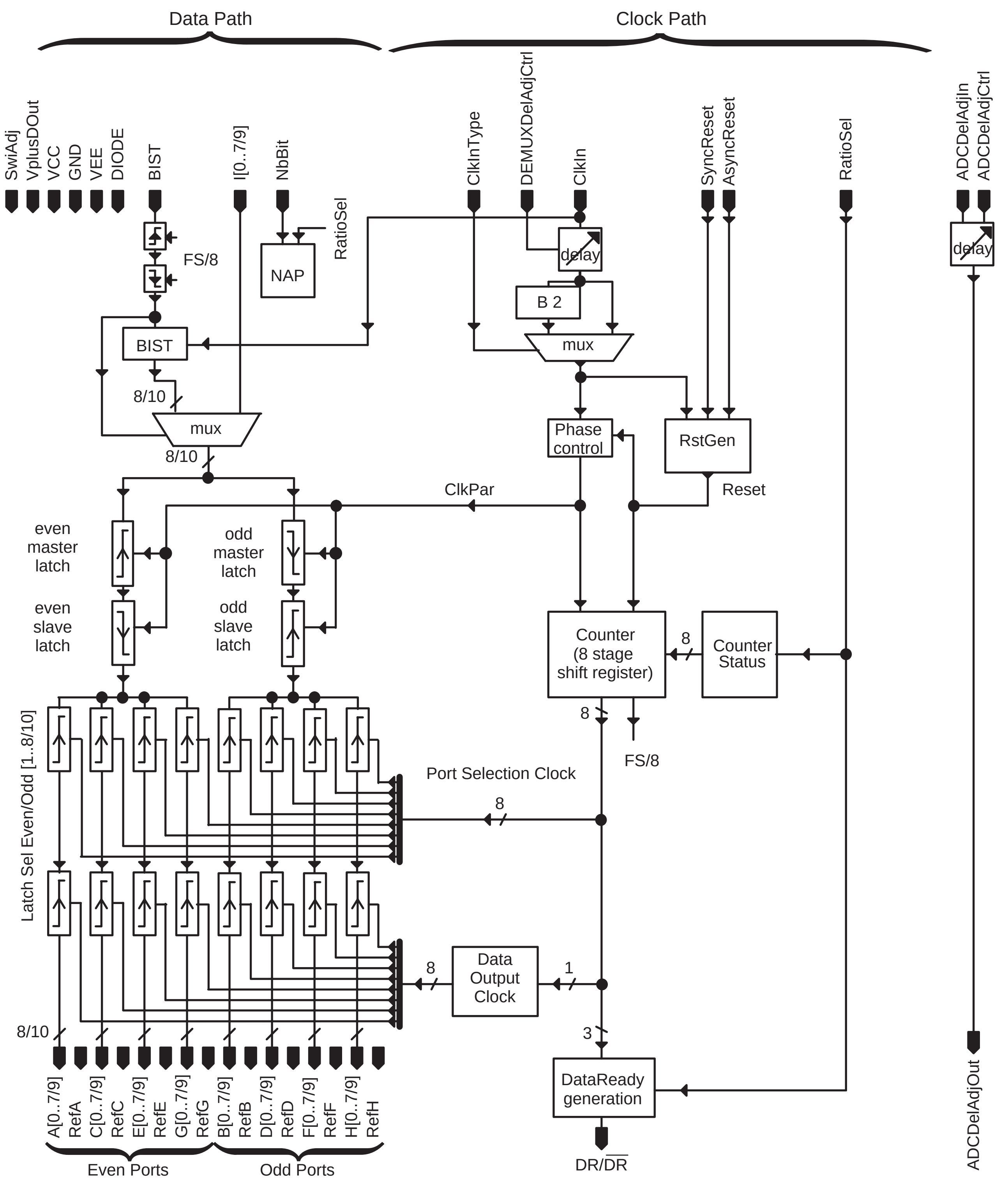
The relationship between VTT, R, Ir and Vout (output voltage level) is given here:

$$Ir = \frac{Vout - Vtt}{R}$$

Block Diagram

TS81102G0 DMUX

Figure 31. TS81102G0 DMUX Block Diagram



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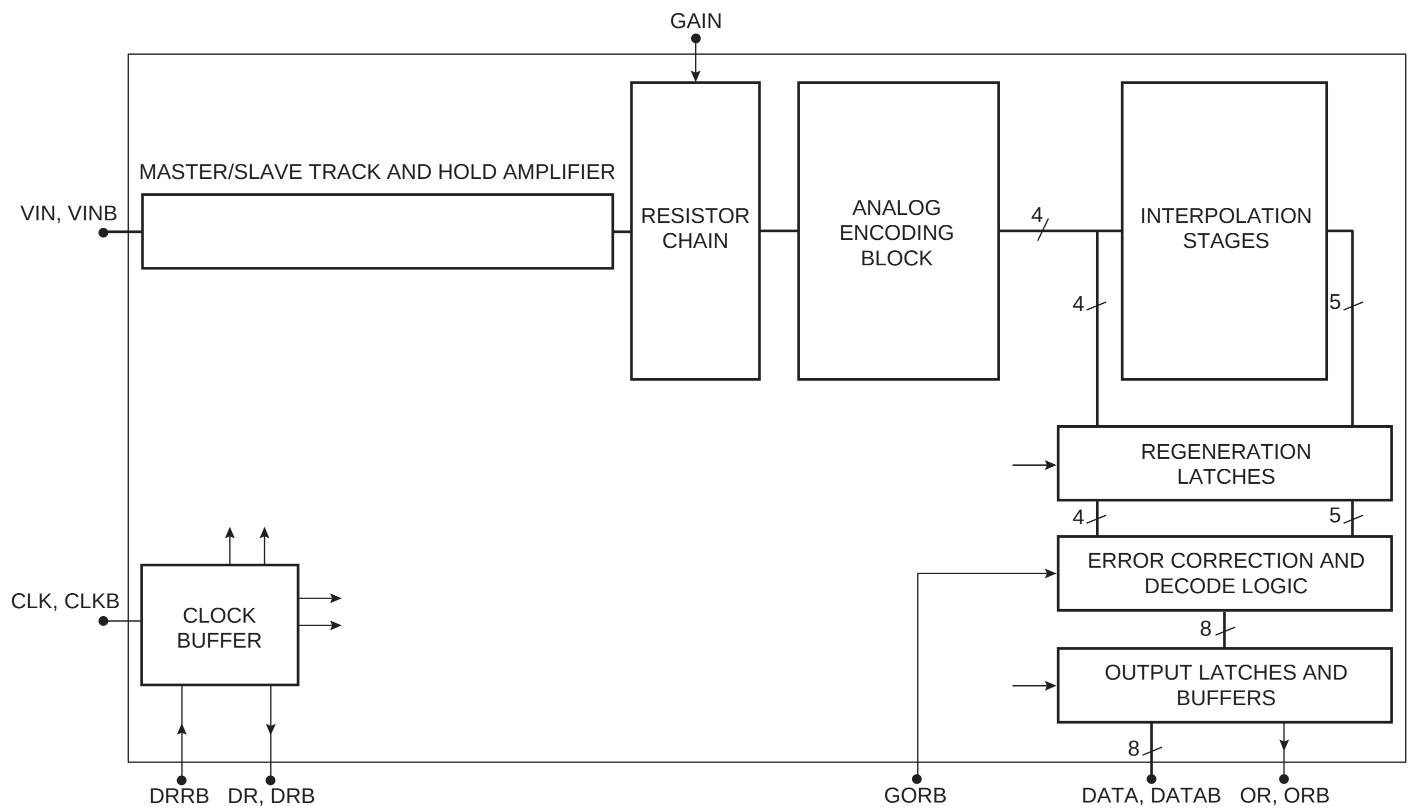
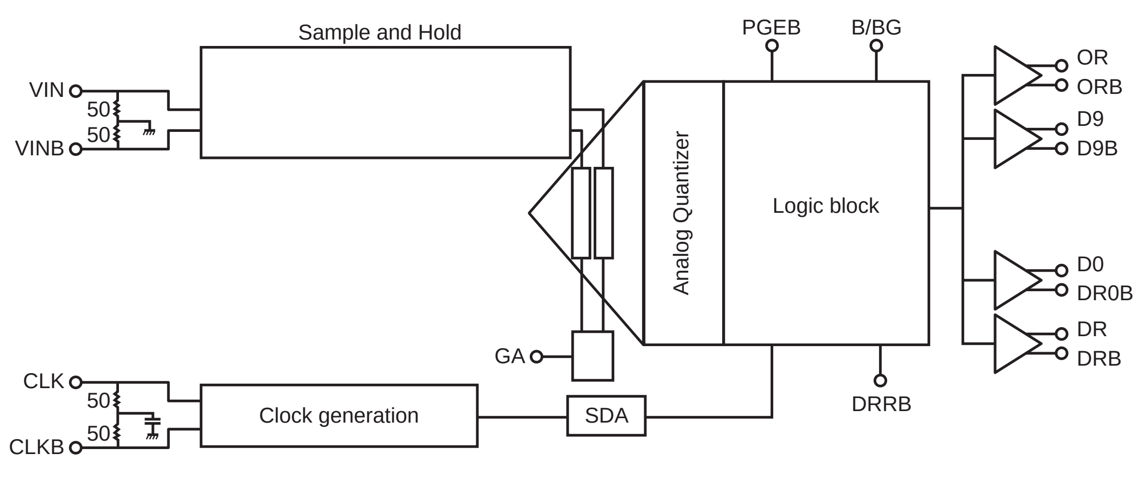
TS8388B ADC

Figure 32. TS8388B ADC Block Diagram



TS83102G0 ADC

Figure 33. TS83102G0 ADC Block Diagram

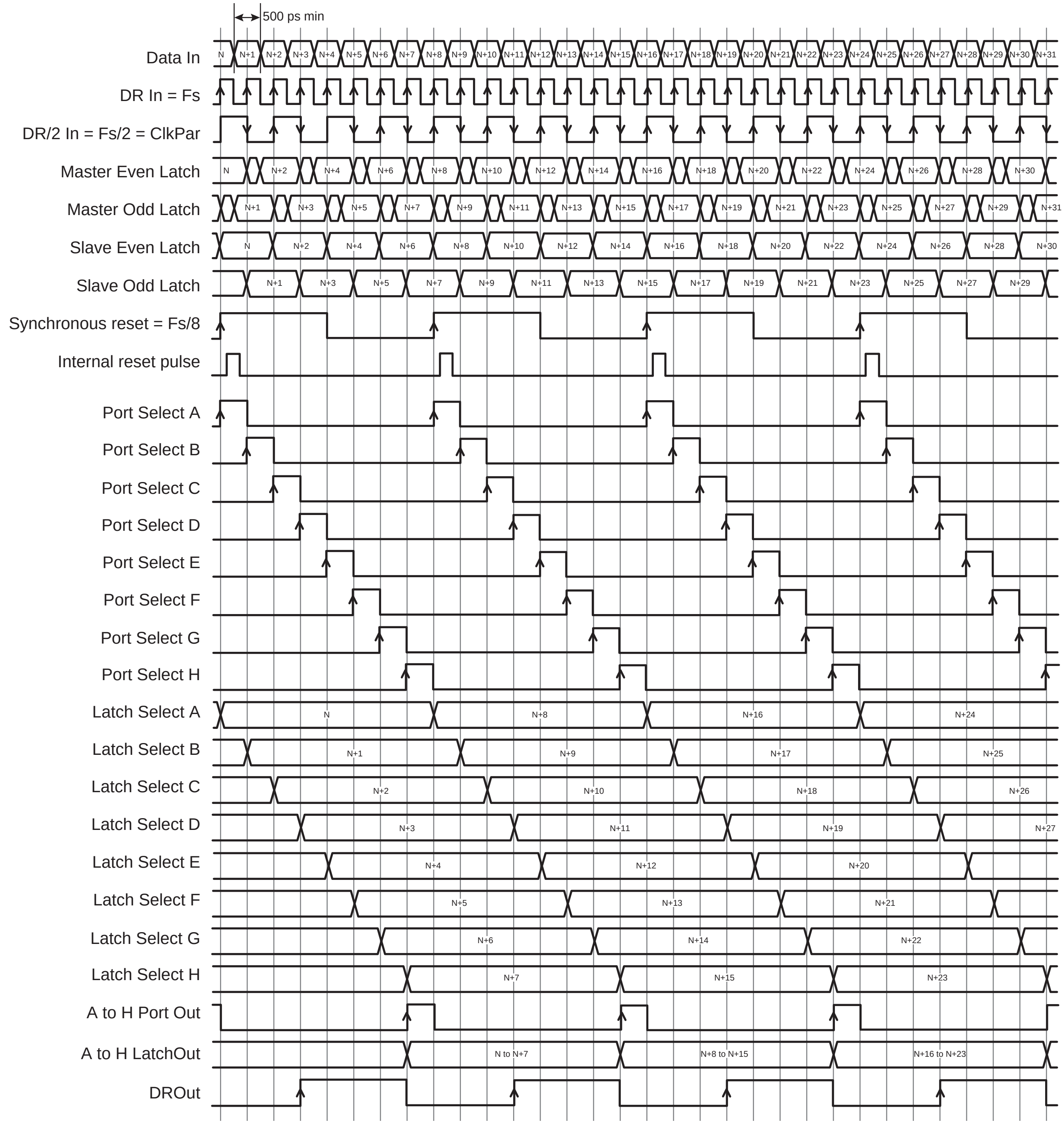


Internal Timing Diagram

DMUX Timing Diagram

This diagram corresponds to an established operation of the DMUX with Synchronous Reset.

Figure 34. DMUX Timing Diagram



ADCs Timing Diagrams

The timing diagrams for the TS8388B and TS83102G0 ADCs are similar. Care should only be taken regarding the values of the specified timings (Refer to the corresponding device data sheets for more details).

Figure 35. Data Ready Reset, Clock Held at LOW Level

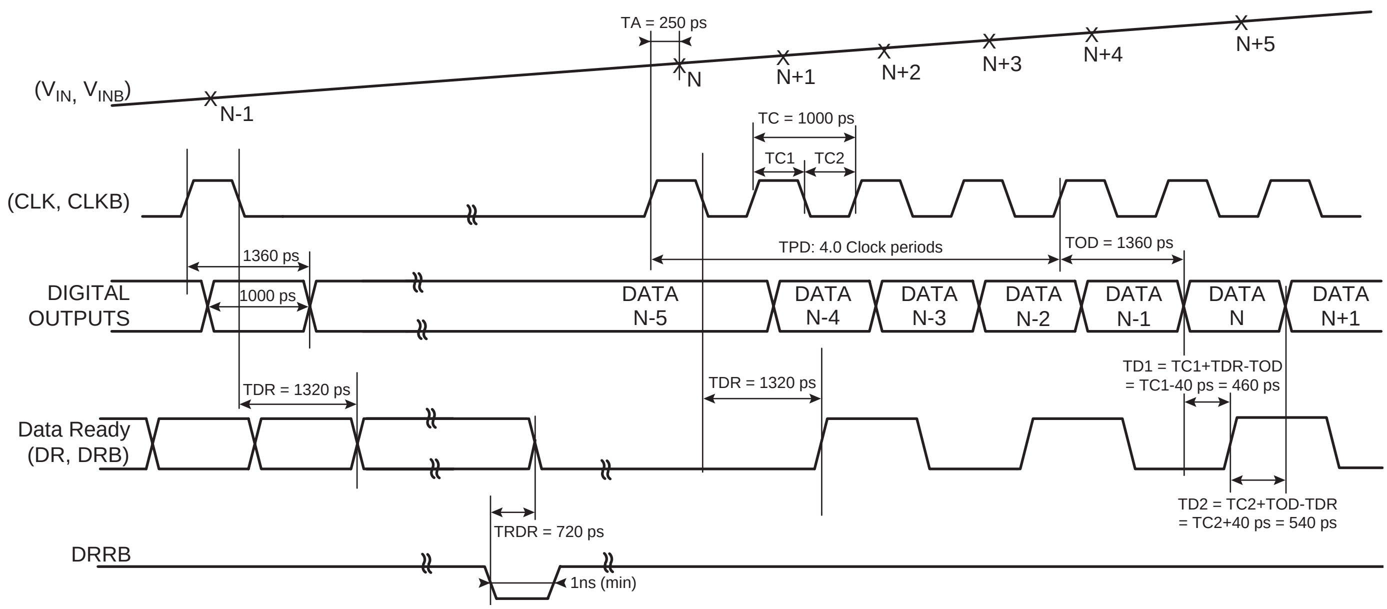
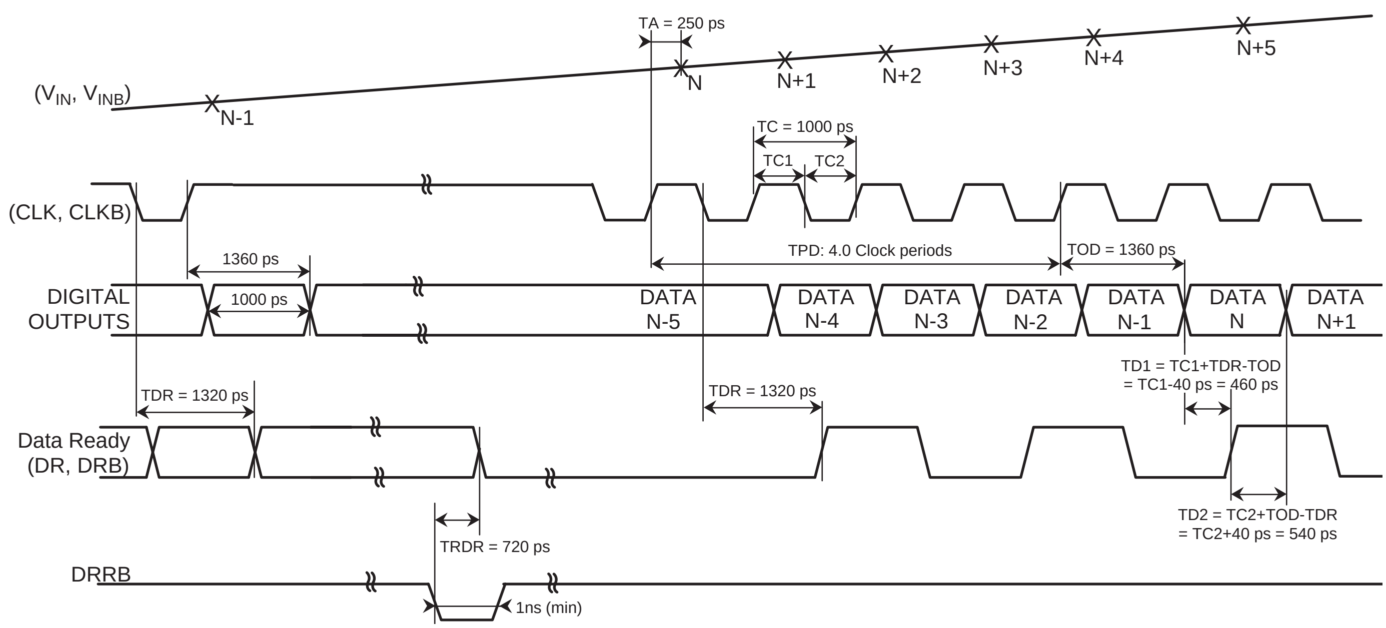
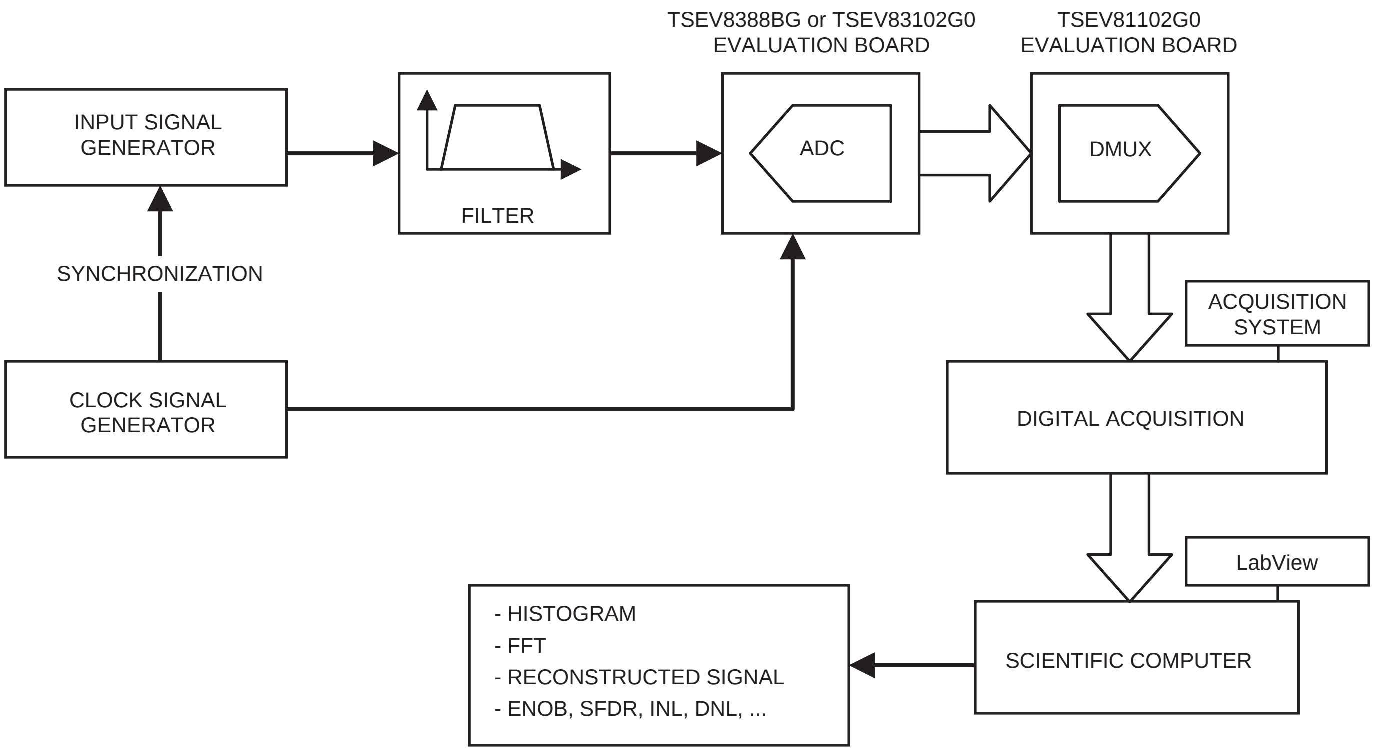


Figure 36. Data Ready Reset, Clock Held at HIGH Level



ADC and DMUX Testbench

Figure 37. Example of ADC and DMUX Testbench



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