Application Note

1. Introduction

This application note aims at providing you some recommendations to implement the AT84AS008 10-bit 2.2 Gsps ADC in your system.

It first presents the ADC input/output interfaces and then provides some recommendations as regards the device settings and board layout to obtain the best performance of the device.

This document applies to the:

- AT84AS008 10-bit 2.2 Gsps ADC
- AT84CS001 10-bit 2.2 Gsps 1:2/4 DMUX

2. AT84AS008 ADC Input Terminations

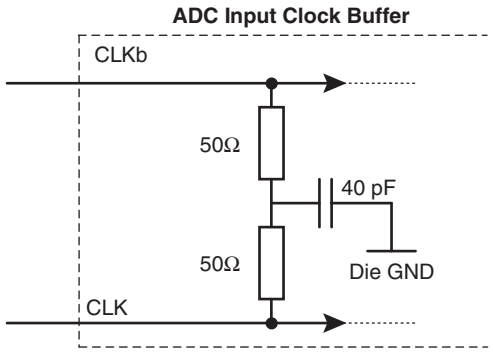
2.1 Clock Input

In the case of the AT84AS008 10-bit 2.2 Gsps ADC, it is recommended to drive the input clock *differentially*. The differential implementation is preferred to the single-ended fashion for the following reason: The differential input clock buffer is on-chip terminated by two 50Ω resistors connected to the die ground plane via a 40 pF capacitor (as described in Figure 2-1).

If the differential pair is used in a single-ended way (in which case, it would be necessary to terminate one signal of the pair *more likely CLKb* to ground via a 50Ω termination in order to keep the balance within the differential pair), then all the noise induced on the unused signal would affect the die ground directly and thus might degrade significantly the ADC performance.

However, this is a recommendation only. Providing a proper decoupling of the ADC power supplies to ground, the difference in performance between a differential and a single-ended use might not be significant.

Figure 2-1. Clock Input Differential Buffer



The clock inputs of the ADC have a 0V common mode and can accept signals with 1 Vpeak maximum and -1 Vpeak minimum.

This means that if the VIH max of the signal you would like to drive the ADC clock with is higher than 1 Vpeak or the VIL min. is lower than -1 Vpeak, then you need to *AC couple* the input signals before applying them to the ADC, this can be done by connecting 10 nF capacitors in series with the incoming signals to the ADC. If you do so, then you need also to bias the CLK and CLKb signals as follows:

- CLK or CLKb biased to ground via a 10 kΩ resistor
- CLKb or CLK respectively biased to ground via a 10 kΩ resistor and to V_{EE} via a 100 kΩ resistor

This will ensure that if no signal is applied to the differential pair, the latter one will not be floating but tied to a low level.

Figure 2-2. Recommended Clock Input AC Coupling Scheme

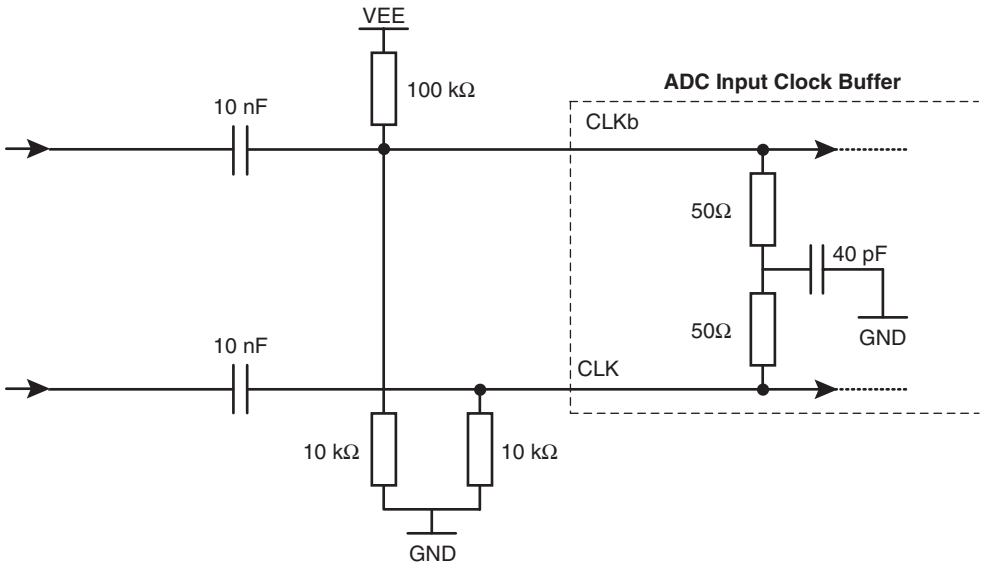
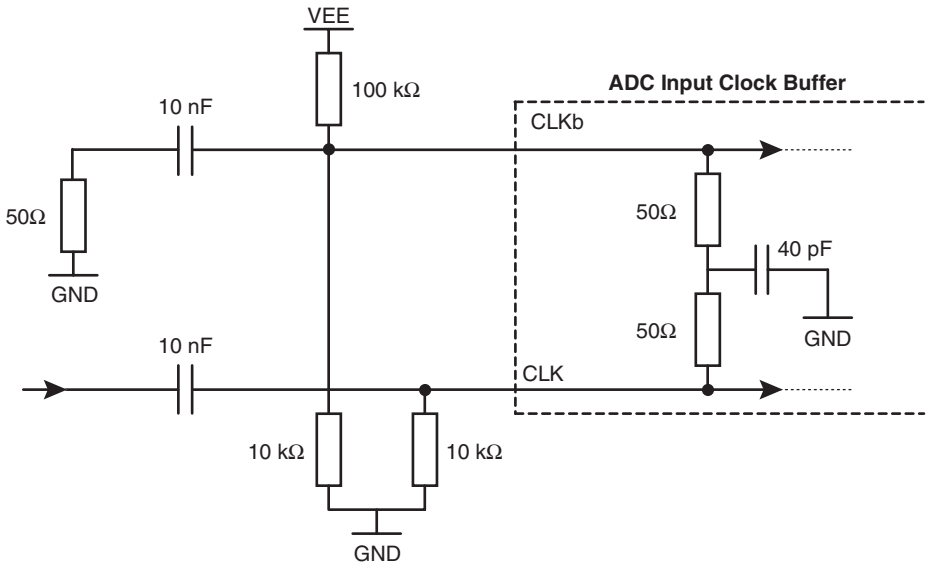


Figure 2-3. Single-ended Scheme (Allowed but not Recommended)



In the case of an application requiring a fixed clock frequency, it is recommended to filter the clock signal for improved jitter performance. The benefits of filtering the clock signal can be quantified to a 1 or 2 dB improvement in the SNR figure and thus in an increase of about 0.1 to 0.2 bit in the ENOB figure.

The filtering can be done using a narrow-band filter but because beyond the stop-band frequency the noise is not filtered out, it might be necessary to have a low pass filter after the narrow band filter.

Table 2-1. References for Filters (for Information Only)

Filter Type	Reference	Frequency
Band pass	4DF12-500/X2-MP (Lorch)	500 MHz
Band pass	4DF12-1000/X2-MP (Lorch)	1000 MHz
Band pass	6DF12-1400/X2-MP (Lorch)	1400 MHz
Low pass	4LP7-550X-MP (Lorch)	550 MHz
Low pass	5LP7-1000X-MP (Lorch)	1000 MHz
Low pass	6LP7-1800X-MP (Lorch)	1800 MHz

2.2 Analog Input

Although it is recommended to drive the input clock differentially with the AT84AS008 10-bit 2.2 Gsps ADC, the analog input can be indifferently driven single-ended or differential.

On the contrary to the differential input clock buffer, the analog input buffer is not on-chip terminated by two 50Ω resistors connected to the die ground plane but it is terminated inside the cavity, in which case the 50Ω resistors are connected to the package ground plane (as described in Figure 2-4).

If the differential pair is used in a single-ended way (in which case, it would be necessary to terminate one signal of the pair *more likely VINb* to ground via a 50Ω termination in order to keep the balance within the differential pair), then all the noise induced on the unused signal would not affect the die ground directly.

Figure 2-4. AT84AS008 Analog Input Buffer Schematic

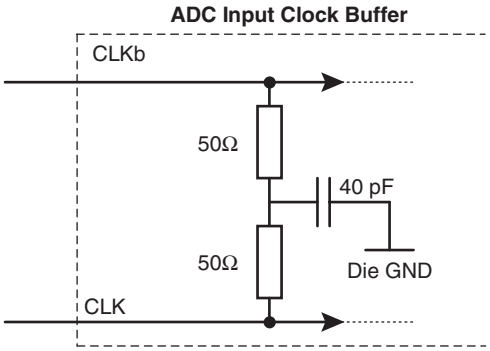
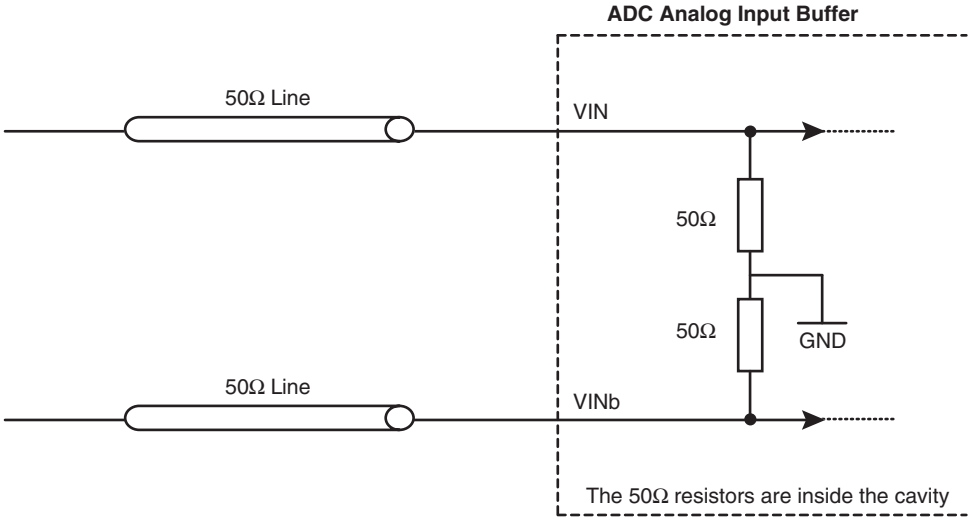
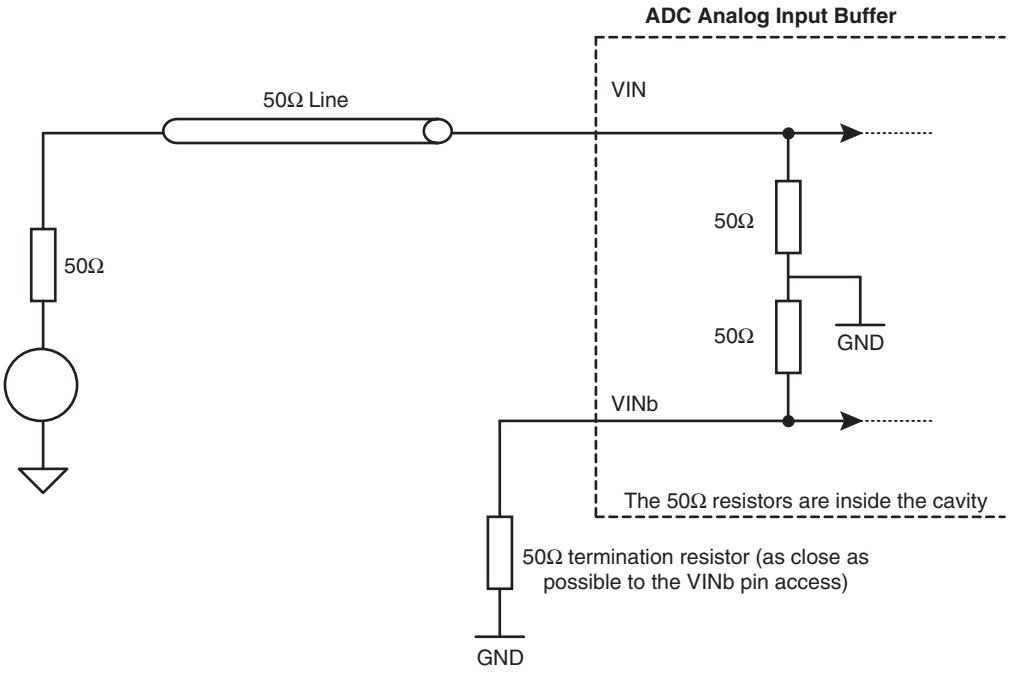


Figure 2-5. AT84AS008 Analog Input Termination Scheme (Differential)



"For more information concerning the conversion from a single-ended signal to a differential signal using transformers, please refer to the “Single to Differential Conversion in High Frequency Applications” appli-cation note ref. 5359."

Figure 2-6. AT84AS008 Analog Input Termination Scheme

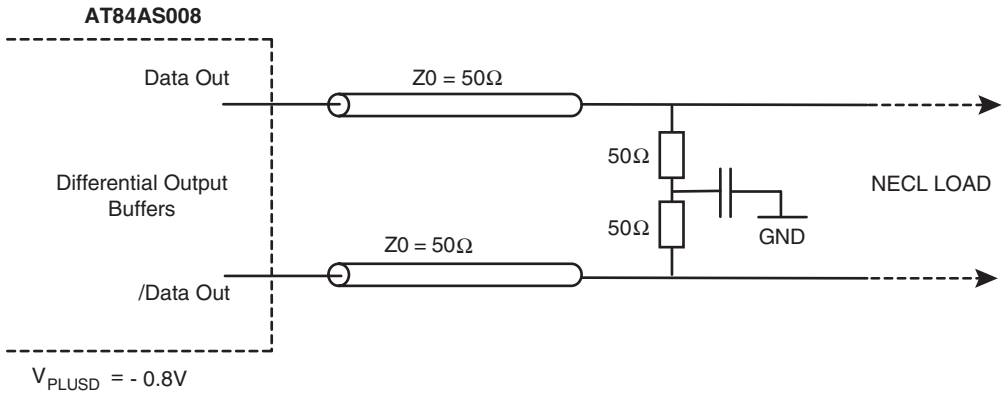


3. AT84AS008 ADC Output Terminations

The output data and clock of the AT84AS008 ADC can be set either in NECL or in LVDS depending on the V_{PLUSD} value.

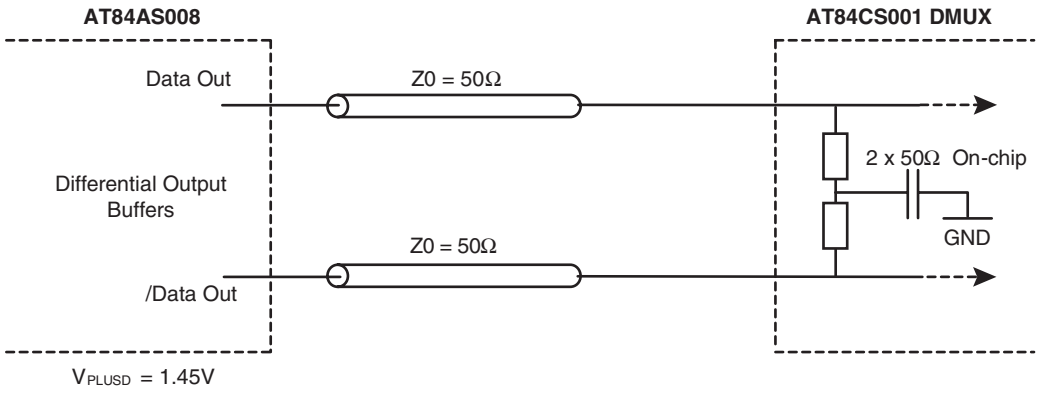
In NECL output mode, the ADC V_{PLUSD} power supply has to be set to -0.8V by connecting V_{PLUSD} plane to the ADC ground plane via a 5.2Ω resistor. The ADC outputs have then to be terminated with 50Ω resistors as shown in Figure 3-1.

Figure 3-1. AT84AS008 Output Data and Clock Interface in NECL



When connected to the AT84CS001 DMUX from e2v, the ADC has to be set in LVDS (V_{PLUSD} = 1.45V). The ADC outputs need to be 100Ω terminated and since the AT84CS001 DMUX input buffers are already on-chip 2 x 50Ω terminated, the ADC can be connected directly to the DMUX as shown in Figure 3-2.

Figure 3-2. AT84AS008 Output Data and Clock Interface to AT84CS001 DMUX in LVDS



4. AT84AS008 ADC Settings

4.1 DRRB Reset Signals

The DRRB signal frequency should be 200 MHz maximum and the reset pulse should be 1 ns minimum. DRRB is active low.

The DRRB reset is not necessary to start the ADC but it is required when several ADCs have to be synchronized to one another. Indeed, it ensures that the two ADC output clocks are in phase after reset at the output of the ADC, providing the reset is performed while the input clock is held either low or high. If the ADC is used with the AT84CS001 DMUX device, it is possible to perform the resets on both devices using the same differential signal with the true signal used for the ASYNCRST of the DMUX and the false signal used for DRRB.

4.2 B/GB

It is possible to choose between a binary or a gray output coding. For high-speed operation (rates above 2 Gsps), it is recommended to use the ADC in Gray mode as only one bit can transition at a time, thus reducing the switching noise at each bit transition (less noise when only one bit transition than several at the same time).

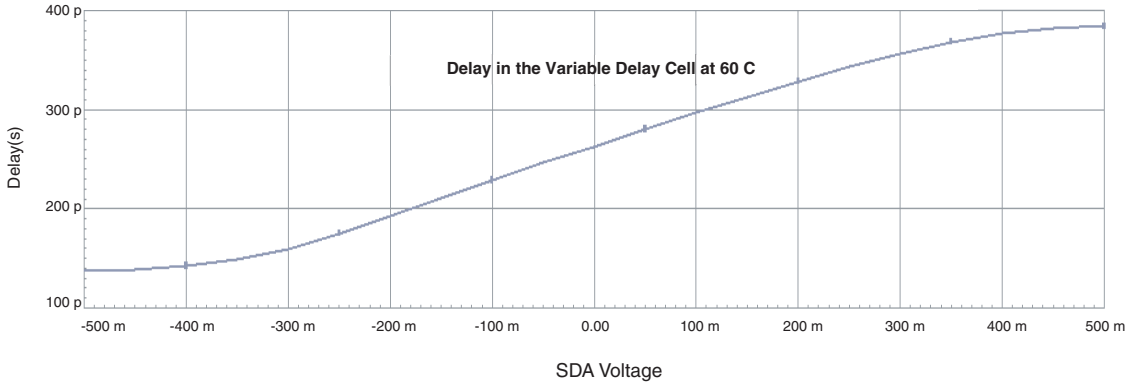
4.3 SDA

The sampling delay adjust function (SDA pin) allows to fine-tune the sampling ADC aperture delay TAD around its nominal value (160 ps). This functionality is enabled thanks to the SDAEN signal, which is active when tied to V_{EE} and inactive when tied to GND or left floating.

If SDAEN is connected to ground or left floating (SDA function not active), then the ADC aperture delay is the nominal one as specified in the datasheet. This feature is particularly interesting for interleaving ADCs to increase sampling rate. The variation of the delay around its nominal value as a function of the SDA voltage is shown in Figure 4-1.

The typical tuning range is ± 120 ps for applied control voltage varying between -0.5V to 0.5V on SDA pin.

Figure 4-1. ADC Aperture Delay vs. SDA

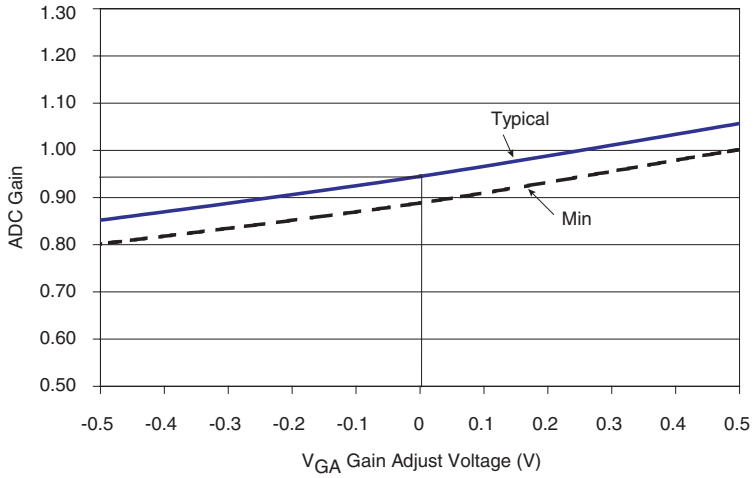


The variation of the delay in function of the temperature is negligible. If this function is not used, SDAEN can be left floating as well as the SDA pin.

4.4 GA

The ADC gain is adjustable by the means of the pin R9 of the CBGA package. If the GA pin is left floating, then the gain of the ADC will be the nominal gain as specified in the datasheet. However, we recommend you to connect the GA pin to ground if the function is not used. The gain adjust transfer function is given in Figure 4-2.

Figure 4-2. ADC Gain vs. GA Voltage



4.5 PGEB

A test function is provided with the ADC (pattern generator function , pin A9) to allow the user to check the ADC output signals. When set in pattern generator function (PGEB connected to V_{EE}), then the ADC outputs series of *ones* and *zeros* as follows:

Cycle N : D9 = 1, D8 = 0, D7 = 1, D6 = 0, D5 = 1, D4 = 0, D3 = 1, D2 = 0, D1 = 1, D0 = 0

Cycle N+1 : D9 = 0, D8 = 1, D7 = 0, D6 = 1, D5 = 0, D4 = 1, D3 = 0, D2 = 1, D1 = 0, D0 = 1

Cycle N+2 : D9 = 1, D8 = 0, D7 = 1, D6 = 0, D5 = 1, D4 = 0, D3 = 1, D2 = 0, D1 = 1, D0 = 0

The output clock transitions from low to high level (from zero to one) when odd bits are high *1* (even bits are low *0*) and from high to low (from one to zero) when odd bits are low *0* (even bits are high *1*)

If you do not intend to use this function, the PGEB signal should be either left floating or connected to ground.

4.6 Diode

If you provide a 1 mA current (using a multimeter in current source mode) to the A10 pin of the ADC, the voltage across pin A10 and the closest ground pin of the ADC (for example pin B10) will give you the approximate die junction temperature with respects to the diode characteristic provided in the device datasheet (ref. 5404). If not used the diode pin can either be left floating or connected to ground.

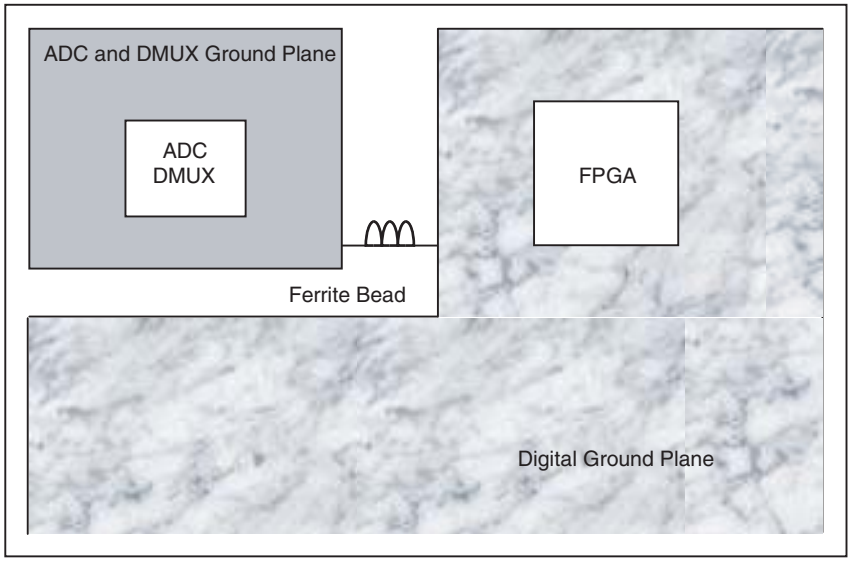
5. Grounding and Power Supplies

5.1 Common Ground Plane

It is recommended to use the same common ground plane for both the ADC and the DMUX but to separate this common plane from the digital ground plane used for the digital part of the system (FPGA for example). These two ground planes will have to be reunited by one point (via a ferrite bead see Figure 5-1).

Note: The analog planes (ground or power supply) should be as less as possible to prevent the planes to suffer from the surrounding digital planes perturbations.

Figure 5-1. Schematic View of the System Board Ground Plane (Example)



5.2 Power Supply Planes

The ADC (AT84AS008) requires three power supplies:

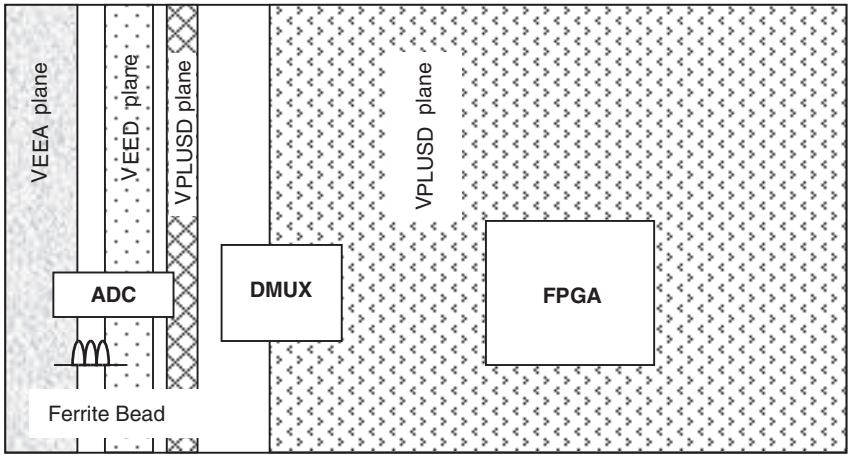
- V_{EE} = -5V analog and V_{EED} = -5V digital
- V_{CC} = 5V
- V_{PLUSD} = 1.45V

The DMUX (AT84CS001) requires two power supplies:

- V_{CC} = 3.3V
- V_{PLUSD} = 2.5V

Five different planes are required for the ADC and the DMUX. It is recommended to use the same layer for both V_{EE} and V_{EED} power supplies but using separate planes which can be reunited by a ferrite bead as shown in Figure 5-2 on page 9.

Figure 5-2. Schematic View of the ADC -5V Planes (Example)



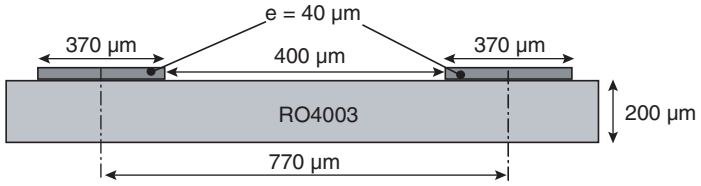
For more information concerning the power supplies decoupling and bypassing, please refer to the device datasheets (ref. 5404 and 0809 for the AT84AS008 and AT84CS001 devices respectively).

5.3 Board Layout Recommendations

It is necessary to ensure that all the lines at the input and output of the ADC are matched to within 2 mm. As all data lines are differential, it is also necessary that each line of a differential pair is matched in length within 1 mm.

Figure 5-3 gives the layout rule used on RO4003 for differential signals.

Figure 5-3. 50Ω Matched Line on R04003 Layout (Differential Signal)



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