Application Note

1. Introduction

This application note aims at providing you some recommendations to implement the AT84AS001 12-bit 500 Msps ADC in your system.

It first presents the ADC input/output interfaces and then provides some recommendations as regards the device settings and board layout to obtain the best performance of the device.

This document applies to the:

- AT84AS001 12-bit 500 Msps ADC

2. AT84AS001 ADC Input Terminations

2.1 Clock Input

In the case of the AT84AS001 12-bit 500 Msps ADC, the input clock can be indifferently driven differentially or single-ended. In all cases however, the input clock needs to be AC coupled as the common mode of the clock differential pair is $V_{CCD}/2$.

The clock differential buffer is 2 × 50Ω terminated to $V_{CCD}/2$ and this is why it is necessary to terminate the unused clock signal via both a capacitor and a 50Ω resistor to ground in single-ended mode, as described in Table 2-2 on page 1.

Figure 2-1. Clock Input AC Coupled Differential Scheme

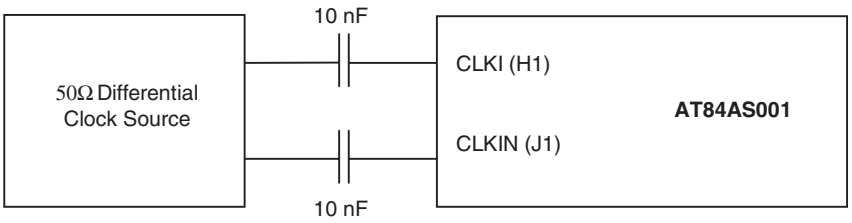
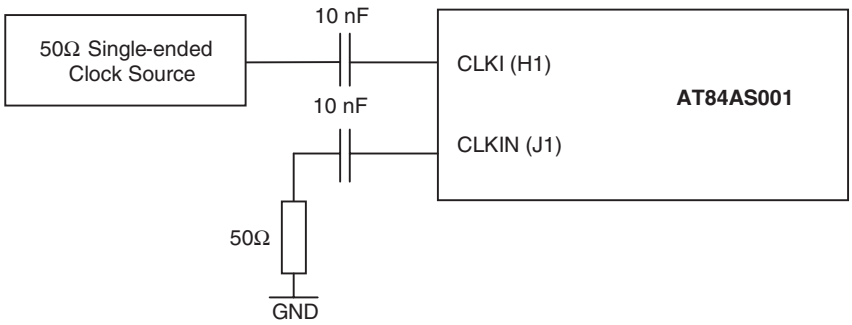


Figure 2-2. Clock Input AC Coupled Single-ended Scheme



Visit our website: www.e2v.com
for the latest version of the datasheet

The AT84AS001 ADC is very sensitive to the clock jitter performance. It is recommended to use a very low phase noise clock source with at least –145 dBc/Hz at 10 MHz from carrier (the most important parameter in the clock source is the noise floor, that is the noise characteristic at 10 MHz and more from the carrier).

Table 2-1. References for Clock Sources (for Information Only)

Clock Source Type	Reference	Output Frequency	Phase Noise L(f)
500 MHz-SC Sprinter Crystal Oscillator	500-14512 (Wenzel Associates, Inc.)	500 MHz	–150 dBc/Hz at 20 KHz from carrier
Low jitter clock generator based on PLL	AD9540 (Analog Devices)	655 MHz	–146 dBc/Hz at > 1 MHz from carrier
Programmable LVDS bus clock synthesizer	SY89532L/SY89533L (MICREL)	500 MHz max	

In the case of an application requiring a fixed clock frequency, it is recommended to filter the clock signal for improved jitter performance. The benefits of filtering the clock signal can be quantified to a 1 or 2 dB improvement in the Signal-to-Noise Ratio (SNR) figure and thus in an increase of about 0.1 to 0.2 bit in the ENOB figure.

The filtering can be done using a narrow-band filter but because beyond the stop-band frequency the noise is not filtered out, it may be necessary to have a low pass filter after the narrow band filter.

Table 2-2. References for Filters (for Information Only)

Filter Type	Reference	Frequency
Band pass	4DF12-500/X2-MP (Lorch Microwave)	500 MHz
Band pass	9BP8-500/30-S (Lorch Microwave)	500 MHz
Low pass	4LP7-550X-MP (Lorch Microwave)	550 MHz

2.2 Analog Input

Although the input clock can be indifferently driven differentially or single-ended with the AT84AS001 12-bit 500 Msps ADC, the analog input should be driven differentially.

- It can be used in AC or DC coupled mode
- In DC coupled mode, the input common mode can be accessed via the VSCH signal
- In AC coupled mode, the VSCH signal has to be left open

Figure 2-3. AT84AS001 Analog Input Buffer Schematic

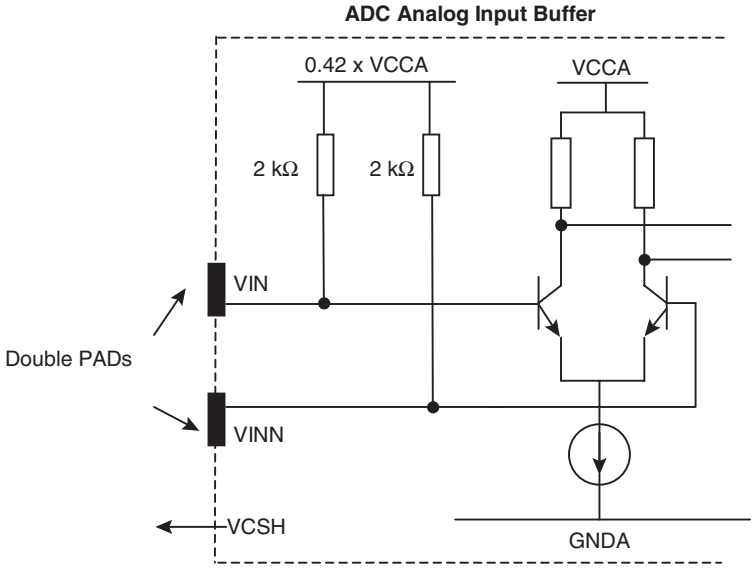


Figure 2-4. AT84AS001 Analog Input Termination Scheme (AC Coupled)

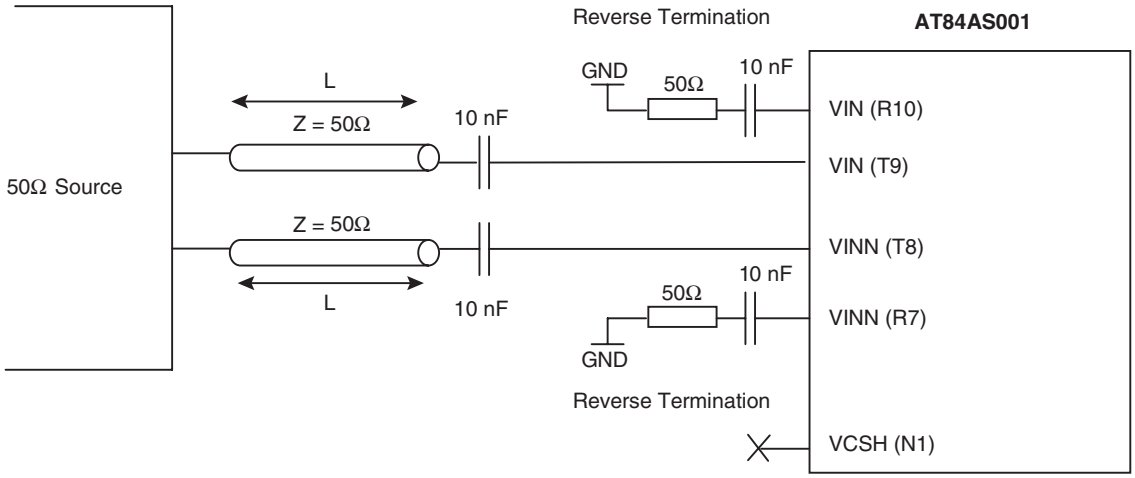
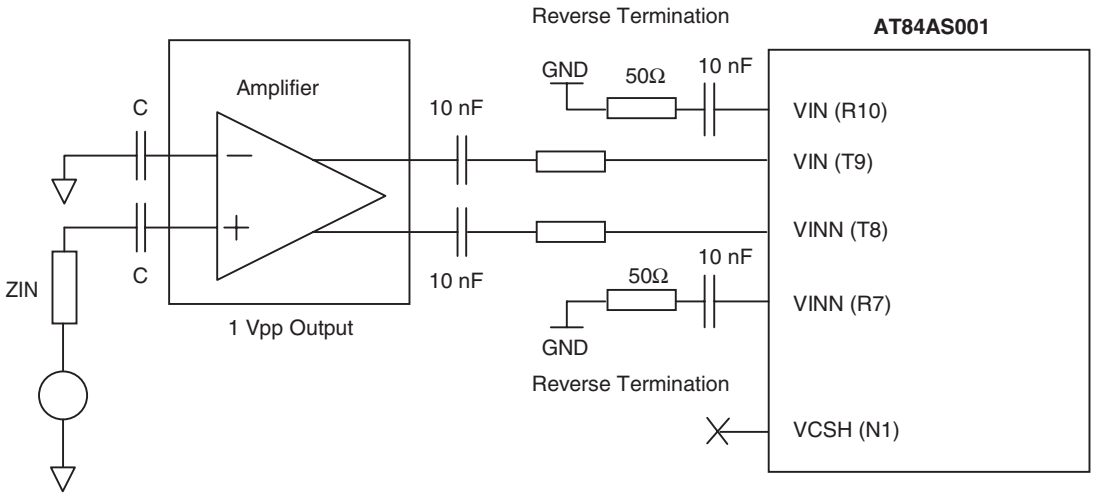


Figure 2-5. AT84AS001 Analog Input Termination Scheme (AC coupled) Using a Differential Amplifier



Note: Please refer to Table 2-3 on page 5 for suitable amplifiers.

In order to set the DC analog input, the VCSH output pin must be used as described in Figure 2-6 on page 4. The impedance Zout//R1 must be lower than 2 kΩ and equal to 50Ω to guarantee a good impedance matching and to force the right DC analog input level.

Figure 2-6. AT84AS001 Analog Input Implementation Scheme (DC Coupled, Principle of Operation)

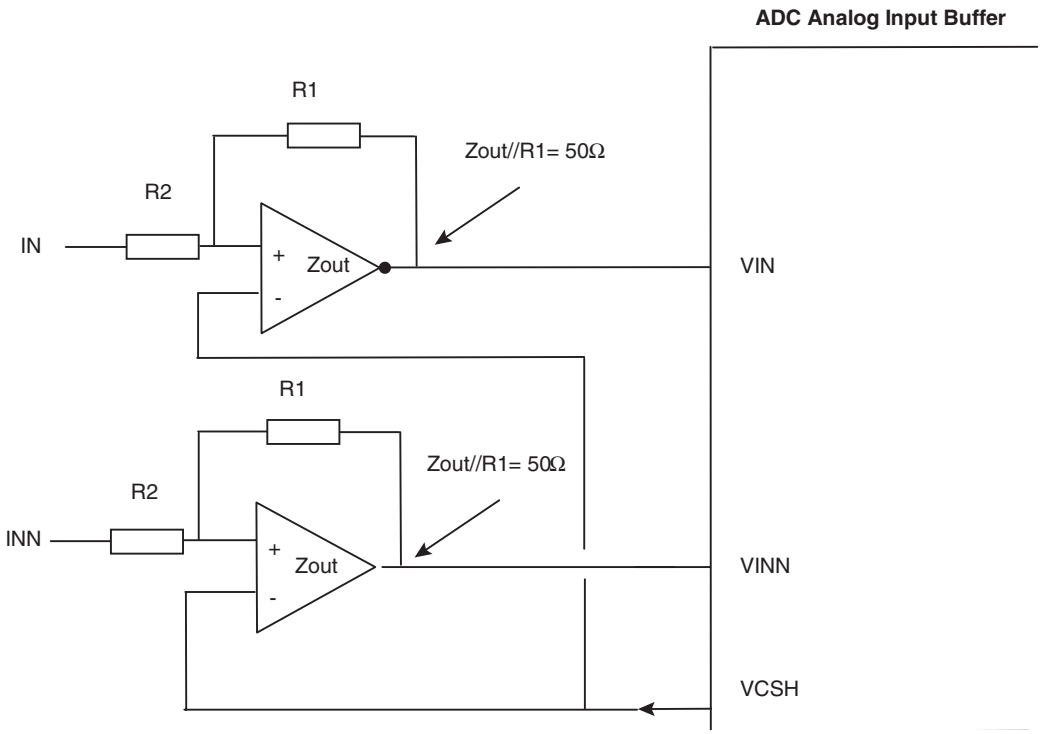


Figure 2-7. AT84AS001 Analog Input Termination Scheme (DC Coupled) Using a Differential Amplifier

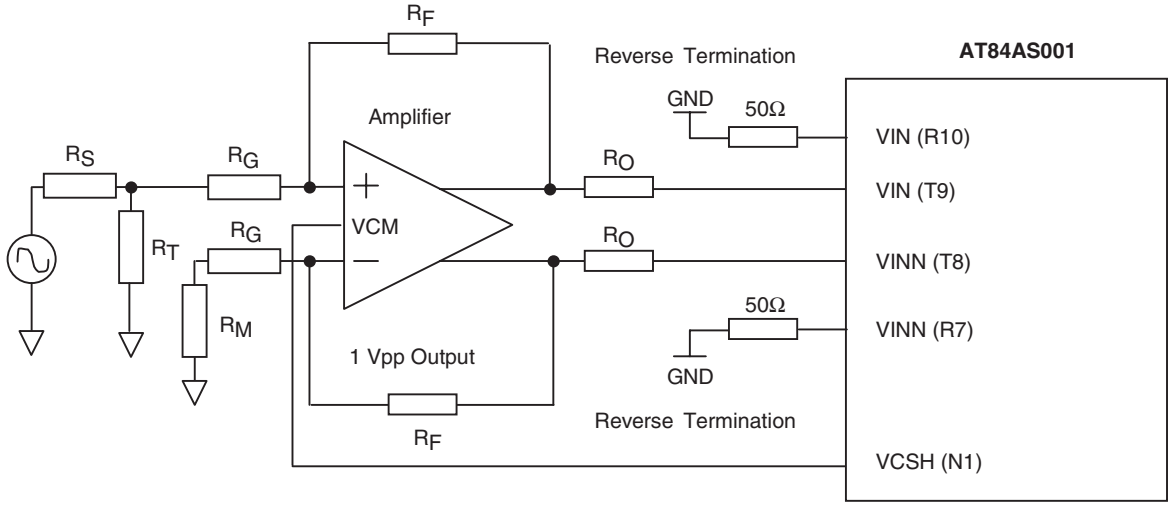


Table 2-3. References for Differential Amplifiers (for Information Only, Not Supported by e2v)

Reference	–3 dB Bandwidth	Type of Use
AD8350	1 GHz	AC coupled mode only
AD8139	410 MHz	DC coupled mode possible
LT1993	700, 800 and 900 MHz versions	AC coupled mode only
LMH6550	400 MHz	DC coupled mode possible
LMH6551	370 MHz	DC coupled mode possible
THS4500	370 MHz	DC coupled mode possible
THS4509	1900 MHz	AC coupled

Figure 2-8. AT84AS001 Used with AD8350 Amplifier (AC Coupled)

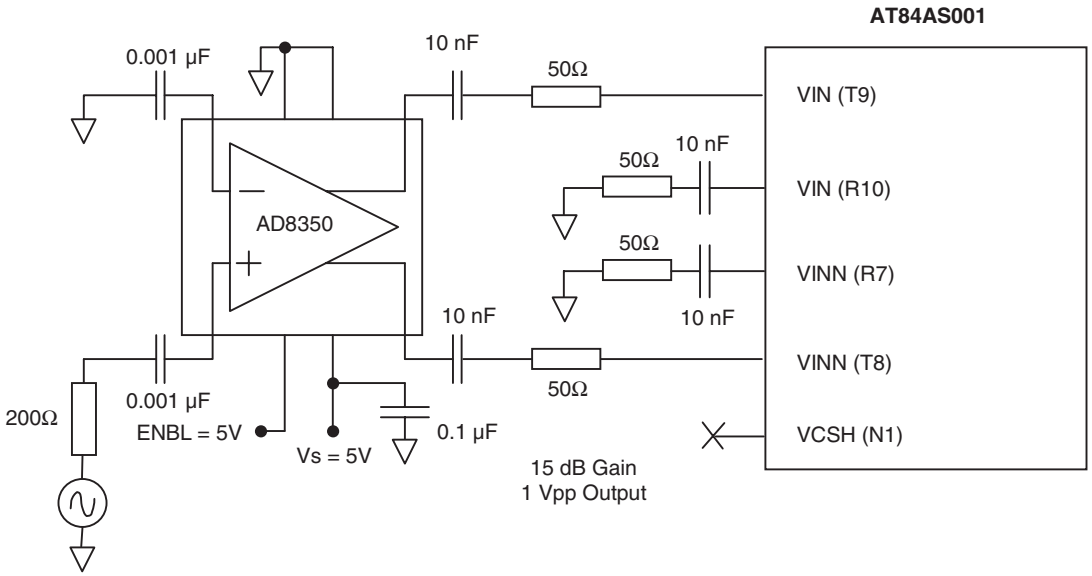


Figure 2-9. AT84AS001 Used with LT1993 Amplifier (AC coupled with 350 MHz Low Pass Filter)

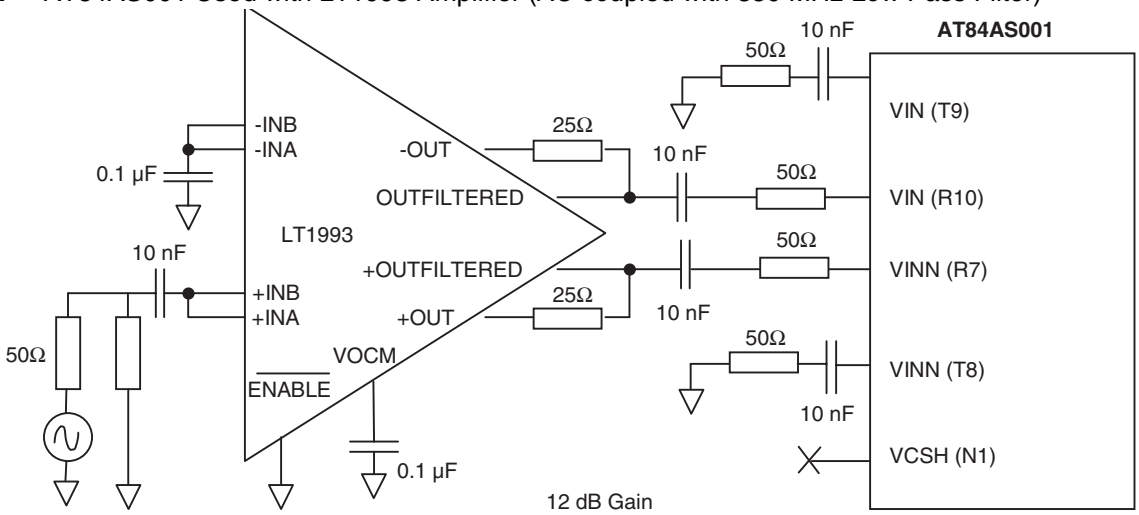
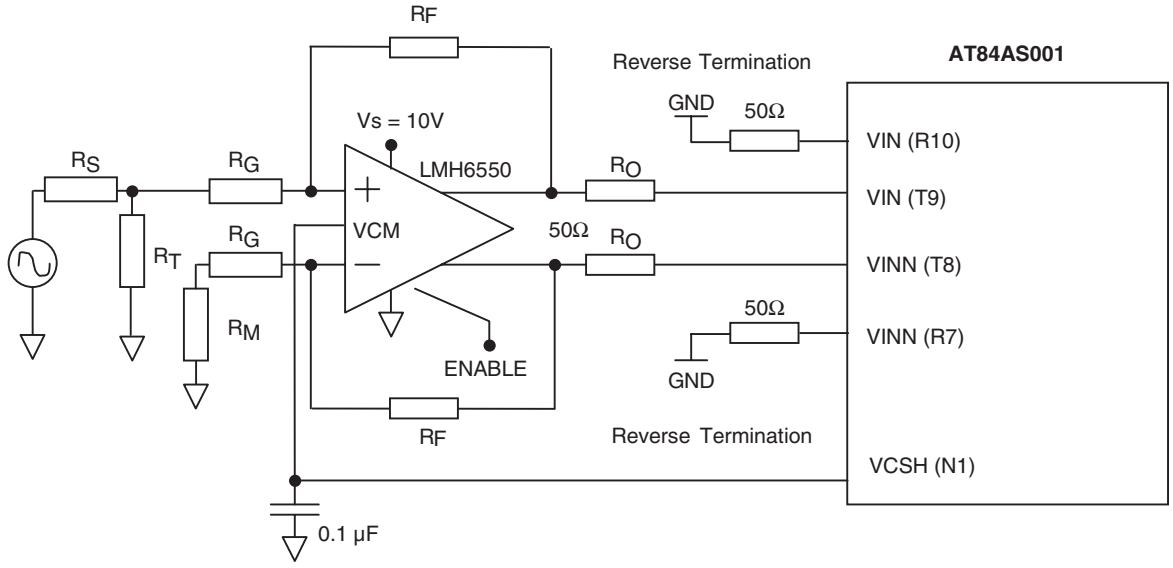


Figure 2-10. AT84AS001 Used with LMH6550 Amplifier (DC Coupled)



Note: 1 Vpp max required on the amplifier output.

$$R_{IN} = \frac{}{1-\left(\frac{R_F}{2*(R_F+R_G)}\right)}$$

$$R_T = \frac{1}{\left(\frac{1}{R_S}-\frac{1}{R_{IN}}\right)}$$

$$R_M = R_T \| R_S$$

Please refer to the Amplifiers datasheets for more information.

3. AT84AS001 ADC Output Terminations

The output data and clock of the AT84AS001 ADC are compatible LVDS.

The ADC outputs have then to be terminated with either one 100Ω resistor across the true and false data or with two 50Ω resistors as shown in Figure 3-1 on page 7 and Figure 3-2 on page 7.

Figure 3-1. AT84AS001 Output Data and Clock Interface in LVDS (One 100Ω Resistor)

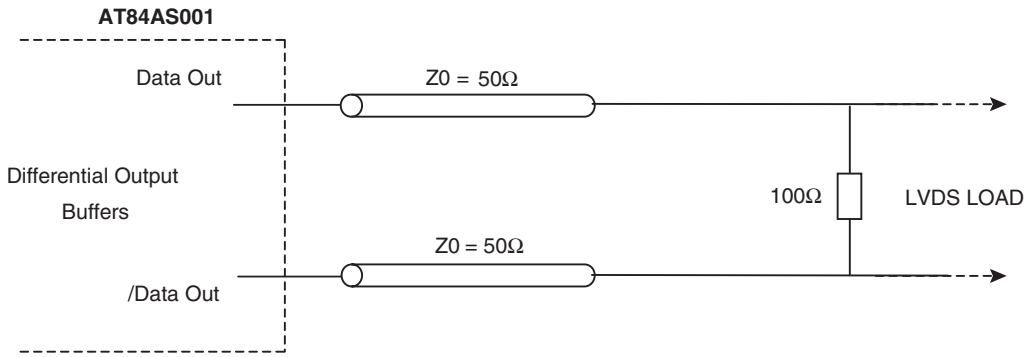
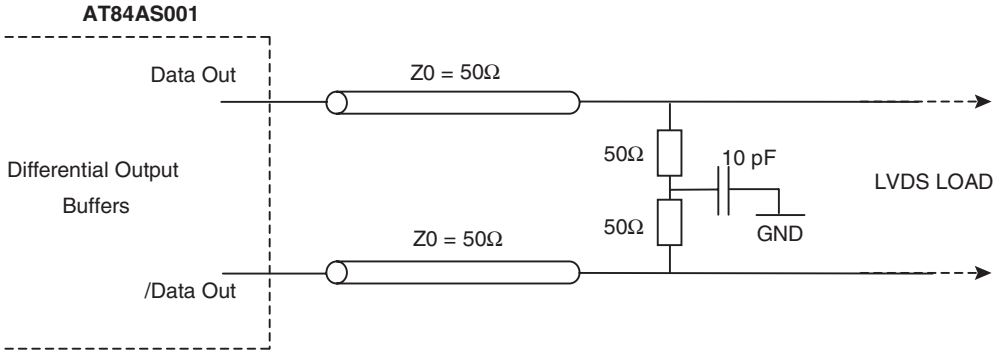


Figure 3-2. AT84AS001 Output Data and Clock interface in LVDS (two 50Ω to ground)



4. AT84AS001 ADC Settings

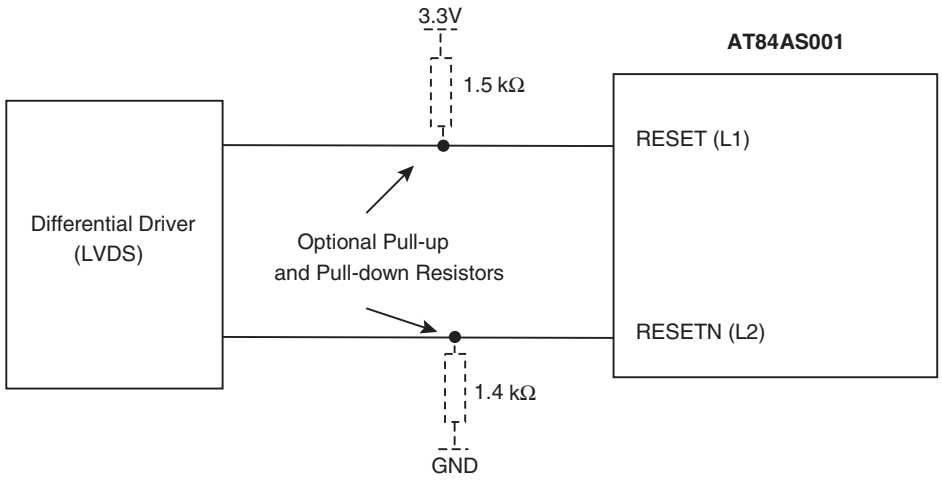
4.1 RESET Signals

The reset is not necessary to start the ADC but it is recommended to apply a reset after power up. It is active high (RESET LVDS high, RESETN LVDS low).

The RESET, RESETN buffer is an LVDS buffer with 100Ω on-chip termination.

Pull-up and pull-down resistors may be needed in the case where no signal is applied via the driver: the ADC will be by default in normal mode (reset inactive)

Figure 4-1. AT84AS001 RESET and RESETN Signals Driven by a Differential Driver



It is also possible to drive the RESET and RESETN signals in single-ended. In this case, RESETN needs to be connected to a fixed level and the active reset signal is applied on RESET.

Figure 4-2. AT84AS001 RESET and RESETN Signals Driven by a Differential Driver

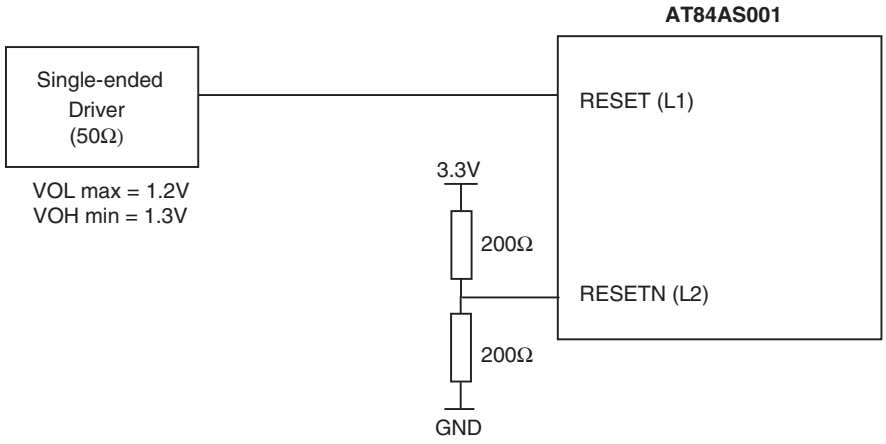
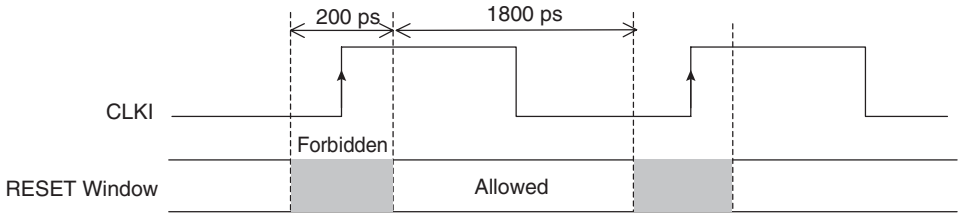


Figure 4-3. AT84AS001 RESET Allowed and Forbidden Zones



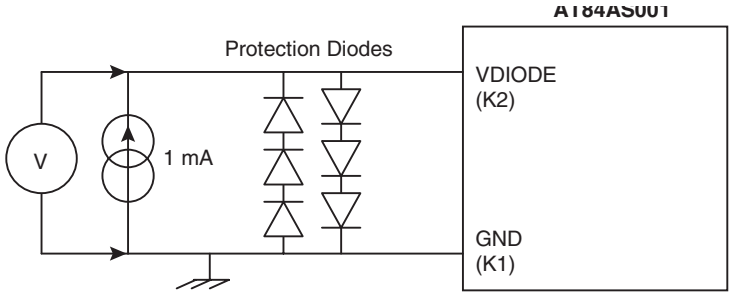
4.2 Diode

If you provide a 1 mA current (using a multimeter in current source mode) to the K2 pin of the ADC, the voltage across pin K2 and the closest ground pin of the ADC (for example pin K1) will give you the approximate die junction temperature with respects to the diode characteristic provided in the device datasheet (ref. 5412).

The ADC diode needs to be protected via 2 × 3 head-to-tail diodes.

If not used, the diode pin can either be left floating or connected to ground.

Figure 4-4. AT84AS001 DIODE



4.3 3-wire Serial Interface

Atmel ATmega128L AVR can be used to drive the 3-wire serial interface of AT84AS001 12-bit 500 Msps ADC.

In this first section, a simple configuration for the interfacing of the AVR with the ADC is provided.

Note: All the information contained in this document concerning the AVR comply with the version available at the date the document was created. This should be checked versus the current version available before design.

4.3.1 AT84AS001 12-bit 500 Msps ADC 3-Wire Serial Interface

Four signals of the AT84AS001 12-bit 500 Msps ADC can be driven via the ATmega128L AVR:

- The SMODE signal (pin P15): used in the ADC to activate the 3-wire serial interface
- The SCLK signal (pin N15): input clock for the serial interface
- The SDATA signal (pin N16): input data for the serial interface
- The SLDN signal (pin P16): beginning and end of register line for the serial interface

The 3-wire serial interface of the ADC only accepts 2.5V CMOS digital signals while Atmel ATmega128L must be supplied with V_{CC} = 2.7 to 5V.

It was thus necessary to add a buffer and line driver with 2.5-3.3V tolerant I/Os used as a translator in this mixed 2.5V and 3.3V environment.

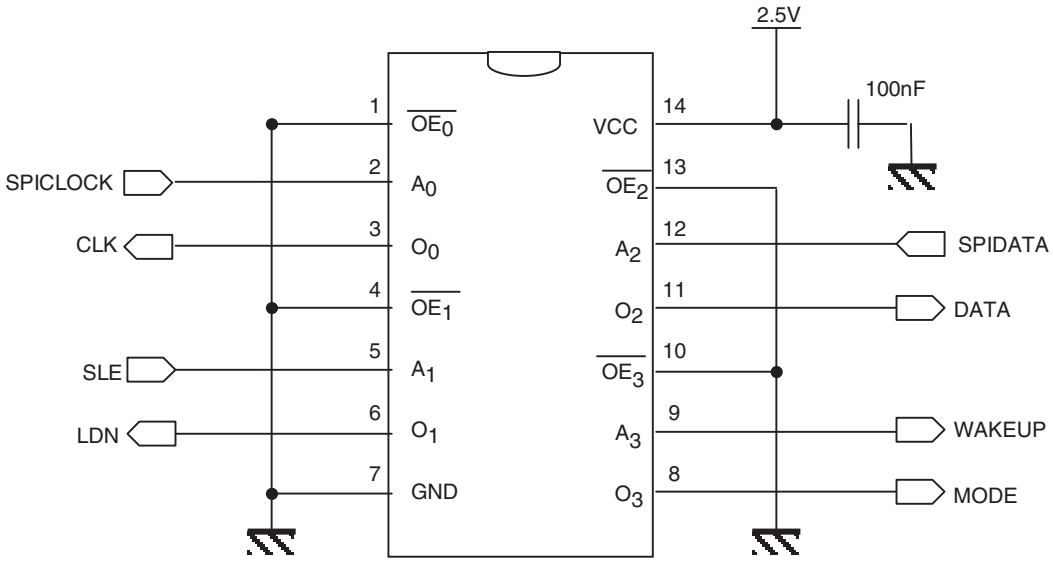
Because only four signals of the ADC have to be managed via the AVR, a quad buffer is sufficient to translate the four signals from the AVR (WAKEUP, SPICLOCK, SPIDATA, SLE) to the SMODE, SCLK, SDATA and SLDN signals (2.5V) of the ADC.

Possible devices allowing to perform the translation between the 3.3V of the AVR and the 2.5V required by the ADC are the 74LCX125 and 74LCX126 low voltage quad buffer and line with 5V tolerant Inputs/outputs or 74LCX244 low voltage octal buffer and line with 5V tolerant Inputs/outputs from any digital buffer manufacturers.

The 74LCX125 and 74LCX126 devices have the advantage of using only four inputs but their drawback is that you will not be able to have all 4 inputs on the same side of the device (easier layout).

Figure 4-5 illustrates the possible application diagrams for the 74LCX125 and 74LCX244 low voltage buffers with 5V tolerant I/Os.

Figure 4-5. Application Diagram Using the 74LCX125 Buffers

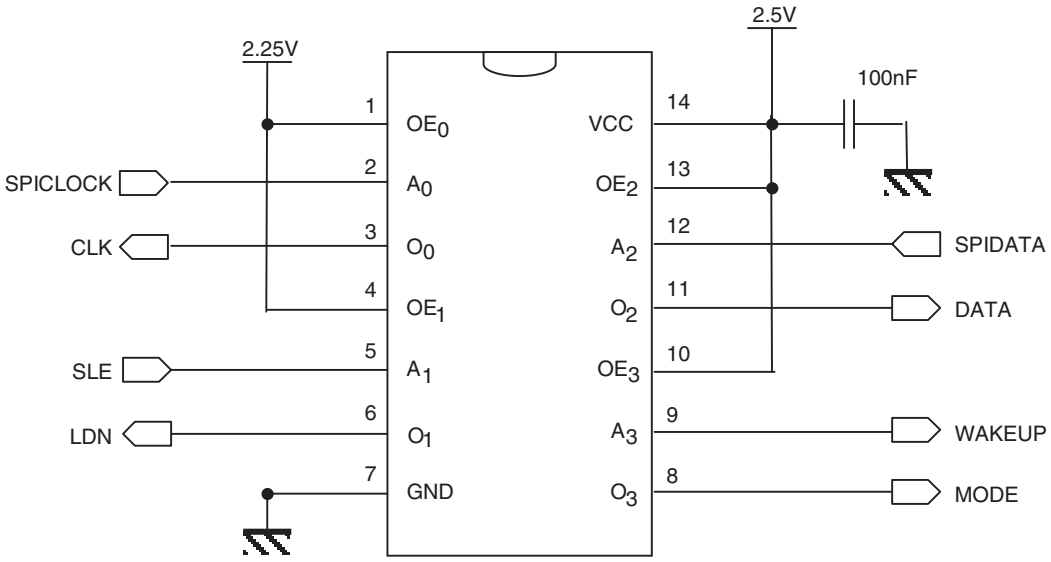


The truth table of the 74LCX125 device is shown in Table 4-1.

Table 4-1. 4LCX125 Truth Table

Inputs		Outputs
$\overline{OEn}$	A_n	O_n
L	L	L
L	H	H
H	Z	Z

Figure 4-6. Application diagram Using the 74LCX126 Buffers

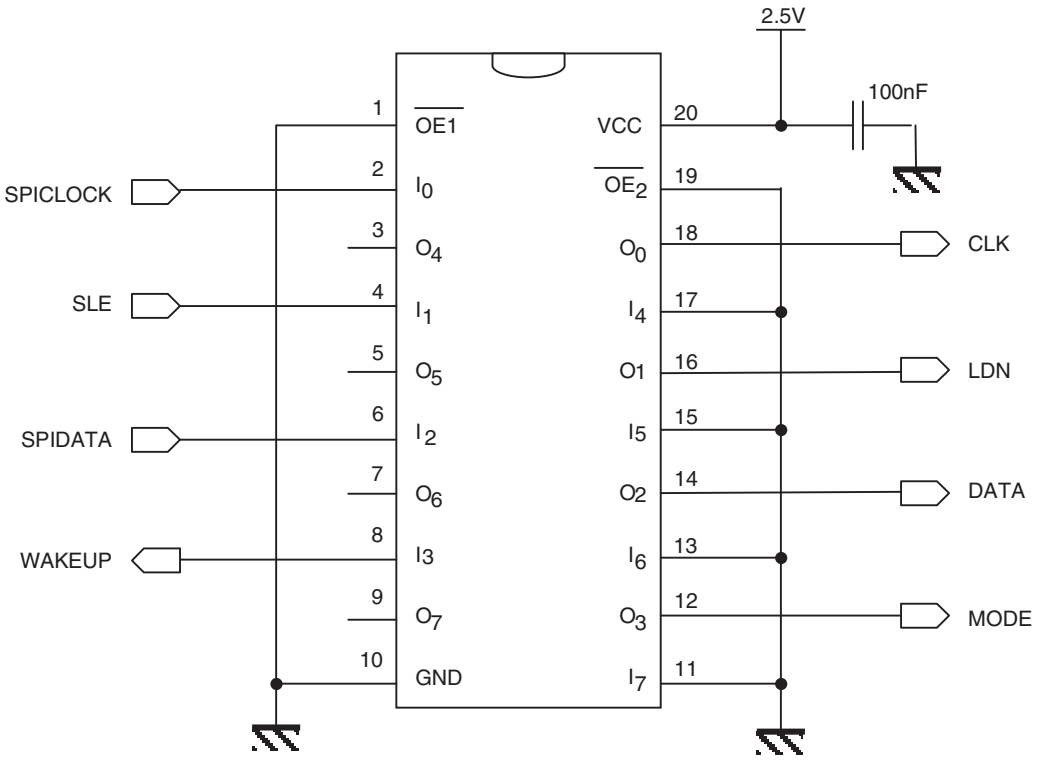


The truth table of the 74LCX126 device is shown in Table 4-2.

Table 4-2. 74LCX126 Truth Table

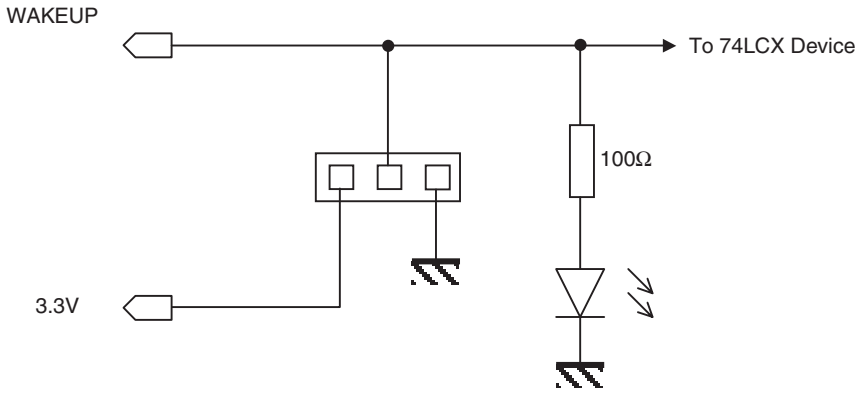
Inputs		Outputs
OE_n	A_n	O_n
H	L	L
H	H	H
L	Z	Z

Figure 4-7. Application Diagram Using the 74LCX244 Buffers



Note:
1. It is highly recommended to connect the unused inputs of the octal buffer to ground (directly to ground or via a 0Ω resistor in case you may need to access the signals in the future) so that the buffers will never toggle and consequently dissipate power while the buffers are not used.
2. It may be useful to connect the OE signals to ground (74LCX125 and 74LCX244 devices) or to 2.5V (74LCX126) via a 0Ω resistor in case you may need to change the signal level in the application.
3. The WAKEUP signal is considered here as an input for both the 74LCX device and the AVR. When connected to 2.5V, the serial interface is made active for the ADC. When connected to ground, the serial interface of the ADC is disabled. In the case of a demonstrator design, it may be useful to connect this signal to a LED to indicate that the 3-wire serial interface has been activated (LED lit) and to a push button (between ground and 3.3V), as illustrated in Figure 4-8 on page 13.

Figure 4-8. Management of the WAKEUP Signal (Manual for a Demonstrator Design for Example)



The truth table of the 74LCX244 device is shown in Table 4-3.

Table 4-3. 74LCX244 Truth Table

Inputs		**Outputs** (O_n, O_1, O_2, O_3)
$\overline{OE1}$	L_n	
L	L	L
L	H	H
H	X	Z
Inputs		Outputs (O_4, O_5, O_6, O_7)
$\overline{OE1}$	L_n	
L	L	L
L	H	H
H	X	Z

4.3.2 ATmega128L 8-Bit Microcontroller In-System Programmable Flash

On the AVR side, 8 bi-directional I/O ports are provided but only 4 bits of one port will be used for the interface between the 74LCX device and the AVR (for the WAKEUP, SPICLOCK, SPIDATA and SLE signals).

Because Port B provides the pins for the SPI channel, this is the port chosen for the four previously mentioned signals:

- SPICLOCK: PB1 (SCK = SPI bus serial clock)
- SPIDATA: PB2 (MOSI = SPI bus Master Output/Slave Input)
- SLE: PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0)
- WAKEUP: PB5 (OC1A = Output Compare and PWM Output A for Timer/Counter1)

The other pins PB0 ($\overline{SS}$), PB6 (OC1B) and PB7 (OC2/OC1C) can be left floating (open).

Pin PB3 (MISO = SPI Bus Master Input/Slave Output) needs to be pulled up to 3.3V via a 1 kΩ resistor in order to be forced to a high level and not left open.

Pins SPICLOCK = PB1 and SPIDATA = PB2 need to be pulled down to ground via a 10 kΩ resistor to be forced to low level (inhibition of the SPI during reset of the microcontroller).

Pin SLE = PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0) needs to be pulled up to 3.3V via a 3.3 kΩ (or 1 kΩ if the power consumption is not critical) resistor in order to protect the line during reset of the microcontroller (in which phase the signal becomes an input).

Ports A and C of the AVR can be left floating (open) but have to be internally configured with pull-ups.

For Port D, pins PD7, PD6, PD5 and PD4 can be left unused (open) but have to be internally configured with pull-ups. Pins PD3, PD2, PD1 and PD0 have to be pulled up in order to inhibit external interrupts.

For port E, pins PE3 and PE2 can be left unused (open) but have to be internally configured with pull-ups. Pins PE7, PE6, PE5 and PE4 have to be pulled up to 3.3V via a 3.3 kΩ (or 1 kΩ if the power consumption is not critical) resistor in order to inhibit external interrupts.

PE1 and PE0 can be used as the Programming Data Output (TX) and Input (RX) to be connected to the TX and TX of the system (in the case of the AT84AS001-EB evaluation board, these signals are sent to the PC via an RS232 port).

All the pins of Port F have to be connected to ground so that they are in a known fixed state (no internal pull-down available for these pins).

All pins of Port G can be left floating (open).

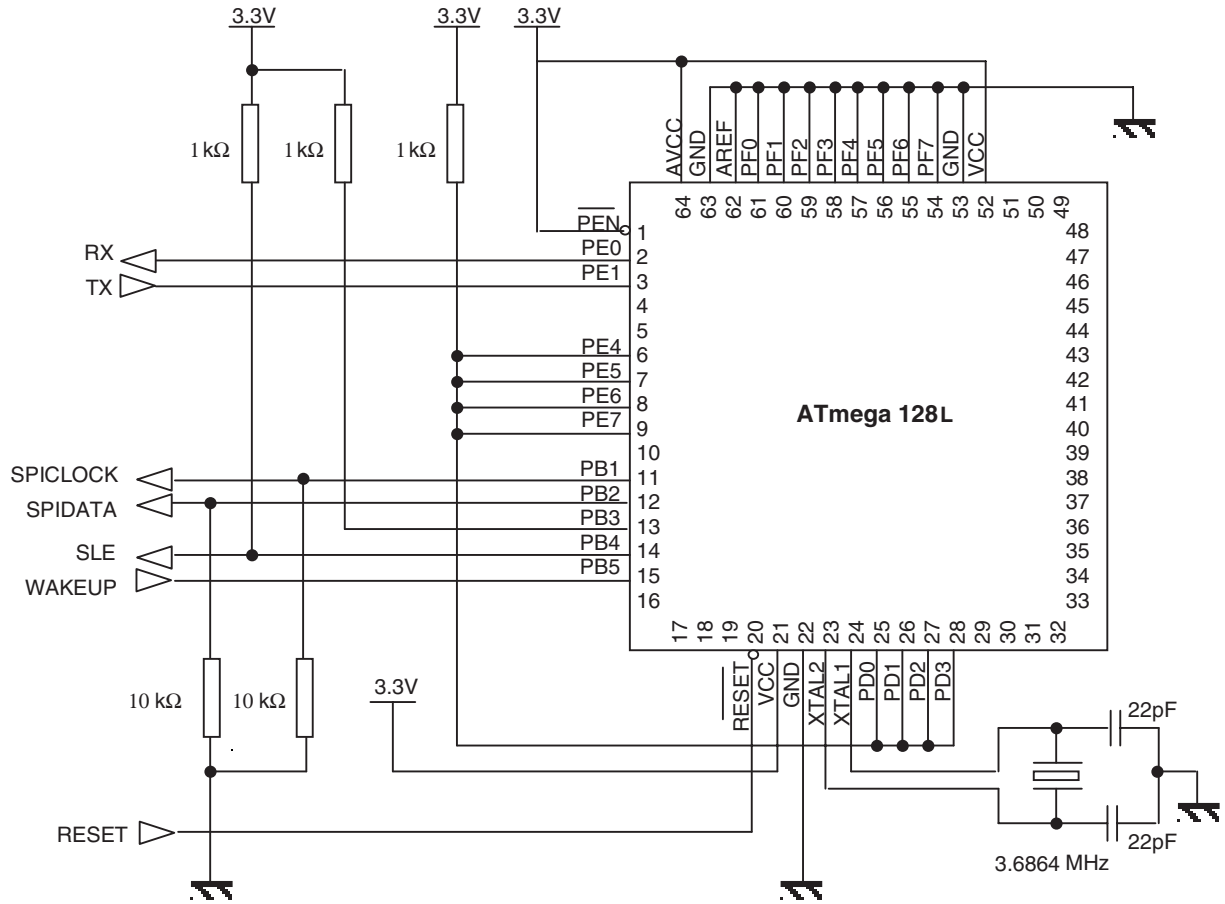
Finally, the five remaining signal pins are to be connected as follows:

- $\overline{PEN}$ = programming enable pin for the SPI serial programming mode, to be connected to V_{CC} = 3.3V to activate the SPI programming mode
- $\overline{RESET}$ = Master reset of the AVR, to be connected to a microcontroller supervisory circuit (for example and for information only: MCP809 from Microchip™, one possible configuration is given in Section 5.
- XTAL1 and XTAL2: input and output to/from the inverting Oscillator amplifier.
- AREF = analog reference for the A/D internal converter

Finally, V_{CC} and AV_{CC} have to be connected to a 3.3V source and GND, to ground.

This gives the following configuration as shown in figure Figure 4-9 (AVR only):

Figure 4-9. ATmega128L Application Diagram (for Use with AT84AS001 12-bit 500 Msps ADC)



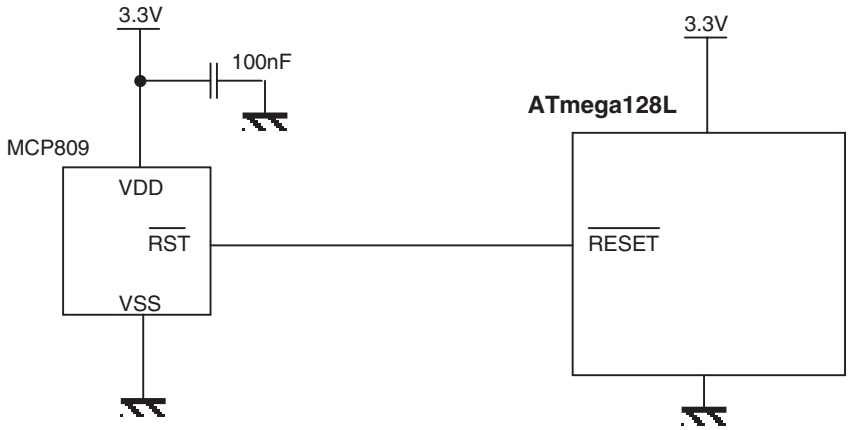
Note: Only the connected pins are shown (the unused pins are left open).

The reset of the ATmega128L AVR can be controlled thanks to a *voltage supervisory circuit* comparable to the MCP809 device from Microchip (for information only). Such a device allows you to keep the microcontroller in reset until the system voltage has reached its final level. It also ensures that the microcontroller will be reset whenever a power drop occurs.

Any voltage supervisory circuit compliant with V_{CC} = 3.3V and with a reset pulse longer than 50 ns minimum width (active low) would work.

Here the supervisory device from Microchip reset voltage level is set to 3.0V with a pulse of 350 ms.

Figure 4-10. Typical Application Diagram for the $\overline{\text{RESET}}$ Circuit



4.3.3 Programming of Atmel ATmega128L AVR

Atmel ATmega128L AVR can be programmed thanks to the AVR ISP (In-System Programmer) tool using AVR Studio®, Atmel's Integrated Development Environment (IDE) for code writing and debugging. The programming software can be controlled from both Windows environment and a DOS command-line interface.

For more information on the AVR Studio programming software, please refer to Atmel Web site.

The programming of the AVR requires the use of a 6- or 10-pin ISP connector.

In our case, an HE10 6-pin connector is chosen:

- Pin 1 = PDO, AVR Programming Data Out
- Pin 2 = AVR Target application card power supply (= 3.3V)
- Pin 3 = SCK, AVR programming clock
- Pin 4 = PDI, AVR programming Data In
- Pin 5 = RST_ISP, AVR programming Reset
- Pin 6 = ground

Note:
1. The ISP card power supply comes from the AVR card (3.3V). There is no need for an additional power supply.
2. The mode used to program the AVR is a serial mode.

The RST_ISP signal is used to manage the AVR mode: programming mode or SPI mode.

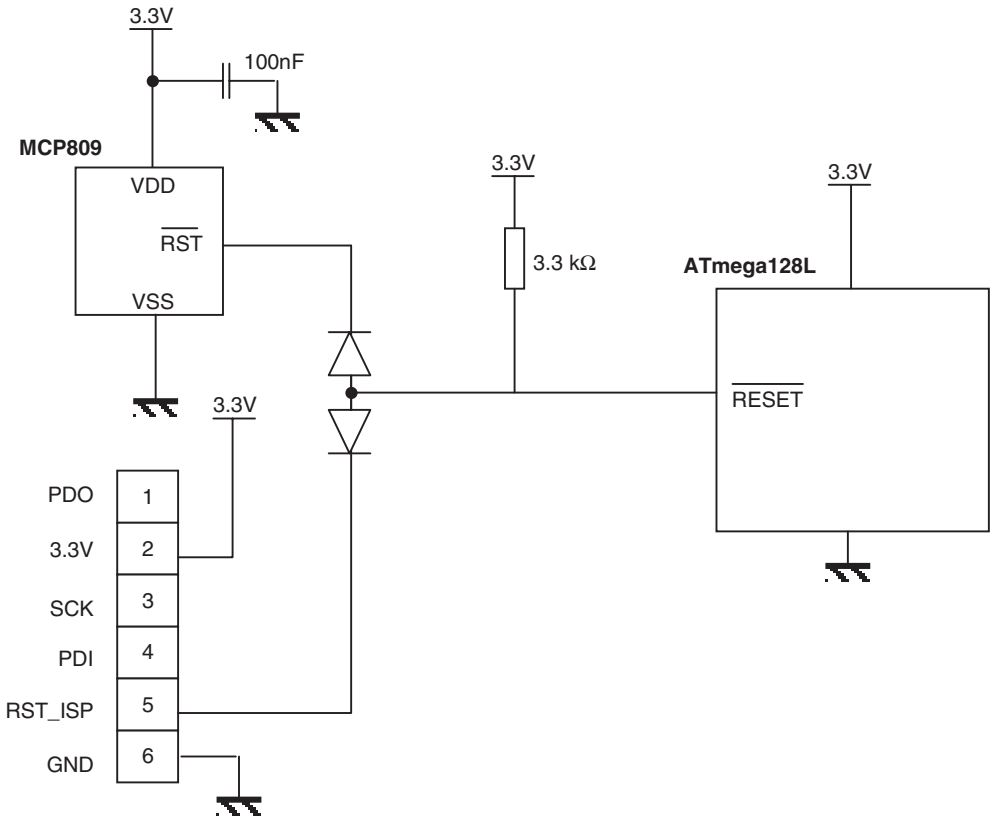
This signal is sent to the $\overline{\text{RESET}}$ of the AVR so that:

- When RST_ISP = 0, $\overline{\text{RESET}}$= 0 and the AVR is in reset (ISP mode), PE0 is used as the Data In for the programming of the AVR, PE1 is the Data Out and PB1 is the programming clock
- When RST_ISP = 1, $\overline{\text{RESET}}$ = 1 and the AVR is in normal mode, PE0 = RX, PE1 = TX, PB1 = SPICLOCK

The three AVR signals mentioned previously (PE0, PE1 and PB1) thus have two functions, controlled by RST_ISP. Be careful when implementing these signals (series resistors on the SCK, PDO and PDI data may be needed to manage possible conflicts, see Section 5.).

Similarly, the $\overline{\text{RESET}}$ signal has two possible sources: the signal generated by the microcontroller supervisory device and the RST_ISP signal from the ISP. In order to manage this signal and in case the microcontroller supervisory device is not with open collector (as for the MCP809 device), two head-to-tail diodes are required, as illustrated in Figure 2-3 on page 3. The line going to the $\overline{\text{RESET}}$ signal of the AVR is then in open-collector and a pull-up resistor (3.3 kΩ) to 3.3V is required.

Table 4-4. Typical Application Diagram for the $\overline{\text{RESET}}$ Circuit with the ISP Connector

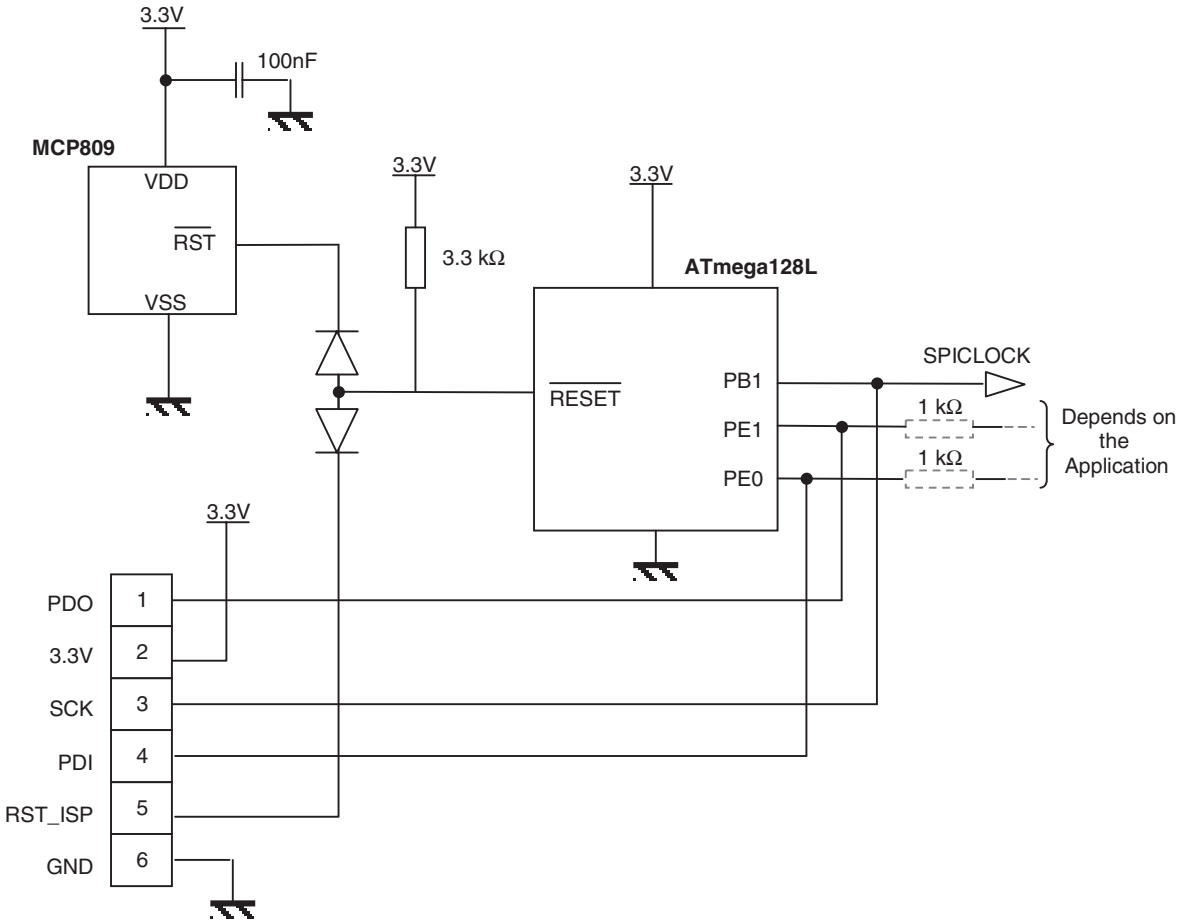


A basic diagram illustrating the interface between the ISP connector and the AVR is shown in Figure 4-11 on page 18.

In this general case, PE1 and PE0 interconnections are left to the user's responsibility. In case of possible conflict on these signals (example PE1 could be driven by both PDO and another signal), it may be necessary to add a 1 kΩ resistor in series so that any voltage difference will be dissipated in this resistor.

No additional protection is required on the AVR PB1 signal there is no conflict between SCK and SPICLOCK. It is nevertheless recommended to set the ADC in standby mode or disable the 3-wire serial interface thanks to the MODE bit during programming of the AVR.

Figure 4-11. General Application Diagram for the ISP Connector and the AVR



In case the RX and TX signals are to be connected to a transceiver (RS232 connector to a PC for example), in order to multiplex the signals of the AVR (PE0, PE1 and PB1) between the ISP and the RX, TX and SPICLOCK signals, a low voltage buffer/line driver with 3-state outputs device can be used. The 74LVQ241 devices are well-suited for this application (clock driver and bus oriented transmitter or receiver).

The 74LVQ241 device has eight inputs and eight corresponding outputs and 2 - 3-state output enable inputs. These 2 - 3-state output enable inputs can be managed by the RST_ISP signal:

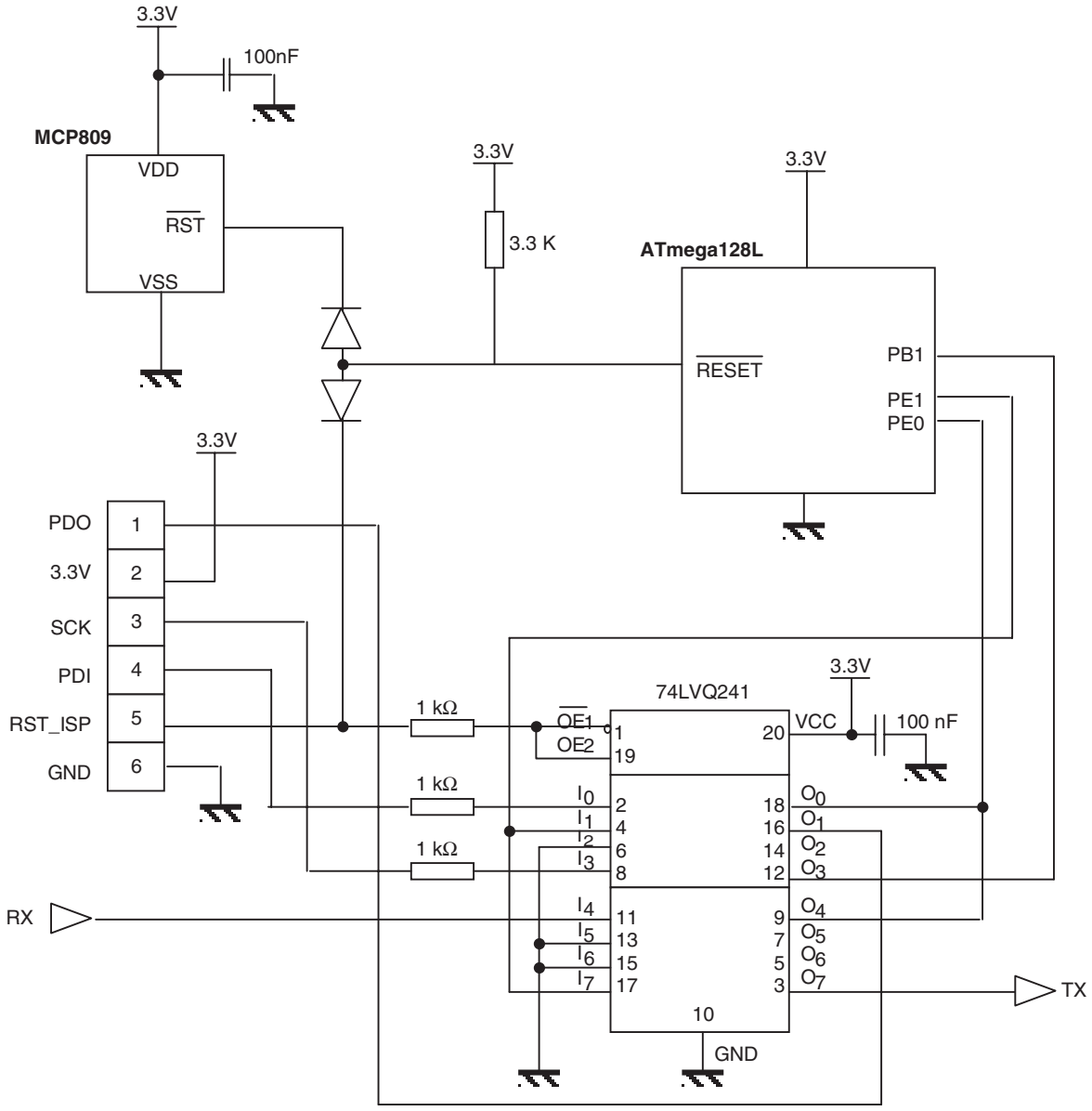
- When RST_ISP = 0, $\overline{0E1}$= OE2 = 0 and then O0 to O3 are low and O4 to O7 are in high impedance
- When RST_ISP = 1, $\overline{0E1}$ = OE2 = 1 and then O_0 to O_3 are in high impedance and O_4 to O_7 are low

The truth table of the 74LVQ241 device is shown in Table 4-5 on page 19.

Table 4-5. 74LVQ241Truth Table

Inputs		**Outputs**
$\overline{OE1}$	L_n	**(O_n, O_1, O_2, O_3)**
L	L	L
L	H	H
H	X	Z
Inputs		Outputs
$\overline{OE2}$	L_n	(O_4, O_5, O_6, O_7)
L	L	Z
L	H	L
H	X	H

Figure 4-12. Typical Application Diagram with the 74LVQ241



Note:
1. The unused inputs are connected to ground to prevent them from toggling.
2. and OE2 are connected together and to RST_ISP via a 1 kΩ resistor.
3. SCK, RST-ISP and PDI are connected to I3, and OE2 and I0 respectively via 1 kΩ resistors in order to manage the possible conflicts on the signals in case the connector is used to program several AVRs.
4. PE0 is connected to both O0 and O4, which are respectively the inputs corresponding to SCK and RX: PE0 will be either generated by SCK or RX depending on the mode.
5. PE1 is connected to both I1 and I7, which are respectively the outputs corresponding to PDO and TX: PE1 will either generate by PDO or TX depending on the mode.

The programming of the AVR itself as well as the connections of the RX and TX signals are not described in this application note as they depend on the final application.

For more information on the AT84AS001 12-bit 500 Msps ADC, please contact the Broadband Data Conversion hotline at hotline-bdc@e2v.com.

For more information on the AVR, please contact the AVR hotline at avr@atmel.com.

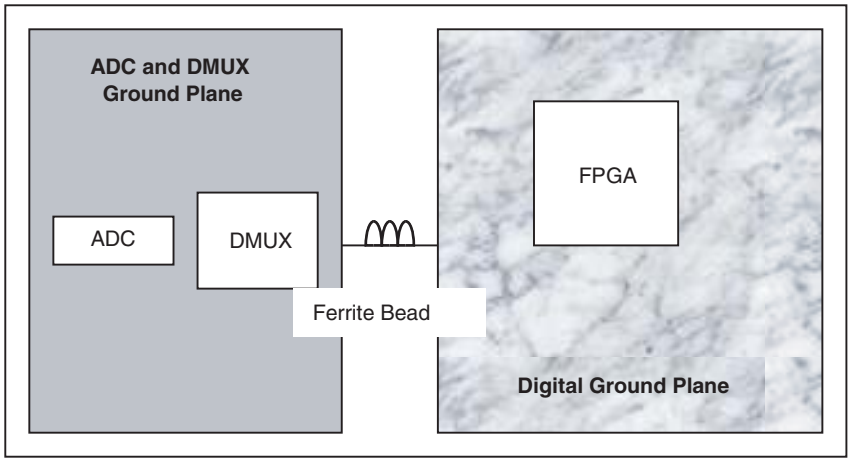
5. Grounding and Power Supplies

5.1 Ground Plane

It is recommended to separate the ground plane of the ADC (one common ground plane GND) and the system's ground plane (for example FPGA digital ground plane).

These two ground planes can be reunited by one point via a ferrite bead as illustrated in Figure 5-1.

Table 5-1. Schematic View of the System Board Ground Plane (Example)



It is also recommended to plan to have one ground plane for each signal plane in the board layer stacking (example: Layer 1 = signal layer, layer 2 = ground layer, etc.).

5.2 Power Supply Planes

The ADC requires three power supplies:

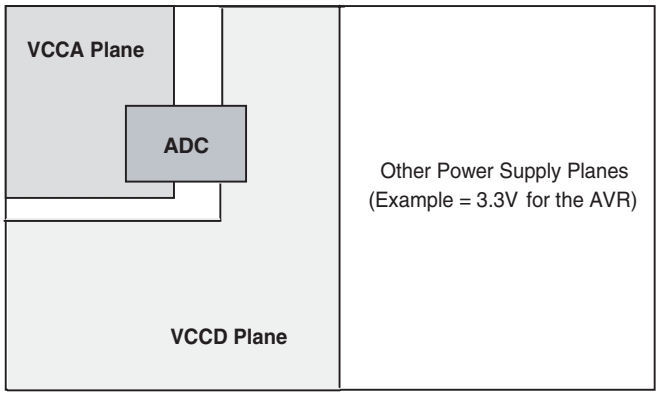
- V_{CCA} = 5V analog
- V_{CCD} = 3.3V digital
- V_{CCO} = 2.5V (for the outputs and the 3-wire serial interface)

At least, three different power planes are required for the ADC.

It is recommended to place the power supplies layers in between two ground layers for better isolation.

You can use the same layer for both V_{CCA} and V_{CCD} power supplies but using separate planes. As the V_{CCA} plane concerns only the analog part of the AT84AS001 device, the less extended it is the better. On the other hand, it may be easier to use another layer for V_{CCO}.

Table 5-2. Schematic View of V_{CCA} and V_{CCD} Planes



As concerns the power supplies decoupling and bypassing, each incoming power supply should be bypassed by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

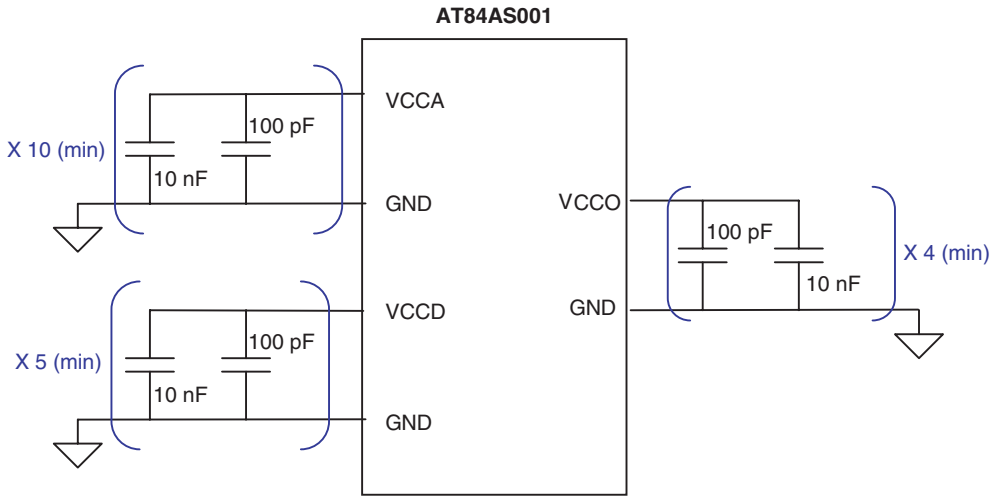
Each power supply should be decoupled as close as possible to the AT84AS001 device by 10 nF in parallel with 100 pF surface mount chip capacitors (the 100 pF capacitors should be mounted first).

To determine how many decoupling capacitor pairs are required, it is necessary to count how many groups of neighboring power supply pins attributed to the same value can be defined. Each group should then be decoupled y at least one pair of 10 nF in parallel with 100 pF capacitors.

The minimum required pairs of capacitors by power supply type is:

- Ten for V_{CCA}
- Five for V_{CCD}
- Four for V_{CCO}

Figure 5-1. AT84AS001 Power Supply Decoupling Scheme



5.3 Board Layout Recommendations

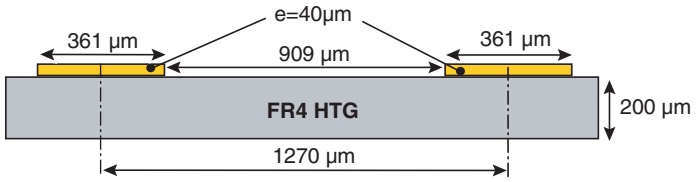
5.3.1 Clock and Analog Input Signals

Special care must be taken for the routing of the analog and clock input signals for optimum performance in the high frequency domain.

In the case of the use of FR4 HTG (ISOLA IS410 with 45% resin content) epoxy dielectric material for the board, the following rules apply:

- 50Ω lines matched to ± 0.1 mm (in length) between VIN and VINN or CLKI and CLKIN
- 1.27 mm pitch between the differential traces
- 361 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the VIN and VINN or CLKI and CLKIN ball footprints

Table 5-3. Board Layout for the Differential Analog and Clock Inputs

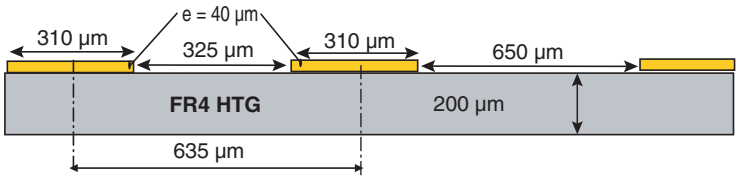


5.3.2 Output data signals

In the case of the use of FR4 HTG epoxy dielectric material for the board, the following rules for the digital output lines apply:

- 50Ω lines matched to ± 0.1 mm (in length) between signal of the same differential pair
- 80 mm max line length
- ± 1 mm line length difference between signals of two differential pairs
- 635 µm pitch between the differential traces
- 650 µm between two differential pairs
- 310 µm line width
- 40 µm thickness

Figure 5-2. Board Layout for the Differential Digital Outputs



How to reach us

Home page: www.e2v.com

Sales Office:

Northern Europe

e2v ltd

106 Waterhouse Lane

Chelmsford

Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax:: +44 (0)1245 492492

E-Mail: enquiries@e2v.com

Southern Europe

e2v sas

16 Burospace

F-91572 Bièvres

Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

E-Mail: enquiries-fr@e2v.com

Germany and Austria

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax:: +49 (0) 8142 284547

E-Mail: enquiries-de@e2v.com

Americas

e2v inc.

4 Westchester Plaza

Elmsford

NY 10523-1482

USA

Tel: +1 (914) 592 6050 or

1-800-342-5338,

Fax:: +1 (914) 592-5148

E-Mail: enquiries-na@e2v.com

Asia Pacific

e2v

Bank of China Tower

30th floor office 7

1 Garden Rd Central

Hong Kong

Tel: +852 2251 8227/8/9

Fax: +852 2251 8238

E-Mail: enquiries-hk@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

hotline-bdc@e2v.com