AT84AD001B and AT84AD004B Dual ADC

Application Note

1. Introduction

This application note aims at providing you some recommendations to implement the AT84AD001B 8-bit 1 Gsps and/or AT84AD004B 8-bit 500 Msps dual ADCs in your system.

It first presents the ADC input/output interfaces and then provides some recommendations as regards the device settings and board layout to obtain the best performance of the device.

This document applies to the:

- AT84AD004B Dual 8-bit 500 Msps ADC
- AT84AD001B Dual 8-bit 1 Gsps ADC

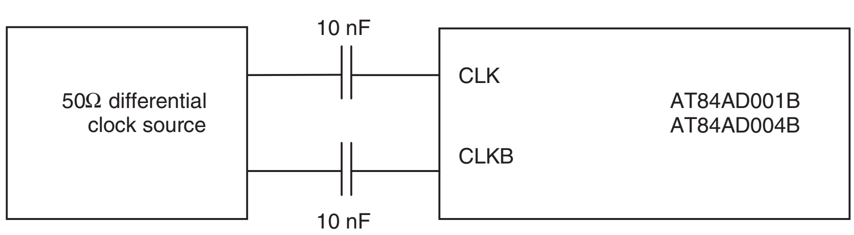
2. AT84AD001B and AT84AD004B ADC Input Terminations

2.1 Clock Input

In the case of the AT84AD001B Dual 8-bit 1 Gsps and AT84AD004B Dual 8-bit 500 Msps ADC, the input clock (I or Q) can be indifferently driven differentially or single-ended. In all cases however, the input clock needs to be AC coupled as the common mode of the clock differential pair is $V_{CCD}/2$.

The clock differential buffer is 2 × 50Ω terminated to $V_{CCD}/2$ and this is why it is necessary to terminate the unused clock signal via both a capacitor and a 50Ω resistor to ground in single-ended mode, as described in Figure 2-2 on page 2.

Figure 2-1. Clock Input AC Coupled Differential Scheme



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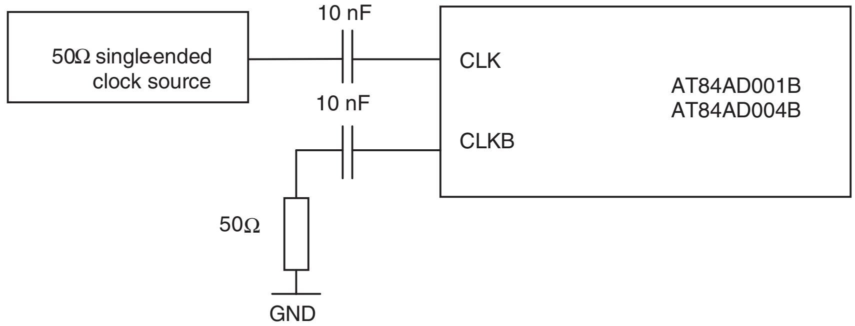
for the latest version of the datasheet

Figure 2-2. Clock Input AC Coupled Single-ended Scheme



Note: When only clock I is used, it is not necessary to add the capacitors on the CLKQ and CLKQN signal paths; they might be left floating.

In the case of an application requiring a fixed clock frequency, it is recommended to filter the clock signal for improved jitter performance. The benefits of filtering the clock signal can be quantified to a 1 or 2 dB improvement in the SNR figure resulting in an increase of about 0.1 to 0.2 bit in the ENOB figure.

The filtering can be done using a narrow-band filter but because it is beyond the stop-band frequency the noise is not filtered out, it might be necessary to have a low-pass filter after the narrow band filter.

Table 2-1. References for Filters (for Information Only)

Filter Type	Reference	Frequency
Band pass	4DF12-500/X2-MP (Lorch Microwave)	500 MHz
Band pass	9BP8-500/30-S (Lorch Microwave)	500 MHz
Low pass	4LP7-550X-MP (Lorch Microwave)	550 MHz
Band pass	4DF12-1000/X2-MP (Lorch)	1000 MHz
Low pass	5LP7-1000X-MP (Lorch)	1000 MHz

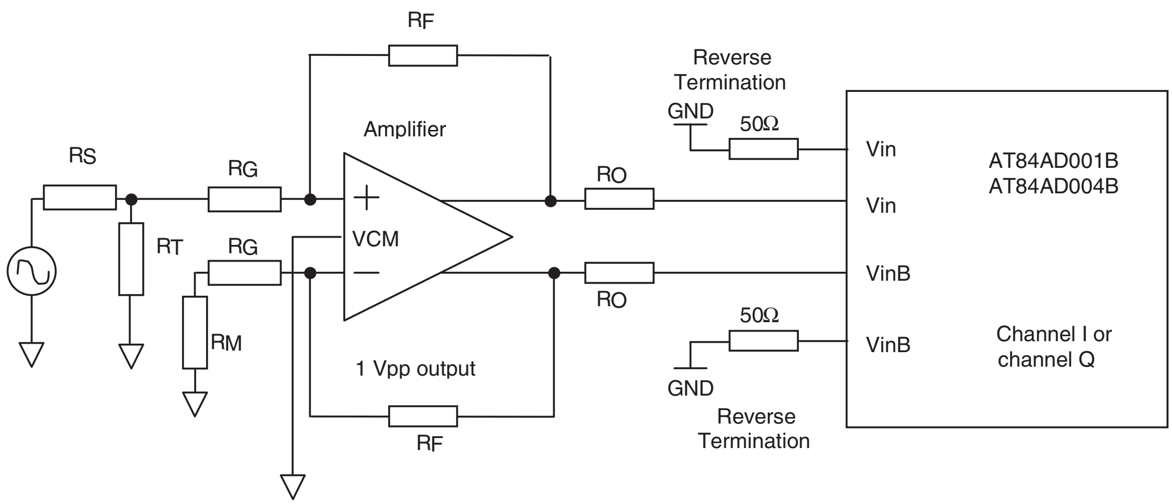
2.2 Analog Input

Although the input clock can be indifferently driven differentially or single-ended with the AT84AD001B and AT84AD004B ADCs, the analog input should be driven differentially. It can be used in AC or DC coupled mode. The input common mode is ground.

The analog inputs of the Dual ADCs were designed with a double pad implementation as illustrated in Figure 2-3. The reverse pad for each input should be tied to ground via a 50Ω resistor.

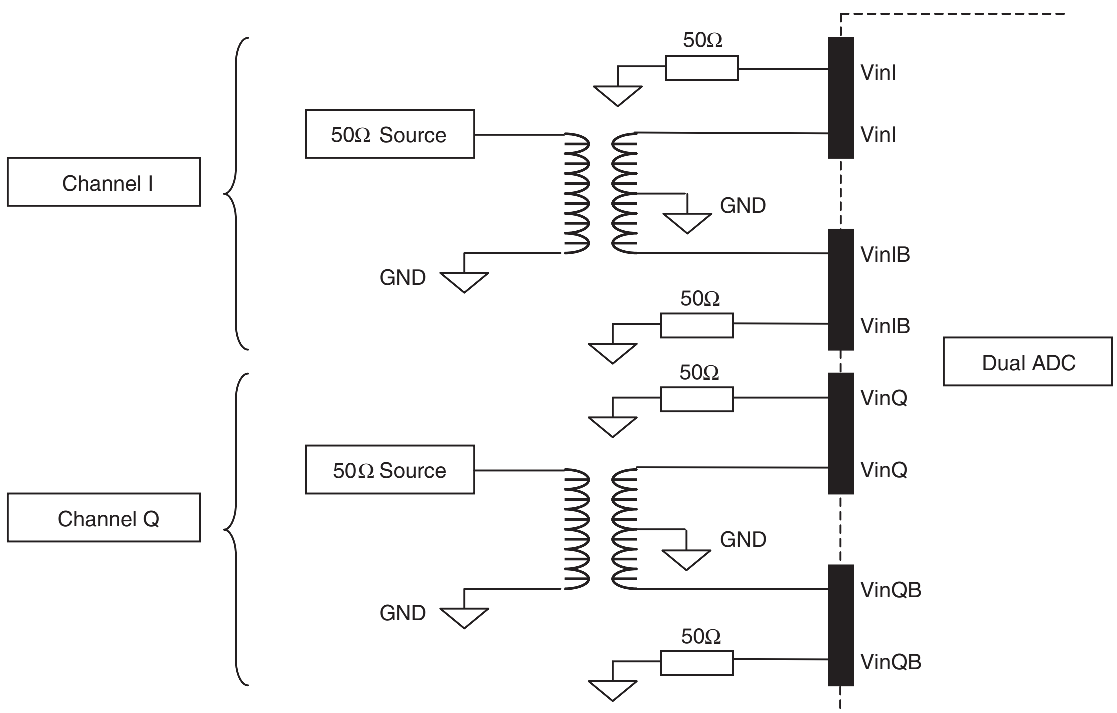
The analog inputs must be used in differential mode *only*.

Figure 2-3. ADC Analog Inputs Termination Method in DC Coupling Mode (Channel I or Q)



Note: Only one channel is represented.

Figure 2-4. ADC Analog Inputs Termination Method in AC Coupling Mode



3. AT84AD001B and AT84AD004B ADC Output Terminations

The output data and clock of the AT84AD001B and AT84AD004B ADCs are in LVDS.

The ADC outputs should then be terminated with either one 100Ω resistor across the true and false data or with two 50Ω resistors as shown in Figure 3-1 and Figure 3-2 on page 4.

Figure 3-1. AT84AD001B and AT84AD004B Output Data and Clock Interface in LVDS (One 100Ω Resistor)

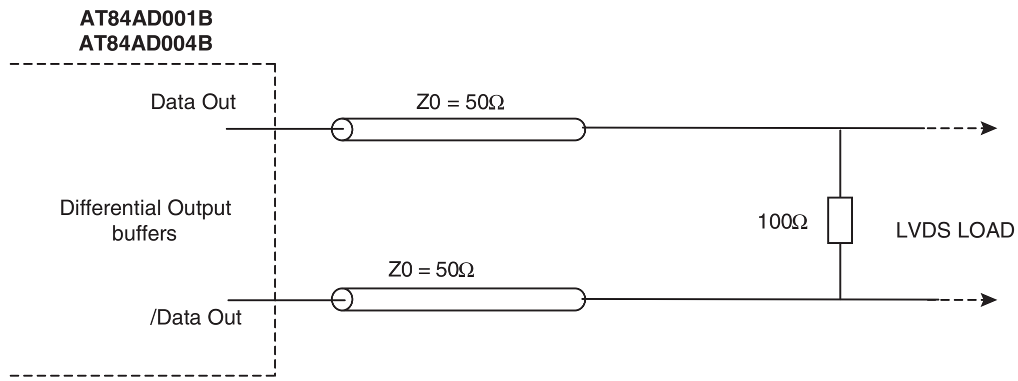
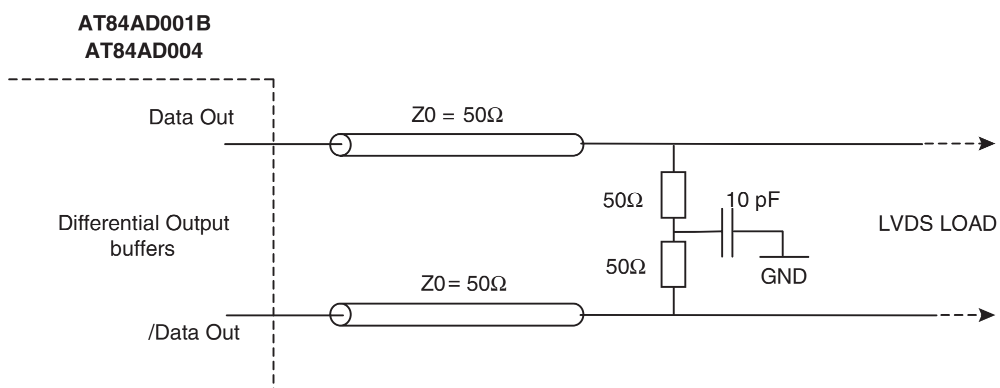


Figure 3-2. AT84AD001B and AT84AD004B Output Data and Clock Interface in LVDS (Two 50Ω to Ground)



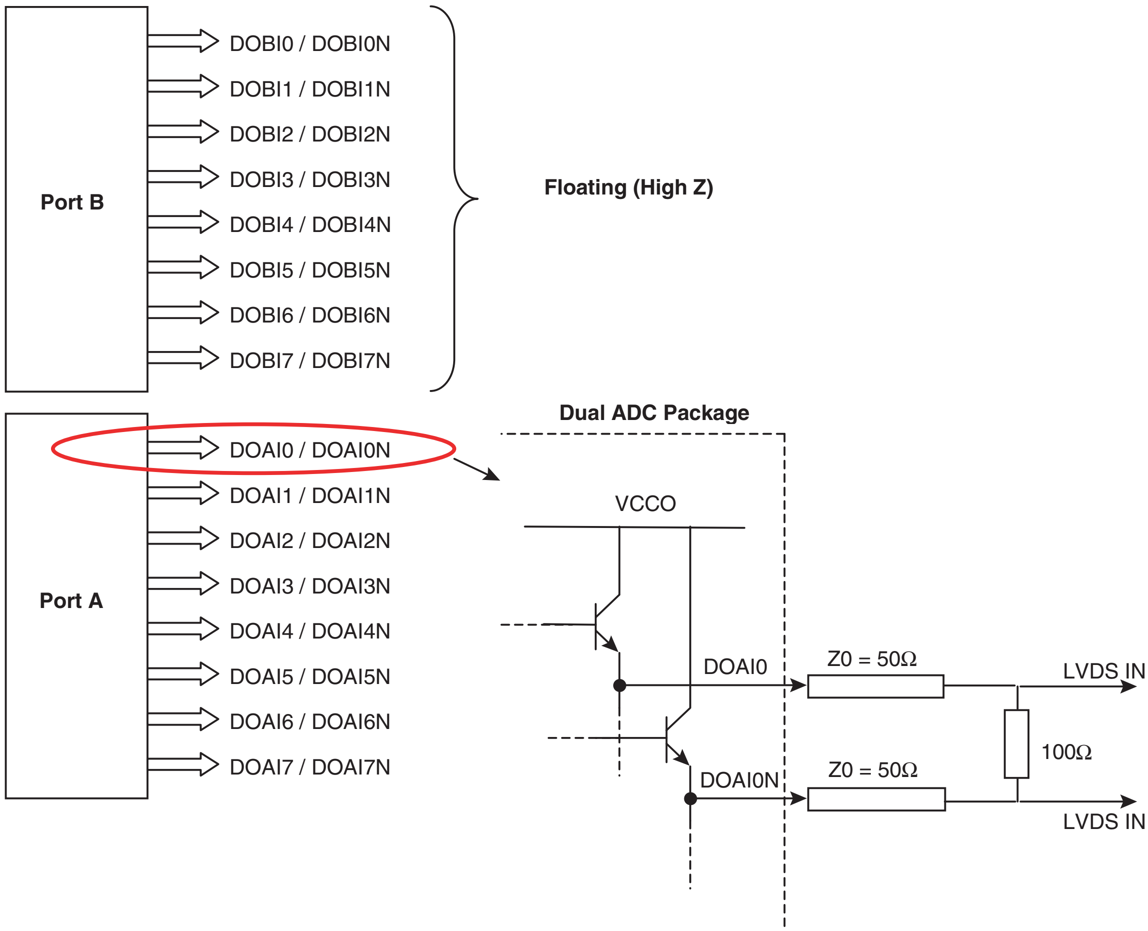
When using the integrated DEMUX in 1:1 ratio, the valid port is port A, whereas the port B stays unused.

Port A functions in LVDS mode and the corresponding outputs (DOAI or DOAQ) should be 100Ω differentially terminated as shown in Figure 3-3 on page 5.

The pins corresponding to Port B (DOBI or DOBQ pins) have to be left floating (in high impedance state).

Figure 3-3 on page 5 shows the example for a 1:1 ratio of the integrated DMUX for channel I (the same applies for channel Q).

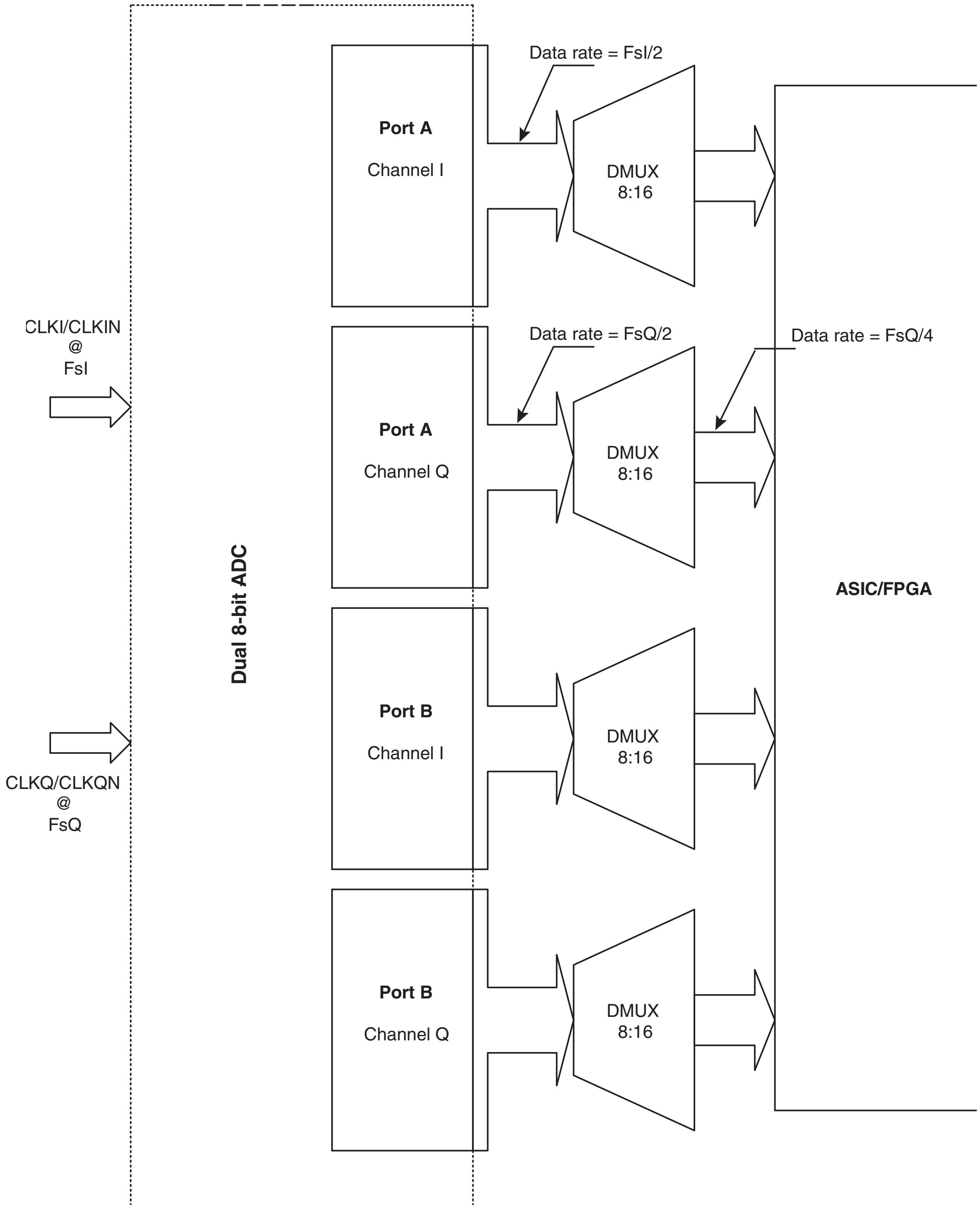
Figure 3-3. Example of Termination for the Dual ADC Channel I used in DMUX 1:1 Ratio (Port B Unused)



Note: If the outputs should be used in single-ended mode, it is recommended to terminate the True and False signals with a 50Ω resistor.

Figure 3-4 illustrates the configuration of the dual ADC (1:2 DMUX mode, independent I and Q clocks) driving an LVDS system (ASIC/FPGA) with potential additional DMUXes used to halve the speed of the dual ADC outputs.

Figure 3-4. Dual ADC + ASIC/FPGA Load Block Diagram



Note: The demultiplexers might be internal to the ASIC/FPGA system.

4. Auto-Calibration Function

The connection to the 3-wire serial interface of the AT84AD001B and AT84AD004B enables the use of the auto-calibration function which is implemented in these two circuits. This function offers the possibility of reducing offset matching for the two ADC cores and diminishing the gain matching between the two channels.

The internal digital calibration starts after the 3-wire serial interface loading has been completed. During the calibration the two ADCs are disabled and use internal references. The output bit CAL goes to a high level during the entire calibration phase. When this bit returns to a low level, the two ADCs are calibrated with offset and gain, and can be used again for a standard data acquisition.

The duration of the calibration is a multiple of the clock frequency ClockI (master clock). Even if a dual clock scheme is used during calibration, ClockQ will not be used. If only one channel is selected (I or Q) the offset calibration duration is divided by two and no gain calibration between the two channels is necessary.

The Control Wait setting gives the possibility to optimize the duration of the calibration depending on the clock frequency.

The calibration phase is necessary when using the AT84AD001B and AT84AD004B in interlace mode, where one analog input is sampled at both ADC cores on the common input clock's rising and falling edges. This operation is equivalent to converting the analog signal at twice the clock frequency.

It is important to draw your attention on the fact that the calibration is sensible to the ADC noise environment. It might be necessary to check the results of the calibration and eventually launch a new calibration phase if the results are not satisfying.

4.1 Wire Serial Interface

Atmel ATmega128L AVR® can be used to drive the 3-wire serial interface of e2v AT84AD001B and AT84AD004B ADCs.

In this first section, a simple configuration for the interfacing of the AVR with the ADC is provided.

Note: All the information contained in this document concerning the AVR complies with the version available at the creation date of the document. They should be checked versus the current version available before design.

4.2 AT84AD001B and AT84AD004B ADC 3-Wire Serial interface

Four signals of the AT84AD001B and AT84AD004B ADCs can be driven via the ATmega128L AVR:

- The SMODE signal (pin P15 of the TBGA192 packaged device): used in the ADC to activate the 3-wire serial interface
- The SCLK signal (pin N15 of the TBGA192 packaged device): input clock for the serial interface
- The SDATA signal (pin N16 of the TBGA192 packaged device): input data for the serial interface
- The SLDN signal (pin P16 of the TBGA192 packaged device): Beginning and End of register line for the serial interface

The 3-wire serial interface of the ADC only accepts 2.5V CMOS digital signals while Atmel ATmega128L should be supplied with V_{CC} = 2.7 to 5V. It was therefore necessary to add a buffer and line driver with 2.5-3.3V tolerant I/Os used as a translator in this mixed 2.5V and 3.3V environment.

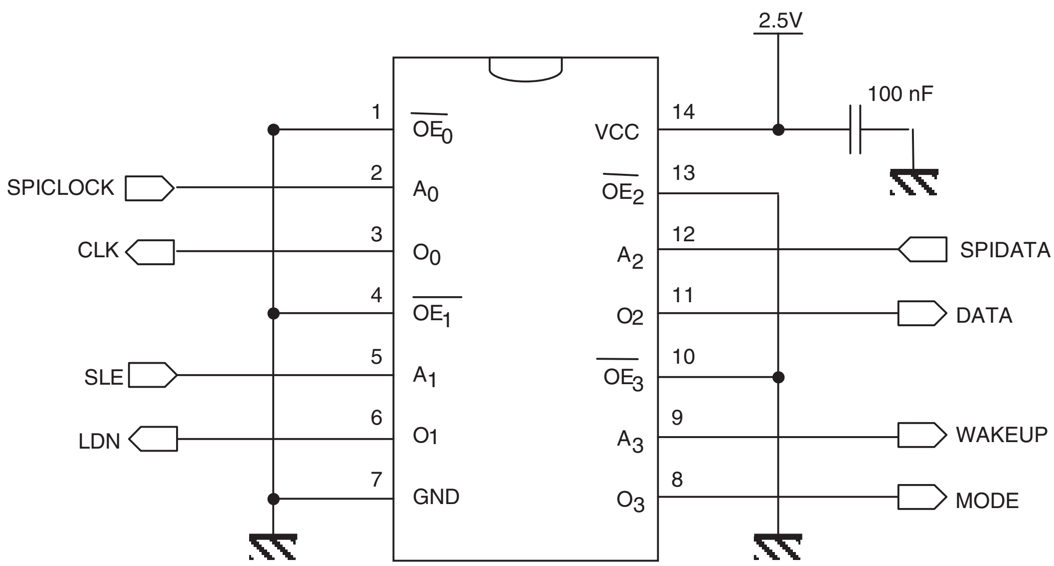
Because only four signals of the ADC have to be managed via the AVR, a quad buffer is sufficient to translate the four signals from the AVR (WAKEUP, SPICLOCK, SPIDATA, SLE) to the SMODE, SCLK, SDATA and SLDN signals (2.5V) of the ADC.

Possible devices allowing to perform the translation between the 3.3V of the AVR and the 2.5V required by the ADC are the 74LCX125 and 74LCX126 low voltage quad buffer and line with 5V tolerant Inputs/outputs or 74LCX244 low voltage octal buffer and line with 5V tolerant Inputs/outputs from any digital buffer manufacturers.

The 74LCX125 and 74LCX126 devices have the advantage of using only four inputs but their drawback is that you will not be able to have all four inputs on the same side of the device (easier layout).

The following figures illustrate the possible application diagrams for the 74LCX125 and 74LCX244 low voltage buffers with 5V tolerant I/Os.

Figure 4-1. Application Diagram Using the 74LCX125 Buffers

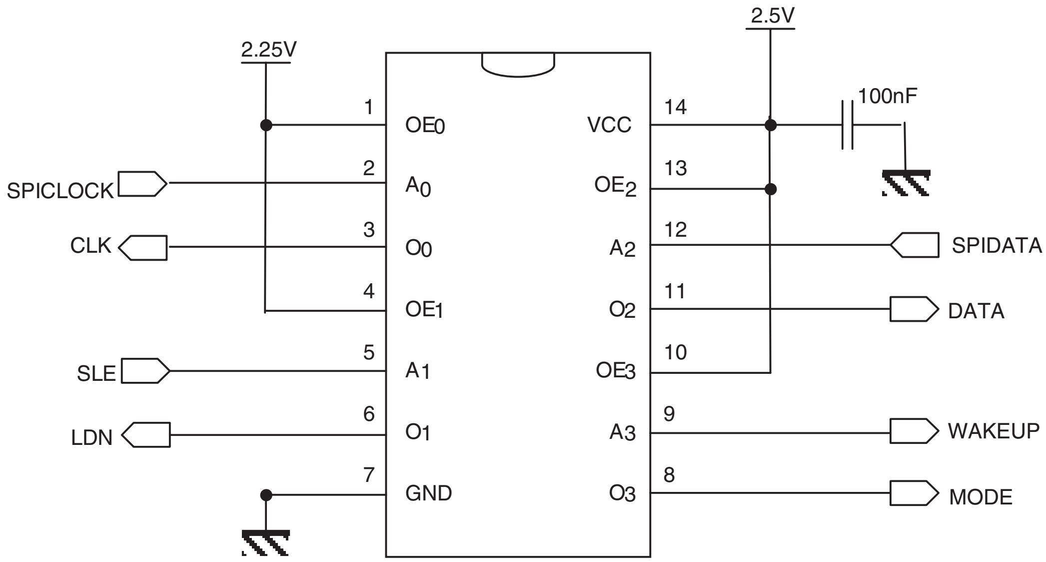


The truth table of the 74LCX125 device is shown in Figure 4-1.

Table 4-1. 74LCX125 Truth Table

Inputs		Outputs
OE_n	A_n	O_n
L	L	L
L	H	H
H	Z	Z

Figure 4-2. Application Diagram Using the 74LCX126 Buffers

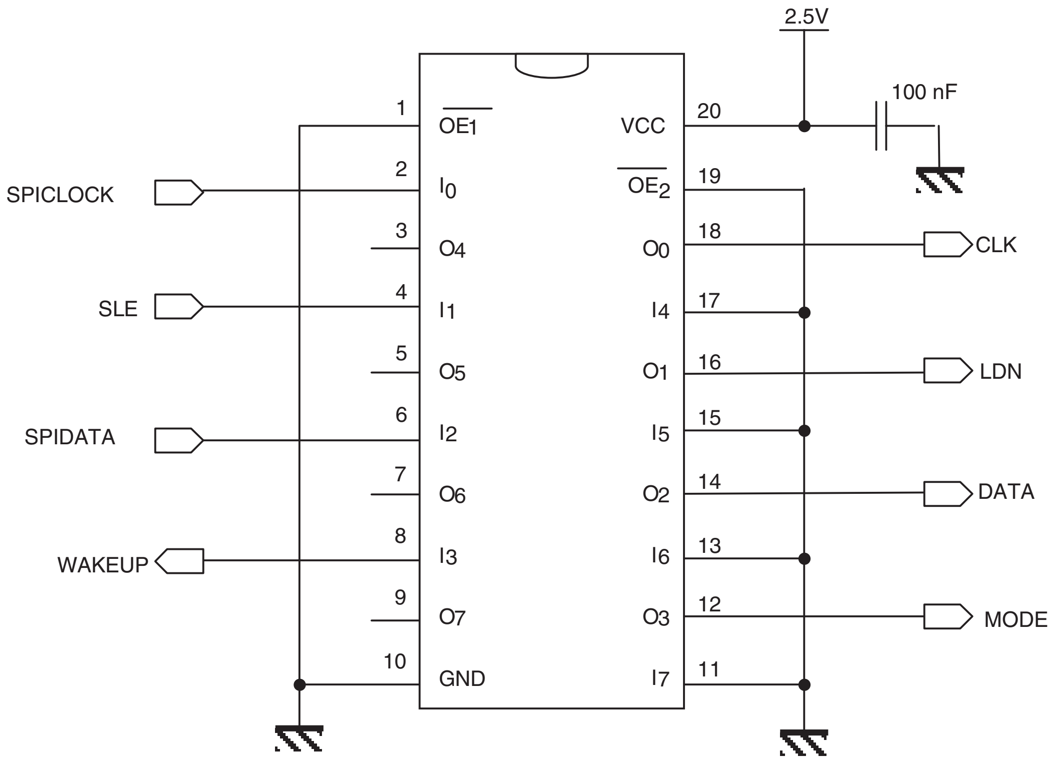


The truth table of the 74LCX126 device is shown in Table 4-2

Table 4-2. 74LCX126 Truth Table

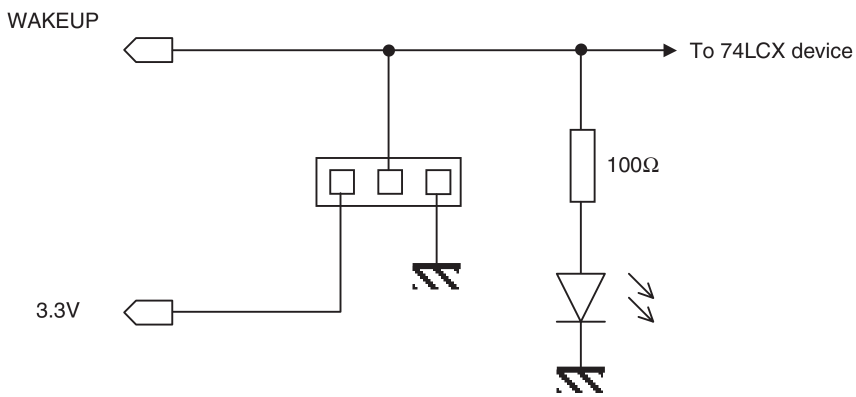
Inputs		Outputs
OEn	A_n	O_n
L	L	L
H	H	H
H	Z	Z

Figure 4-3. Application Diagram Using the 74LCX244 Buffers



Note:
1. It is highly recommended to connect the unused inputs of the octal buffer to ground (directly to ground or via a 0Ω resistor in case you might need to access the signals in the future) so that the buffers will never toggle and consequently dissipate power while the buffers are not used.
2. It might be useful to connect the OE signals to ground (74LCX125 and 74LCX244 devices) or to 2.25V (74LCX126) via a 0Ω resistor in case you might need to change the signal level in the application.
3. The WAKEUP signal is considered here as an input for both the 74LCX device and the AVR. When connected to 2.25V, the serial interface is made active for the ADC. When connected to ground, the serial interface of the ADC is disabled. In the case of a demonstrator design, it might be useful to connect this signal to a LED to indicate that the 3-wire serial interface has been activated (LED lit) and to a push button (between ground and 3.3V), as illustrated in Figure 4-4 on page 11

Figure 4-4. Management of the WAKEUP Signal (Manual for a Demonstrator Design for Example)



The truth table of the 74LCX244 device is shown in Figure 4-3

Table 4-3. 74LCX244 Truth Table

Inputs		**Outputs (O_0, O_1, O_2, O_3)**
OE1	In	
L	L	L
L	H	H
H	X	Z
inputs		**Outputs (O_4, O_5, O_6, O_7)**
OE2	In	
L	L	L
L	H	H
H	X	Z

4.3 ATmega128L 8-bit Microcontroller In-system Programmable Flash

On the AVR side, 8 bi-directional I/O ports are provided but only 4 bits of one port will be used for the interface between the 74LCX device and the AVR (for the WAKEUP, SPICLOCK, SPIDATA and SLE signals).

Because Port B provides the pins for the SPI channel, this is the port chosen for the four previously mentioned signals:

- SPICLOCK: PB1 (SCK = SPI bus serial clock)
- SPIDATA: PB2 (MOSI = SPI bus Master Output/Slave Input)
- SLE: PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0)
- WAKEUP: PB5 (OC1A = Output Compare and PWM Output A for Timer/Counter1)

The other pins PB0 ($\overline{SS}$), PB6 (OC1B) and PB7 (OC2/OC1C) can be left floating (open).

Pin PB3 (MISO = SPI Bus Master Input/Slave Output) needs to be pulled up to 3.3V via a 1 kΩ resistor in order to be forced to a high level and not left open.

Pins SPICLOCK = PB1 and SPIDATA = PB2 need to be pulled down to ground via a 10 kΩ resistor to be forced to low level (inhibition of the SPI during reset of the microcontroller).

Pin SLE = PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0) needs to be pulled up to 3.3V via a 3.3 kΩ (or 1 kΩ if the power consumption is not critical) resistor in order to protect the line during reset of the microcontroller (in which phase the signal becomes an input).

Ports A and C of the AVR can be left floating (open) but have to be internally configured with pull-ups.

For Port D, pins PD7, PD6, PD5 and PD4 can be left unused (open) but have to be internally configured with pull-ups. Pins PD3, PD2, PD1 and PD0 have to be pulled up in order to inhibit external interrupts.

For port E, pins PE3 and PE2 can be left unused (open) but have to be internally configured with pull-ups. Pins PE7, PE6, PE5 and PE4 have to be pulled up to 3.3V via a 3.3 kΩ (or 1 kΩ if the power consumption is not critical) resistor in order to inhibit external interrupts.

PE1 and PE0 can be used as the Programming Data Output (TX) and Input (RX) to be connected to the TX and TX of the system (in the case of the AT84AD001-EB and AT84AD004-EB evaluation boards, these signals are sent to the PC via an RS232 port).

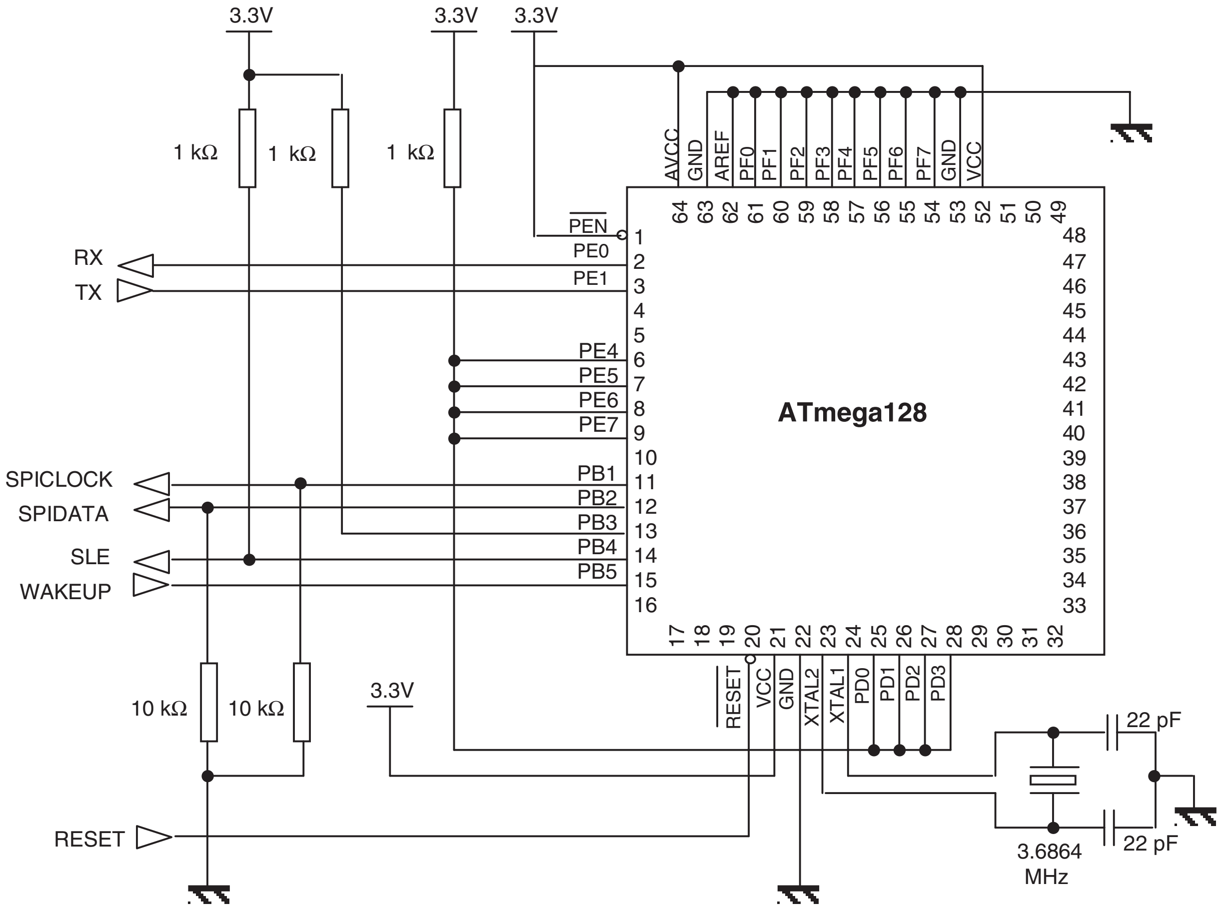
All the pins of Port F must be connected to ground so that they are in a known fixed state (no internal pull-down available for these pins). All pins of Port G can be left floating (open). Finally, the five remaining signal pins should be connected as follows:

- $\overline{PEN}$ = programming enable pin for the SPI serial programming mode, to be connected to VCC = 3.3V to activate the SPI programming mode
- $\overline{RESET}$ = Master reset of the AVR, to be connected to a microcontroller supervisory circuit (for example and for information only: MCP809 from Microchip™, one possible configuration is given in the Section 4.4)
- XTAL1 and XTAL2: input and output to/from the inverting Oscillator amplifier
- AREF = analog reference for the A/D internal converter

Finally, V_{CC} and AV_{CC} have to be connected to a 3.3V source and GND, to ground.

This gives the following configuration (AVR only):

Figure 4-5. ATmega128L Application Diagram (for Use with e2v AT84AD001B and AT84AD004B ADCs)



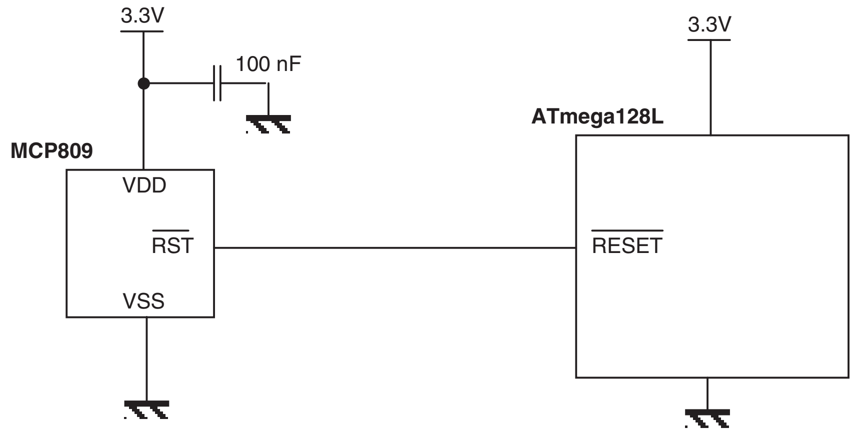
Note: Only the connected pins are shown (the unused pins are left open).

The reset of the ATmega128L AVR can be controlled thanks to a *voltage supervisory circuit* comparable to the MCP809 device from Microchip™ (for information only). Such a device allows you to keep the microcontroller in reset until the system voltage has reached its final level. It also ensures that the microcontroller will be reset whenever a power drop occurs.

Any voltage supervisory circuit compliant with VCC = 3.3V and with a reset pulse longer than 50 ns minimum width (active low) would work.

Here the supervisory device from Microchip reset voltage level is set to 3.0V with a pulse of 350 ms.

Figure 4-6. Typical Application Diagram for the Circuit



4.4 Programming of Atmel ATmega128L AVR

Atmel ATmega128L AVR can be programmed thanks to the AVR ISP (In-System Programmer) tool using AVR Studio®, e2v's Integrated Development Environment (IDE) for code writing and debugging. The programming software can be controlled from both Windows® environment and a DOS command-line interface.

For more information on the AVR Studio® programming software, please refer to e2v web site.

The programming of the AVR requires the use of a 6-pin or 10-pin ISP connector.

In our case, an HE10 6-pin connector is chosen:

- Pin 1 = PDO, AVR Programming Data Out
- Pin 2 = AVR Target application card power supply (= 3.3V)
- Pin 3 = SCK, AVR programming clock
- Pin 4 = PDI, AVR programming Data In
- Pin 5 = RST_ISP, AVR programming Reset
- Pin 6 = ground

Note: 1. The ISP card power supply comes from the AVR card (3.3V). There is no need for an additional power supply.
2. The mode used to program the AVR is a serial mode.

The RST_ISP signal is used to manage the AVR mode: programming mode or SPI mode.

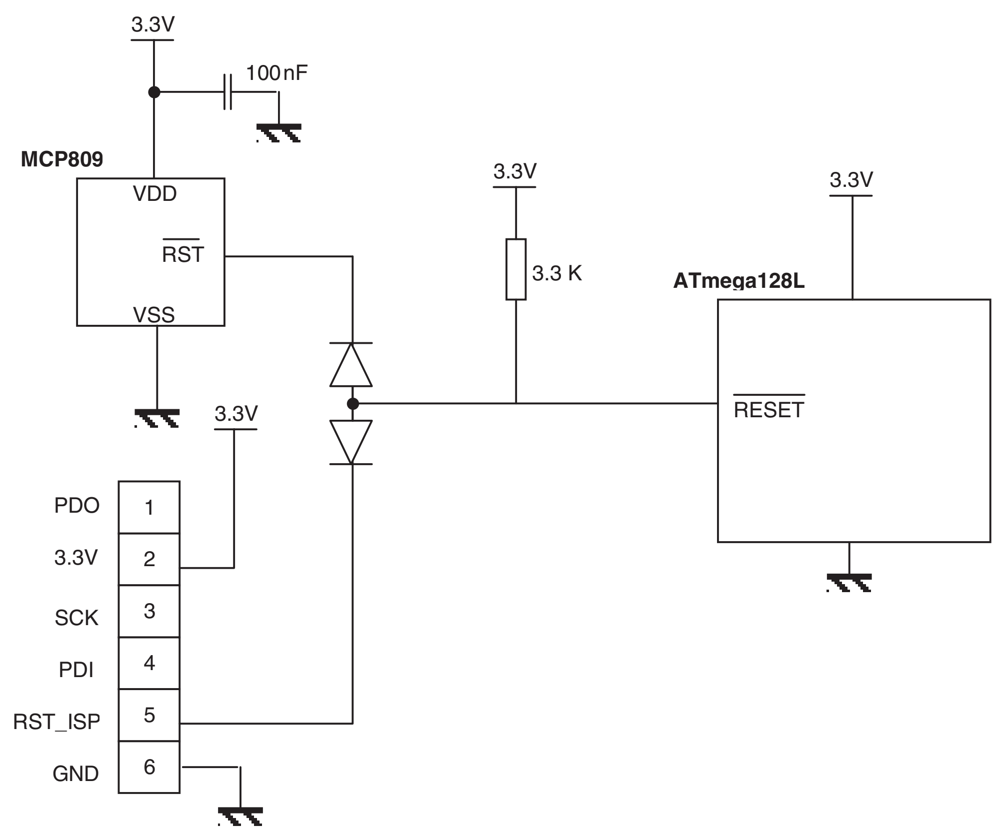
This signal is sent to the $\overline{\text{RESET}}$ of the AVR so that:

- When RST_ISP = 0, $\overline{\text{RESET}}$ = 0 and the AVR is in reset (ISP mode), PE0 is used as the Data In for the programming of the AVR, PE1 is the Data Out and PB1 is the programming clock
- When RST_ISP = 1, $\overline{\text{RESET}}$ = 1 and the AVR is in normal mode, PE0 = RX, PE1 = TX, PB1 = SPICLOCK

The three AVR signals mentioned previously (PE0, PE1 and PB1) thus have two functions, controlled by RST_ISP. Be careful when implementing these signals (series resistors on the SCK, PDO and PDI data might be needed to manage possible conflicts, see Section 5.

Similarly, the $\overline{\text{RESET}}$ signal has two possible sources: the signal generated by the microcontroller supervisory device and the RST_ISP signal from the ISP. In order to manage this signal and in case the microcontroller supervisory device is not with open collector (as for the MCP809 device), two head-to-tail diodes are required, as illustrated in Figure 3-3 on page 5. The line going to the $\overline{\text{RESET}}$ signal of the AVR is then in open-collector and a pull-p resistor (3.3 kΩ) to 3.3V is required.

Figure 4-7. Typical Application Diagram for the Circuit with the ISP Connector

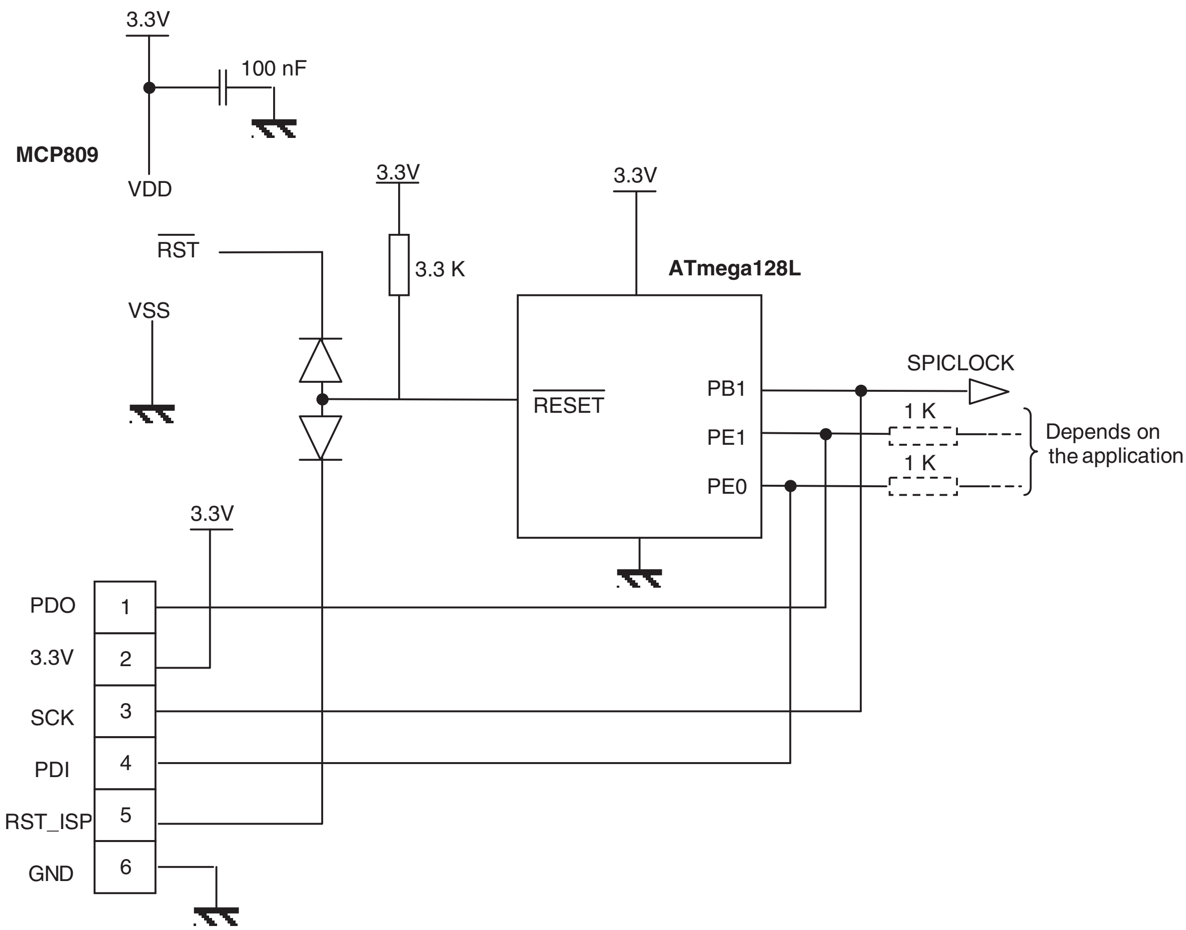


A basic diagram illustrating the interface between the ISP connector and the AVR is depicted in Figure 4-8 on page 16.

In this general case, PE1 and PE0 interconnections are left to the user's responsibility. In case of possible conflict on these signals (example PE1 could be driven by both PDO and another signal), it might be necessary to add a 1 kΩ resistor in series so that any voltage difference will be dissipated in this resistor.

No additional protection is required on the AVR PB1 signal there is no conflict between SCK and SPI-CLOCK. It is nevertheless recommended to set the ADC in standby mode or disable the 3-wire serial interface thanks to the MODE bit during programming of the AVR.

Figure 4-8. General Application Diagram for the ISP Connector and the AVR



In case the RX and TX signals are to be connected to a transceiver (RS232 connector to a PC for example), in order to multiplex the signals of the AVR (PE0, PE1 and PB1) between the ISP and the RX, TX and SPICLOCK signals, a low voltage buffer/line driver with 3-state outputs device can be used. The 74LVQ241 devices are well-suited for this application (clock driver and bus oriented transmitter or receiver).

The 74LVQ241 device has 8 inputs and 8 corresponding outputs and two three-state output enable inputs. These 2 3-state output enable inputs can be managed by the RST_ISP signal:

- When RST_ISP = 0, = OE2 = 0 and then O0 to O3 are low and O4 to O7 are in high impedance
- When RST_ISP = 1, = OE2 = 1 and then O0 to O3 are in high impedance and O4 to O7 are low

The truth table of the 74LVQ241 device is shown in Figure 4-4 on page 16.

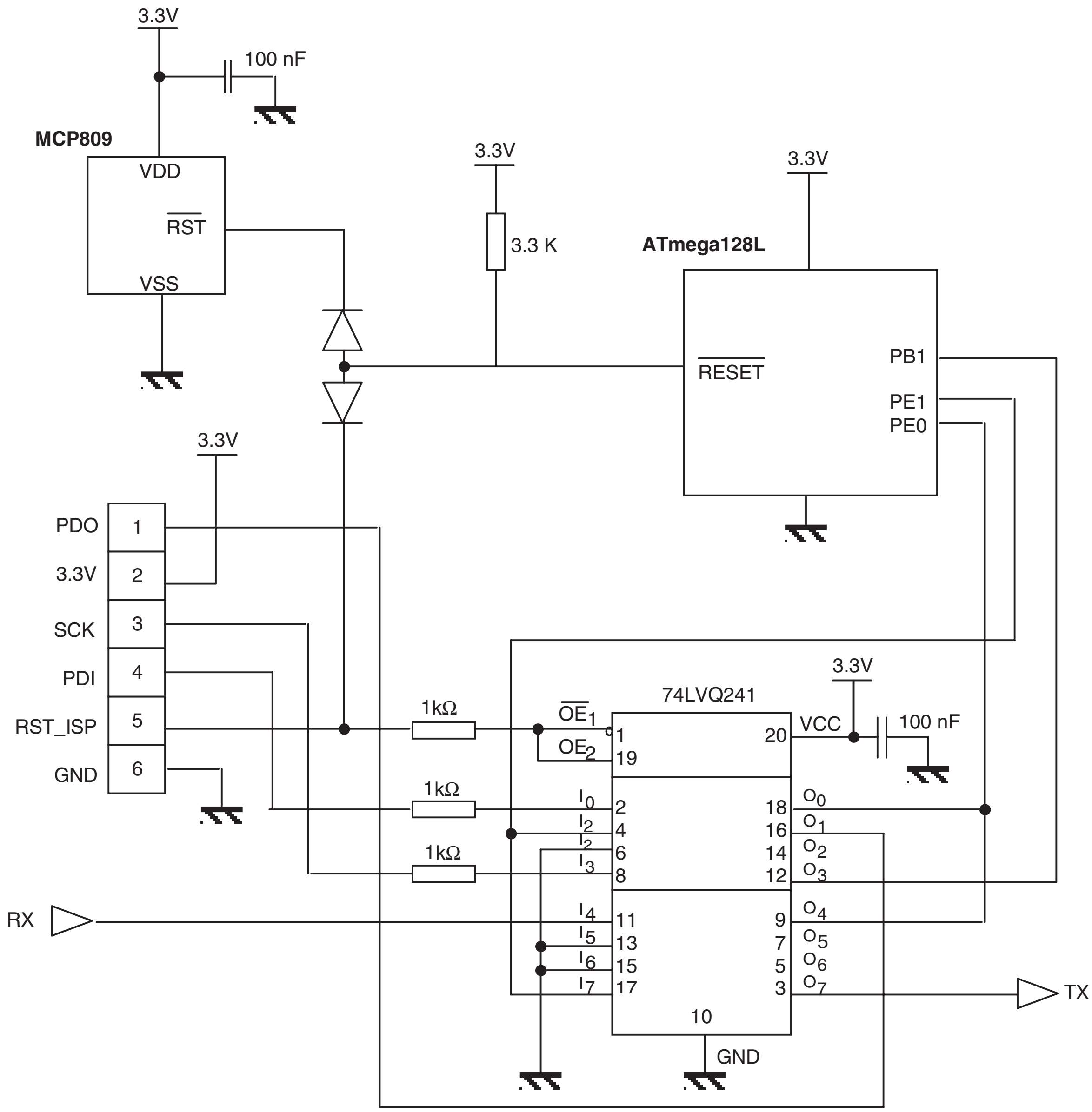
Table 4-4. Table 5.74LVQ241 Truth Table

Inputs		Outputs
OE1	In	(O_0, O_1, O_2, O_3)
L	L	L

Table 4-4. Table 5.74LVQ241 Truth Table

L	H	H
H	X	Z
inputs		**Outputs**
OE2	In	**(O_4, O_5, O_6, O_7)**
L	L	L
L	H	H
H	X	Z

Figure 4-9. Typical Application Diagram with the 74LVQ241



1. The unused inputs are connected to ground to prevent them from toggling.
2. and OE2 are connected together and to RST_ISP via a 1 kΩ resistor.
3. SCK, RST-ISP and PDI are connected to I3, and OE2 and I0 respectively via 1 kΩ resistors in order to manage the possible conflicts on the signals in case the connector is used to program several AVRs.
4. PE0 is connected to both O0 and O4, which are respectively the inputs corresponding to SCK and RX: PE0 will be either generated by SCK or RX depending on the mode.
5. PE1 is connected to both I1 and I7, which are respectively the outputs corresponding to PDO and TX: PE1 will either generate by PDO or TX depending on the mode.

The programming of the AVR itself as well as the connections of the RX and TX signals are not described in this application note as they depend on the final application.

For more information on the AT84AD001B and AT84AD004B ADCs, please contact the Broadband Data Conversion hotline at hotline-bdc@e2v.com. For more information on the AVR, please contact the AVR hotline at avr@atmel.com.

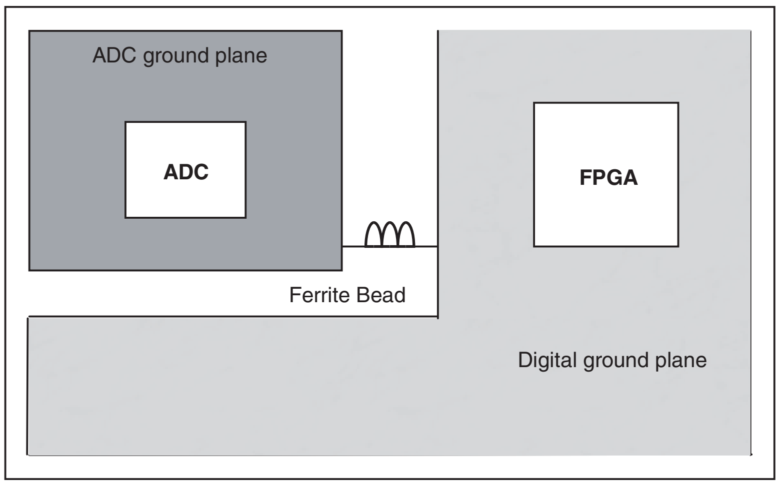
5. Grounding and Power Supplies

5.1 Ground Plane

It is recommended to separate the ground plane of the ADC (one common ground plane GND) and the system's ground plane (for example FPGA digital ground plane).

These two ground planes can be reunited by one point via a ferrite bead as illustrated in Figure 5-1.

Figure 5-1. Schematic View of the System Board Ground Plane (Example)



It is also recommended to plan to have one ground plane for each signal plane in the board layer stacking (example: Layer 1 = signal layer, layer 2 = ground layer, etc.).

5.2 Power Supply Planes

The ADC requires three power supplies:

- V_{CCA} = 3.3V analog
- V_{CCD} = 3.3V digital
- V_{CCO} = 2.25V (for the outputs and the 3-wire serial interface)

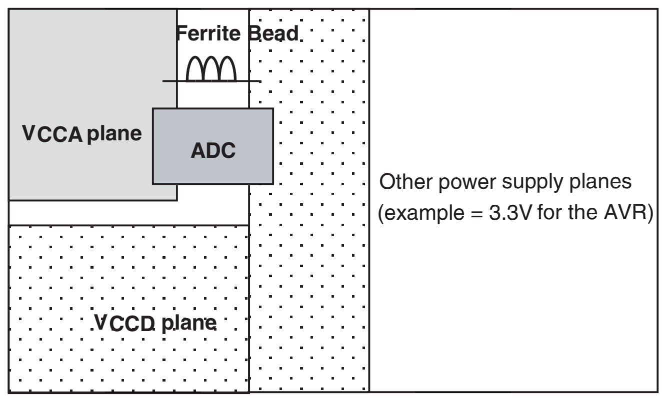
At least, three different power planes are required for the ADC.

It is recommended to place the power supplies layers in between two ground layers for better isolation.

You can use the same layer for both V_{CCA} and V_{CCD} power supplies however you should use separate planes as the V_{CCA} plane concerns only the analog part of the AT84AS001 device. The less extended the better it is.

On the other hand, it might be easier to use another layer for V_{CCO}.

Figure 5-2. Schematic View of V_{CCA} and V_{CCD} Planes



As concerns the power supplies decoupling and bypassing, each incoming power supply should be bypassed by a 22 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

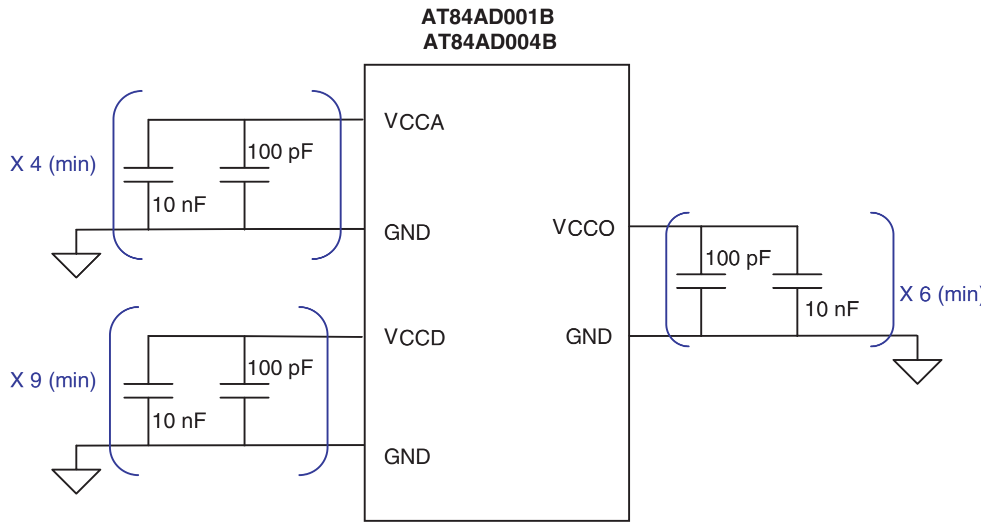
Each power supply should be decoupled as close as possible to the AT84AS001 device by 10 nF in parallel with 100 pF surface mount chip capacitors (the 100 pF capacitors should be mounted first).

To determine how many decoupling capacitor pairs are required, it is necessary to count how many groups of neighboring power supply pins attributed to the same value can be defined. Each group should then be decoupled by at least one pair of 10 nF in parallel with 100 pF capacitors.

The minimum required pairs of capacitors by power supply type are:

- Four for V_{CCA}
- Nine for V_{CCD}
- Six for V_{CCO}

Figure 5-3. AT84AD001B and AT84AD004B Power Supply Decoupling Scheme



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