High-speed ADC Input Clock Issues

Application Note

1. Introduction

The e2v converters family addresses the high-speed market in the field of ADCs as well as DACs, with frequencies operating in the GHz range. Such high-speed devices require high-speed clock signals, which are usually subject to noise and which users are not used to deal with. As a matter of fact, the clock signal integrity is one of the main factor to be taken into account for proper operation of an ADC.

High-speed ADCs require a low phase noise clock (namely a low jitter clock) in order to limit the dynamic performance degradation caused by noise on the clock. Even though many manufacturers offer crystal oscillators with the right jitter characteristics, only a few are able to generate clocks in the GHz range.

These two issues are addressed in this paper, which intends to help the user understand the jitter phenomenon and design a proper clock with the right performance.

2. Input Clock Performance

e2v Broadband Data Conversion products are high-speed products operating in the GHz range. They consequently require very high-speed signal management, which refers to two main parameters:

- The signal integrity, involving the phase noise
- The signal frequency itself

The phase noise or jitter is defined in the next section, where the stress is laid on what jitter is, what it is due to and finally what impact it has on an A to D converter dynamic performances.

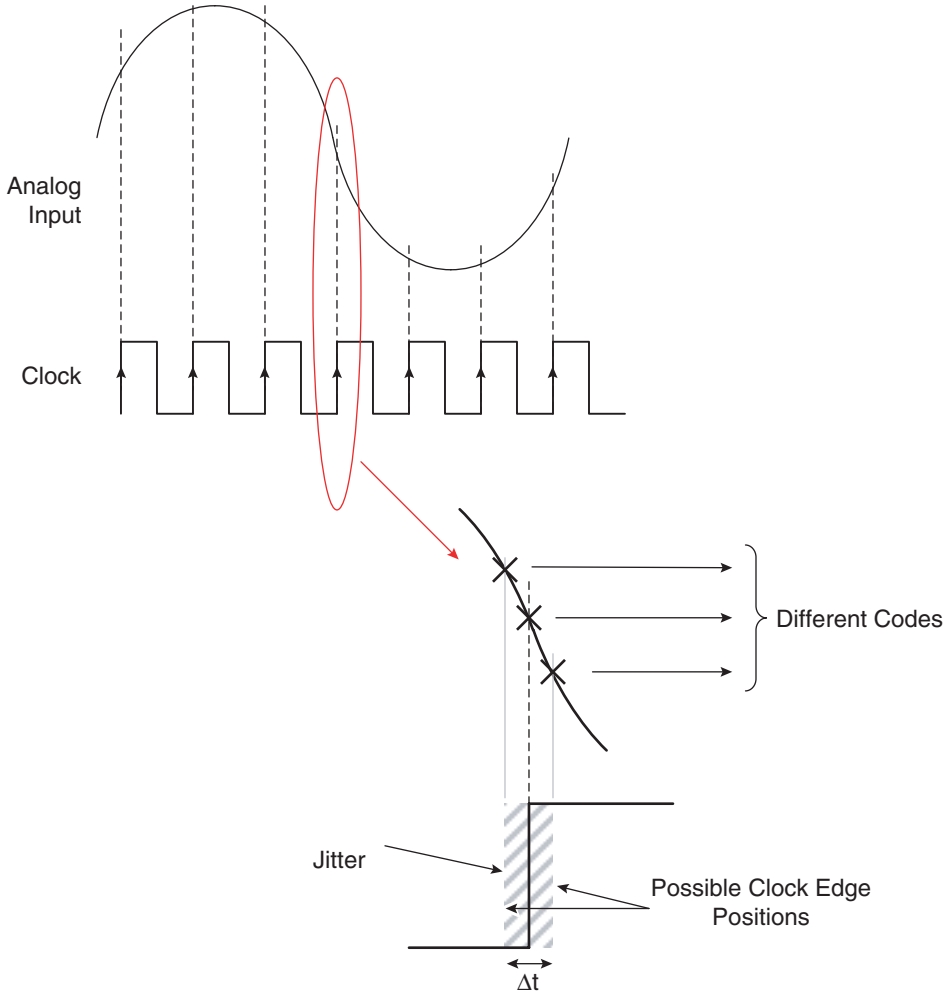
A second half of this paragraph is dedicated to the comparison between differential and single-ended signaling used for high-speed signals.

2.1 Clock Jitter

2.1.1 What is Clock Jitter?

We usually define the clock jitter for the case of an ADC, as the sample to sample variation in aperture delay of the clock signal. It is the *uncertainty we have on the instant of sampling*, which causes voltage errors at the sampling point. This is clearly illustrated in the following figure:

Figure 2-1. Effect of Clock Jitter on the Instant of Sampling



As illustrated previously, jitter can be expressed in absolute time. In this case, what is stressed is the magnitude of the jitter and it is usually given in picoseconds, which is the appropriate order of magnitude for jitter.

It might also be expressed in degrees, where one cycle of clock corresponds to 360°, but the normalized definition of jitter is in *unit intervals*, where one single unit interval corresponds to a clock period. This latter definition gives the jitter as a fraction of one clock period.

In our case, we usually give the jitter in absolute time.

Finally, before getting into the causes of jitter, it can be highlighted that three types of jitter can be observed:

- Regular and periodic jitter
- Random jitter
- Signal-dependent jitter

Each type of jitter has a different cause and this will be developed in the following section.

2.1.2 What Causes Jitter?

Jitter can be defined as a time-based error and as such, is explained as the result of varying time delays in the signal path and waveform distortion due to poor impedance matching in the signal path. More technically speaking, the notion of jitter is connected to the phase noise, due to Frequency Modulation (FM), Amplitude Modulation (AM) and Phase Modulation (PM).

However, the phase noise is not the only cause of jitter. As a matter of fact, thermal noise and spurious components have a non-negligible contribution to jitter.

Jitter is caused by noise but what can be interesting to understand in the phenomenon of jitter is to explore how noise can contribute to jitter.

2.1.2.1 Signal Generator Phase Noise Profile

The stress can be first laid on the characteristic SSB phase noise for standard signal generators (example: ESG-AP and ESG-DP series from Agilent).

The following figures illustrate these characteristics for carrier frequencies of 100 MHz and 1 GHz for standard instrument and then for carrier frequencies of 900 MHz and 1.8 GHz with I/Q modulation ON respectively.

Figure 2-2. SSB Phase Noise, Fc = 100 MHz (ESG-AP Series)

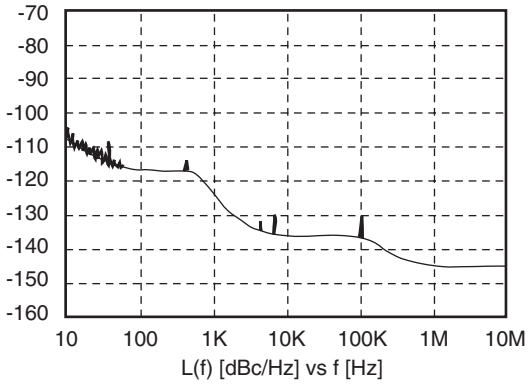


Figure 2-3. SSB Phase Noise, Fc = 1 GHz (ESG-AP Series)

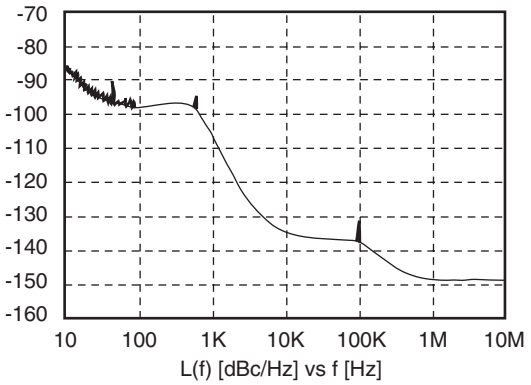


Figure 2-4. SSB Phase Noise, Fc = 900 MHz, I/Q Modulation ON (ESG-AP Series)

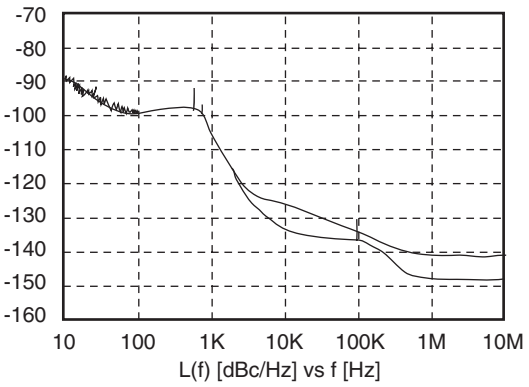
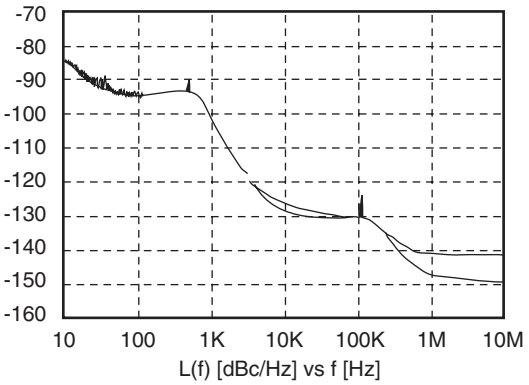


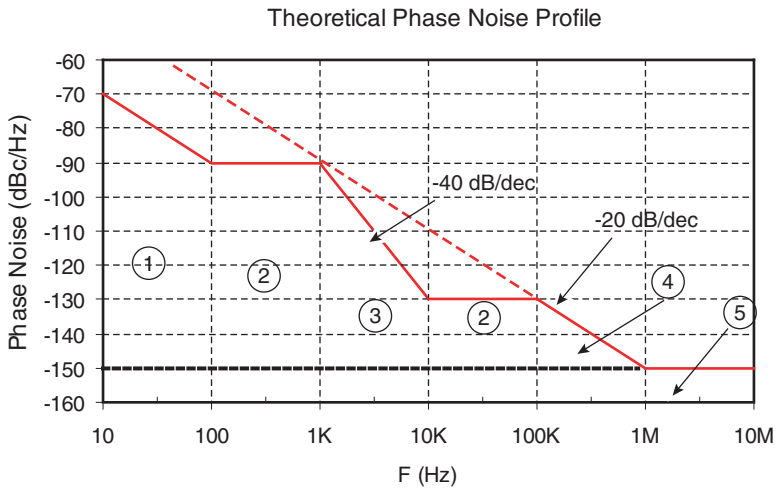
Figure 2-5. SSB Phase Noise, Fc = 1.8GHz, I/Q Modulation ON (ESG-AP Series)



Note: Figure 2-4 on page 4 illustrates the fact that the modulation impacts the phase noise. When the signal generator is used with modulation, the phase noise characteristics are worse than without modulation.

These characteristics are real ones, measured in practice thanks to spectrum analyzers. The theoretical characteristics can however be depicted as in the following figure:

Figure 2-6. Theoretical Signal Generator Phase Noise Profile

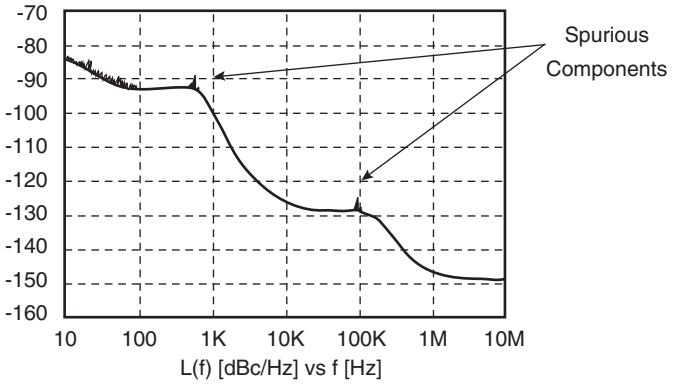


At first sight, the SSB phase noise profile of standard signal generators can be divided into two different parts:

- A part from 10 to 100Hz (1)
- A part from 100Hz to 1 kHz and from 10 kHz to 100 kHz (2), due to the Phase Locked Loop divisors
- A 1/F² part from 1 kHz to 10 kHz (3), which corresponds to angle modulation by non-uniform 1/F noise (-40 dB/dec)
- A 1/F part from 100 kHz to 1 MHz (4), which corresponds to the close-in phase noise (20 dBc/Hz)
- A *Flat* segment from 1 Mhz to higher frequencies (5), corresponding to the thermal noise.

To these theoretical segments (close-In phase noise and noise floor), the spurious components should be added: these are the spurious peaks, which can be seen on the real characteristics of the generators:

Figure 2-7. SSB Phase Noise Characteristic, Fc = 2 GHz (ESG-AP Series)



The spurious components contribution to jitter is however negligible with respect to the two other contributions (phase noise and noise floor).

Each contribution to jitter will be now dealt with in the following sections of this document.

Note: Except the noise floor segment, the rest of the approximated phase noise characteristic of standard generators could be simplified to a -20 dBc/Hz segment from 10Hz to 1 MHz. The error induced by such an approximation would then be negligible compared to the contribution of all 1 to 4 segments.

2.1.2.2 Spurious Components

The Spurious components are closely linked to the characteristics of the generator used. It mainly depends on the phase noise characteristic of the generator at an offset frequency fm. Each spurious component has to be taken into account and contributes to the total spurious components.

Each spurious component contribution is calculated as follows:

$$\sigma^2_{spurious} = \frac{8}{\omega_0^2} L(f_m) \times sin^2(\Pi \times \tau \times f_m)$$

where:

$\sigma^2_{spurious}$= variance of spurious components RMS (in absolute time square = s^2)

$\omega_0 = 2\Pi f_0$ = pulsation (in rad/s) corresponding to the beat frequency of the oscillator (or generator)

f_0 = oscillator center frequency (in Hz)

fm = offset Frequency from center frequency of the oscillator (in Hz)

$\tau = 1/2f_0$ = Half period (in s)

L(f) = phase noise at the offset frequency f (in dBc/Hz)

The total spurious components contribution to jitter is therefore:

$$\sigma^2_{spurious_{(total)}} = \sum_1^m \sigma^2_{spurious(i)} = \sum_1^m \frac{8}{\omega_0^2} L(f_m) \times sin^2(\Pi \times \tau \times f_m)$$

sum of the contribution of each spurious component.

As this can be seen clearly on the real characteristics of the generators (see Figure 2-2 on page 3 to Figure 2-5 on page 4 and Figure 2-7 on page 5), the spurious components are not the main contributors to jitter and can well be neglected in most cases.

For the ESG-AP generator for Fc = 1 GHz (Figure 2-3 on page 3), if we only take the main spurious component of the characteristic at 100 kHz offset from carrier, the contribution to jitter gives:

$$\sigma^2_{spurious} = \frac{8}{(2\Pi \times 10^9)^2} \times 10^{-130/20} \times sin^2(\Pi \times 0,5 \bullet 10^{-9} \times 100 \bullet 10^3) = 1,5 \times 10^{-21} ps$$

2.1.2.3 *Phase Noise*

This noise is in fact the ratio of noise power given at a given offset frequency to the max. power level of the spectrum (corresponding to the central frequency of the generator). The calculation of the phase noise does not include the noise floor (described hereafter).

In general, this ratio is normalized for a 1Hz band, which explains why it is given in dBc/Hz (see Figure 2-6 on page 4).

The phase noise can be approximated by a 1/F curve with F, the corner offset frequency. This gives a characteristic with a -20 dBc/Hz slope , as illustrated in Figure 2-6 on page 4. In this area, the phase noise has the following expression [1]:

$$\sigma_{phaseNoise} = \frac{f}{f_0^{1,5}} \times 10^{L(f))/20}$$

where:

f = offset frequency from carrier (central frequency of generator)

f_0 = oscillator Center frequency

L(f) = phase noise at the offset frequency f (in dBc/Hz)

The L(f) term is given by the generator phase noise characteristic.

In the case of the ESG-AP generator for Fc = 1 GHz (Figure 2-3 on page 3), the phase noise can be approximated to:

$$\sigma_{phaseNoise} = \frac{f}{f_0^{1,5}} \times 10^{L(f))/20} = \frac{100 \bullet 10^3}{(10^9)^{1,5}} \times 10^{-135/20} = 0,0006 ps$$

with a phase noise of -135 dBc at F = 100 kHz offset.

2.1.2.4 *Thermal Noise (Noise Floor)*

We usually assume at first order that the thermal noise is a white gaussian noise with a finite bandwidth, generally defined with a cutoff frequency of twice the operating frequency.

The noise floor is generally given in the literature as:

$$\sigma^2_{thermal} = \frac{8}{\omega_0^2}\int_0^{\infty} L(f) \times sin^2(\Pi \times \tau \times f) df$$

where:

$\sigma^2_{thermal}$ = Variance of spurious components RMS (in absolute time square = s^2)

$\omega_0 = 2\Pi f_0$ = Pulsation (in rad/s) corresponding to the beat frequency of the oscillator (or generator)

f_0 = oscillator center frequency (in Hz)

fm = offset Frequency from center frequency of the oscillator (in Hz)

$\tau = 1/2f_0$ = half period (in s)

L(f) = phase noise at the offset frequency f (in dBc/Hz)

Assuming that the noise floor is constant, L(f) = L, because the noise floor is even for offset frequencies from DC to f_0, the previous equation becomes (after reduction):

$$\sigma_{thermal} = \frac{2\sqrt{L \times f_0}}{\omega_0}$$

If we take the ESG-AP generator characteristic given for Fc = 1 GHz (Figure 2-3 on page 3), the noise floor is approximately -147 dBc.

The resulting edge-to-edge timing jitter due to the noise floor is then:

$$\sigma_{thermal} = \frac{2\sqrt{L \times f_0}}{\omega_0} = \frac{2\sqrt{10^{-147/10}(10^9)}}{2\pi 10^9} = 0,450ps$$

2.1.2.5 *Total Jitter*

The Total jitter is given by the following formula:

$$\sigma_{total} = \sqrt{\sigma^2_{phaseNoise} + \sigma^2_{thermal} + \sum \sigma^2_{spurious}}$$

It is the quadratic sum of the thermal noise, phase noise and spurious components noise.

In our example, the total edge-to-edge jitter is then:

$$\sigma_{total} = \left(\sqrt{(0,0006ps)^2 + (0,450ps)^2 + (1,5 \times 10^{-21}ps)^2} \approx 0,450ps\right)$$

And therefore, we can conclude (true in most cases):

$$\sigma_{total} \approx \sigma_{thermal}$$

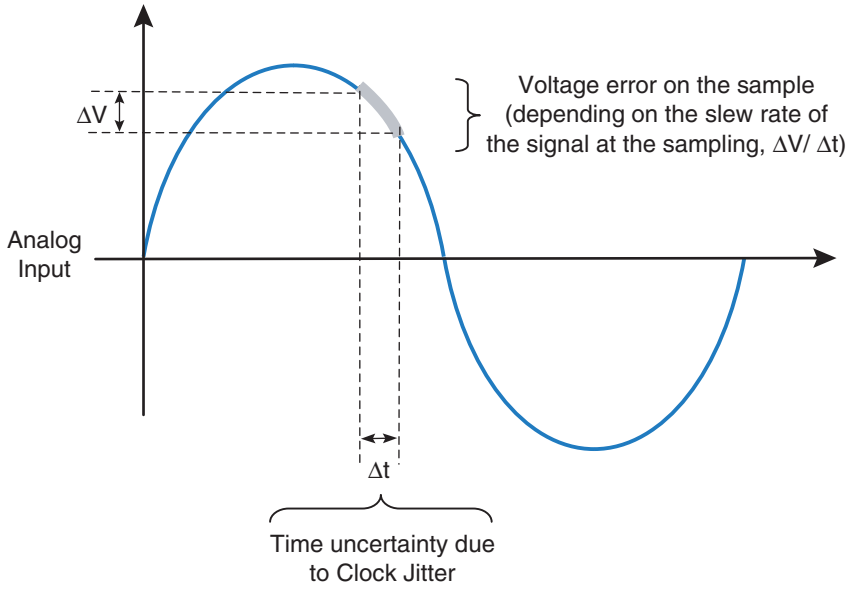
At high frequencies, the noise floor dominates the other contributors to jitter and is directly linked to the source used.

The following section illustrates how the imperfections of the source can distort the performances of a high-speed ADC, not due to the ADC itself but mainly to the source itself.

2.1.3 How Does the Clock Jitter Impact the ADC Dynamic Performances?

As explained previously, the clock jitter for an ADC affects the instant of sampling of the ADC with respect to an ideal instant of sampling. The uncertainty on the instant of sampling results in a false acquisition of the analog signal, as shown below:

Figure 2-8. Time Jitter Impact on Noise

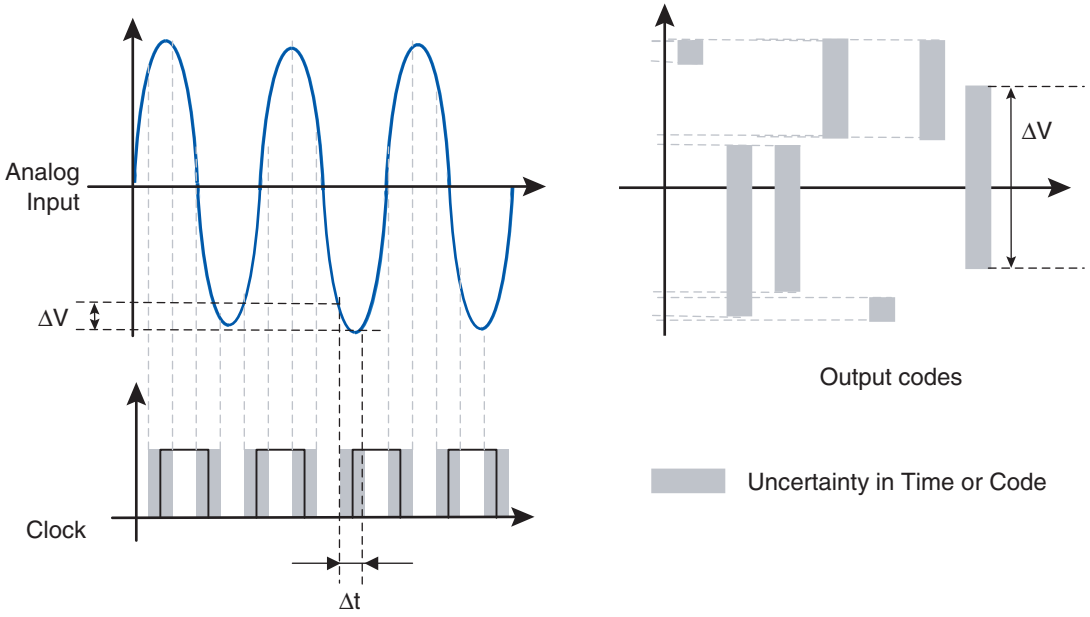


The impact of the time jitter on the voltage errors is accentuated by the slew rate of the analog signal at the sampling point:

$$SlewRate = \frac{\Delta V}{\Delta t}$$

The following figure illustrate the magnitude of the phenomenon of jitter on voltage errors as a function of the slew rate:

Figure 2-9. Consequences of Time Jitter on the Output Codes of an ADC



The uncertainty on the output codes of the ADC, due to jitter, can be interpreted as noise or random distortion and as such, can be linked to the SNR performance of the ADC.

Consequently, jitter impacts directly the dynamic performances of the ADC via the SNR. As a matter of fact, the slew rate can be expressed as follows:

$$SlewRate = \frac{\Delta V}{\Delta t} = A\omega\cos(\omega t)$$

assuming that the analog signal is a sinusoid of amplitude A.

The maximum slew rate is obtained at the zero crossing, for which cos (ωt) = 1.

The equation then becomes

$$MaxSlewRate\big|_{t=0} = \frac{\Delta V}{\Delta t} = A\omega$$

Since

$$\frac{A}{\Delta V}$$

corresponds to the SNR and Dt to the rms value of the jitter, the relationship between the SNR performance of the ADC and the jitter is:

$$\frac{A}{\Delta V} = \frac{1}{\Delta t \times \omega}$$

which can also be expressed as

$$SNR_{max} = 20 \times Log\frac{1}{\omega \times \Delta t} = 20 \times Log\left(\frac{1}{2\pi F_{in} \times \Delta t}\right)$$

This is the contribution of the jitter on the SNR performance. The SNR is however also due to quantization noise, thermal noise and distortion. A more realistic equation for the SNR is then:

$$SNR = 20 \times Log\left(\frac{A}{\sqrt{(nq^2 + (n_{thermal})^2 + (n_{distortion})^2 + (n_{jitter})^2)}}\right)$$

With:

n_q = Quantization Noise

$$n_q = \frac{Q}{\sqrt{12}}$$

where

$$Q = \frac{FS}{2^N}$$

FS = analog signal full-scale and N, number of bits.

$$n_{thermal} = thermalnoise = \sqrt{(tnsd)^2 \times BW \times \frac{\pi}{2}}$$

with BW = input bandwidth and tnsd = Thermal Noise Spectral Density.

$$n_{distortion} = distortioncomponents = \frac{A}{10^{THD/20}}$$

with THD = Total Harmonic Distortion.

n_{jitter} = jitter noise energy = 2πFin Δt.

Consequently, the noise jitter contributes to the degradation of the SNR parameter of an ADC and has an equivalent contribution as the thermal noise, the quantization noise and the distortion.

Since the SNR can be directly linked to the SINAD (Signal to Noise and Distortion Ratio) performance and since the SINAD is itself correlated to the ENOB (Effective Number of Bits) performance of the ADC.

The ENOB is the parameter, which characterizes the effective resolution of the ADC and is the parameter which is looked for in instrumentation applications. However, in other applications as telecommunication applications or RADAR applications, the main parameter to take care of is the SFDR parameter, which gives an idea of the capability of the ADC to discriminate one spur from another, the closest to each other they may be.

The noise jitter on the ADC clock considerably affects the ADC dynamic performances and has to be taken care of in a system design.

However, as well as the clock jitter impacts the instant of sampling and thus results in voltage errors, the uncertainty on the analog input signal may also have similar consequences on the ADC dynamic performances.

Although the notion of jitter is usually only dedicated to digital signals, we may introduce the notion of analog signal jitter, which is a consequence of distortion and noise on the analog input signal of an ADC.

This issue is briefly dealt with in the appendix section.

2.2 High-speed Clock Signals

When dealing with high-speed clock signals some rules have to be followed carefully in order to optimize the clock efficiency, either at device or at system level.

At system level, the clock jitter is the main parameter to take care of and has already been dealt with in the previous section.

At device level, the choice is given between single-ended signals and differential architectures, and this does not apply only to the clock signals but also to any high-speed signal.

The choice between the one or the other clock input mode is discussed below:

For all our high-speed ADC and DAC family, the choice was made to have fully differential architectures from input to output in order to limit the influence of the variations of a signal to its reference (ground, common mode). Indeed, with a differential architecture, the perturbations on the true and false signals are the same and the signal is no more referenced to the ground, which may be subject to perturbations.

The possibility of using single-ended signals is however still provided but we usually recommend to use differential signals for the clock input especially in the high frequency range (above 1.5 GHz) for better performances.

3. Clock Generation

3.1 How to Design a Low Phase Noise High-speed Clock

As underlined in the previous sections, two factors are of great importance in the clock generation for high-speed systems such as high-speed ADCs or DACs:

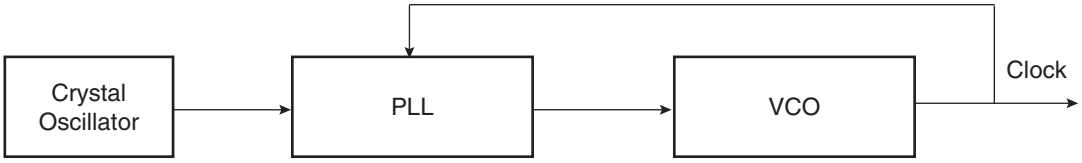
- The clock jitter
- The high frequency capability of the clock

For generating a clock for such systems, the first idea is to use a crystal oscillator, which fulfills the first criteria: many crystal oscillators with low phase noise are available on the market. However, nowadays crystal oscillators are not likely to achieve high speeds above a hundred MHz.

A trade-off between speed and jitter performance is then needed to implement a clock generating system able to output oscillating frequencies of the order of the GHz but also featuring a low jitter.

An example of clock generating system is depicted below:

Figure 3-1. Example of High-speed Low Jitter Clock Generating System



The clock generating system described above is constituted by three elements:

- A crystal oscillator
- A PLL (Phase Locked Loop)
- A VCO (Voltage-controlled Oscillator)

3.2 Description of the PLL-based Clock

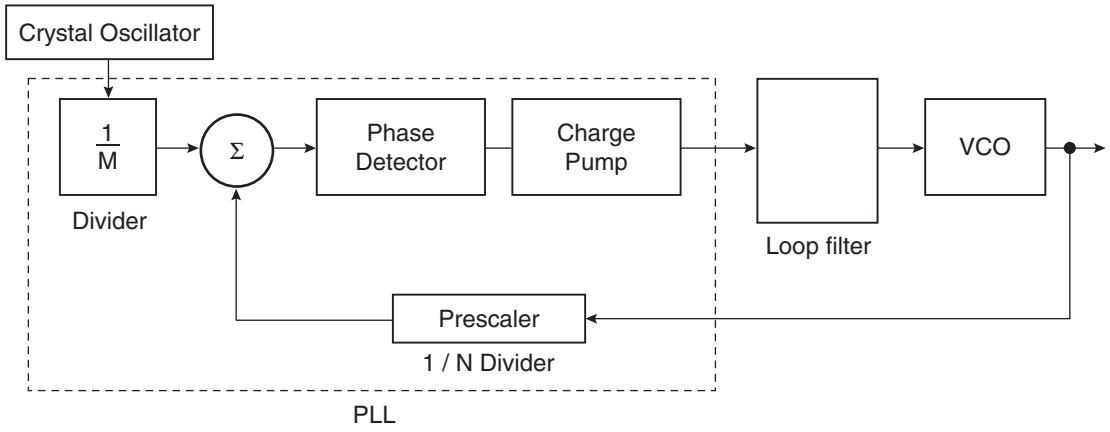
The VCO provides the oscillator frequency (the state-of-the-art in VCOs enables us nowadays to find VCOs providing frequencies of 1 GHz, 2 GHz, and even above).

Because the VCO is subject to inherent frequency drifts, a PLL is needed to lock the VCO output to the desired frequency. It works by comparing the VCO output frequency to a crystal oscillator.

Since the crystal oscillator is not able to provide the oscillating frequency required by the system, it seems obvious that some frequency divisions have to be performed to match the VCO oscillator frequency to the crystal oscillator frequency. In fact, the PLL divides the VCO frequency as well as the crystal frequency so that the resulting frequency at each end is the same except a possible offset. By comparing the two frequencies, the PLL then adjusts its voltage output, which controls the VCO. The VCO frequency then changes accordingly in order to match the crystal oscillator frequency.

The following figure shows in more details how the PLL performs the comparison between the crystal oscillator frequency and the VCO output frequency.

Figure 3-2. Functional Description of a PLL

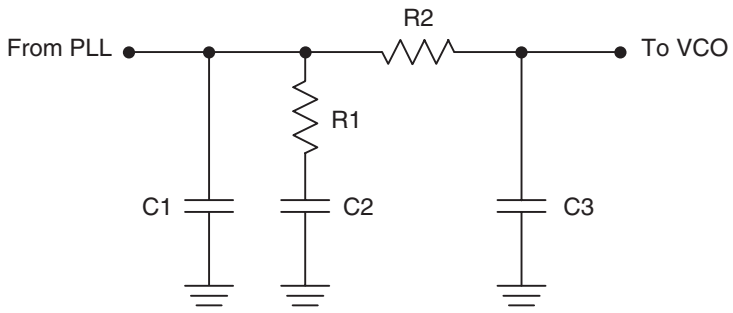


The output signal of the VCO is sent to the prescaler of the PLL, which divides the VCO signal by a factor N. At the same time, at the crystal oscillator's end, the PLL divides by a factor M the signal from the crystal oscillator and compares the two frequencies. A phase detector enables to see if there is a phase difference between the two signals. If there is one, the charge pump will either charge or discharge the loop filter capacitors to either increase or decrease (respectively) the voltage controlling the VCO.

3.2.1 Loop Filter Design

A typical loop filter schematic is given below:

Figure 3-3. Loop Filter Architecture



The C1, C2, C3 and R1, R2 parameters of the loop filter has to be determined according to:

- The charge pump current I_{CP}
- The VCO tuning Gain (or sensitivity) K_V
- The value N of the divider in the preschooler
- The damping factor ξ (= 0.707 typical)

3.2.1.1 Loop Filter Parameters Calculation

The following equations give the relations between the loop filter parameter values and the previous factors:

1. Determining the dividing ratios N and M for the PLL

At the output of the VCO we specify a required frequency of F_{OUT}.

The reference frequency provided by the crystal oscillator is referred to as F_{REF}.

The relation between the output frequency and the reference frequency is:

$F_{OUT} = N / M \times F_{REF}$

Where N is the dividing ratio for the VCO frequency and M is the dividing ratio for the crystal oscillator.

Moreover, N can be determined with the following equation:

$$N = \frac{VCOFrequency}{ChannelSpacing}$$

where the channel spacing is to be defined according to the application.

2. Calculate the natural frequency Fn

The natural frequency depends on:

- ts = desired time for the carrier to step to a new frequency
- ξ = the damping factor
- f_a = the frequency of the carrier, within the desired time ts, after a step or hop (1 kHz typical)
- f_{step} = maximum frequency change during a step or hop, from one frequency to another

The equation is:

$$fn = \frac{-1}{2\pi \times ts \times \xi} \times \ln\left(\frac{fa}{fstep}\right)$$

3. Determine capacitor C2

$$C2 = \frac{I_{CP} \times K_V}{N \times (2\pi \times fn)^2}$$

4. Determine capacitor C1

$$C1 = \frac{C2}{10}$$

5. Determine resistor R1

$$R1 = 2\xi \times \sqrt{\frac{N}{I_{CP} \times K_V \times C2}}$$

6. Determine resistor R2 and capacitor C3

One rule has to be respected for the values of R2 and C3: their product should be at least 1/10 of the R1 with C2 product.

R2 and C3 are used in the loop filter to smooth the possible spurs generated by the reference frequency.

In order to simplify all calculations, we will take:

$$R2 = R1 and C3 = \frac{C2}{10}$$

7. Calculate the loop bandwidth

The loop bandwidth is an interesting parameter giving the bandwidth of the loop filter (band for which the phase noise is constant).

$$LoopBandwidth = f_{LOOP} = \pi \times fn \times \left(\xi + \frac{1}{4\xi}\right)$$

3.2.1.2 Design Parameters Example

Given specifications

- VCO tuning Gain (or sensitivity) KV = 17 MHz / V
- F_{OUT} = 1 GHz
- I_{CP} = 6 mA
- F_{ref} = 20 MHz

Application requirements

- Frequency Range: up to 1 GHz
- Channel spacing = 200 kHz
- Maximum frequency hop = 60 MHz
- Frequency hop time = 500 ms
- Frequency accuracy after hop time = 10 kHz

1. Determining the dividing ratios N and M for the PLL

Considering the equation:

$$N = \frac{VCOFrequency}{ChannelSpacing}$$

We obtain:

$$N = \frac{1GHz}{200KHz} = 5000$$

Then, we can determine the proper M factor:

$F_{OUT} = N / M \times F_{REF}$

$M = 5000 \times F_{REF} / F_{OUT}$

$M = 5000 \times 20\ MHz / 1000\ MHz$

$M = 100$

2. Calculate the natural frequency Fn

$$fn = \frac{-1}{2\pi \times ts \times \xi} \times \ln\left(\frac{fa}{fstep}\right)$$

$$fn = \frac{-1}{2\pi \times 500\mu s \times 0,707} \times \ln\left(\frac{1000}{60 \bullet 10^{6}}\right) = 4953,43Hz$$

3. Determine capacitor C2

$$C2 = \frac{I_{CP} \times K_V}{N \times (2\pi \times fn)^2}$$

$$C2 = \frac{6mA \times 17MHz/V}{5000 \times (2\pi \times 4953,43)^2} = 20nF$$

4. Determine capacitor C1

$$C1 = \frac{C2}{10}$$

$$C1 = \frac{20nF}{10}$$

$$C1 \times 2nF$$

5. Determine resistor R1

$$R1 = 2\xi \times \sqrt{\frac{N}{I_{CP} \times K_V \times C2}}$$

$$R1 = 2 \times 0,707 \times \sqrt{\frac{5000}{6mA \times 17MHz \times 20nF}} = 2,2k\Omega$$

6. Determine resistor R2 and capacitor C3

$$R2 = R1 and C3 = \frac{C2}{10}$$

$$R2 = 2,2k\Omega and C3 = 2nF$$

7. Calculate the loop bandwidth

$$LoopBandwidth = f_{LOOP} = \pi \times fn \times \left(\xi + \frac{1}{4\xi}\right)$$

$$LoopBandwidth = f_{LOOP} = 16504,8Hz$$

3.2.1.3 Board Design Recommendations

If the equations given in the previous section are respected with care, the loop filter design should be optimum. However, it is still subject to external parasitic or inherent parasitic dependent on the choice of the components used.

The VCO and PLL performances are one main point contributing to the overall performance of the clock generator. Nowadays manufacturers offer a wide choice of VCOs and PLLs with high performances.

However, the intrinsic performances of these device will not be of any benefit if special care is not taken with the discrete components for the loop filter but also for the board layout.

As a matter of fact, with regards to discrete components, they have to be of the smallest size (0603 or 0402 size preferably). The capacitors should have a very low leakage and the resistors should be the less noisy as possible.

Concerning the decoupling and bypassing of the power supplies for the VCO and the PLL, it is highly recommended to bypass the power supply lines with capacitors as close as possible to the PLL and VCO. If the VCO and the PLL are supplied by the same VCC, it is recommended to place a resistor of proper value between the PLL and the VCO power supply for isolation. Decoupling capacitors should be implemented for each power supply connection, with a direct connection to the ground plane.

Finally, the board traces should be as short as possible between each device and the ground path between the PLL, loop filter and VCO should be the shortest too. All lines should be with controlled impedance, especially the connection between the VCO and the ADC clock input.

If all these recommendations are followed carefully, one should be able to design a high- speed clock with high immunity to noise performances. Note only that the values given by the theoretical calculations (previous section) may be modified to close values in case of parasitic effects, in order to reach the optimum performances of the overall system.

3.3 VCO/PLL Manufacturers References (For Information only)

Fujitsu Microelectronics	http://www.fujitsumicro.com
Altera®	http://www.alter.com
MAXIM®	http://www.maxim-ic.com
On Semiconductor®	http://www.onsemi.com
MITEL®	http://www.mitel.com

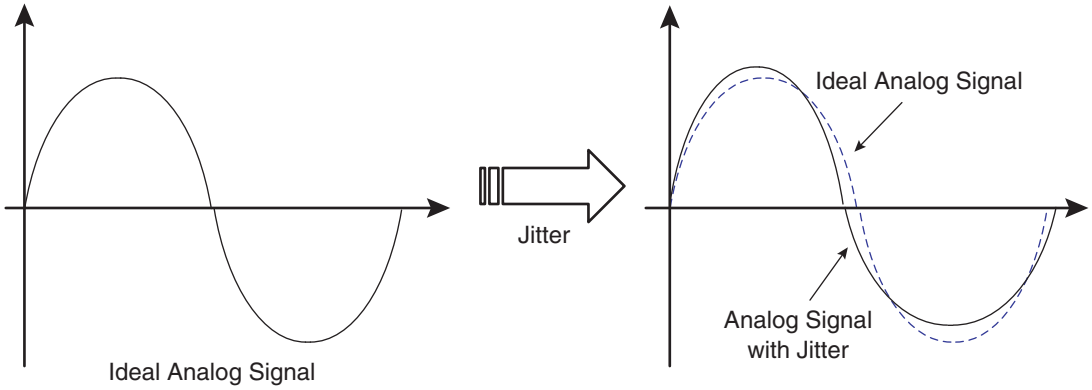
4. Appendix

4.1 Analog Signal Jitter

4.1.1 Empirical Definition

Similarly to the clock jitter, what we define as analog signal jitter can be defined as an uncertainty on the value of the signal at a defined instant. This can be illustrated as follows:

Figure 4-1. Effects of Jitter on the Analog Signal



The analog signal jitter is in fact the consequence of noise and distortion on the analog input signal of the ADC. This noise and distortion are themselves due to a poor transmission of the analog signal, to which noise can be added during propagation.

An real sinusoid analog signal includes two noisy components: the amplitude noise and the phase noise, as depicted below:

Ideal Sine wave: $s_{ideal}(t) = A \sin(\omega t)$

Real Sine wave with amplitude and phase noise: $s_{real}(t) = [A + a(t)] \sin(\omega t + \phi(t))$

With A = Amplitude of the sine wave

ω = pulsation

a(t) = Amplitude Noise

$\phi(t)$ = phase Noise

If we consider the carrier signal now, we obtain the following equation:

$V(t) = [V_0 + P(t)] \sin(\omega_0 t + \phi(t))$

Where:

V_0 = Carrier Amplitude

P(t) = Amplitude Noise

$\phi(t)$ = Phase Noise

In the general case, the amplitude noise is neglected and the equation then becomes:

$V(t) = V_0 \sin(\omega_0 t + \phi(t))$

$V(t) = V_0 [\cos(\omega_0 t)\sin(\phi(t)) + \sin(\omega_0 t)\cos(\phi(t))]$

Assuming $|\phi(t)| << 1$, $\phi(t) \bullet \sin(\phi(t))$ and $\cos(\phi(t)) \bullet 1$, we have then

$V(t) = V_0\ \phi(t) \cos(w_0 t) + V_0 \sin(\omega_0 t)$

This equation show that the signal has then two components: the phase noise term and the desired RF modulated signal respectively.

Phase noise on the analog signal causes, in the frequency domain, spectral leakage and reciprocal mixing.

Spectral leakage refers to the process of distributing the energy of a component in the signal into various components.

Reciprocal mixing is due to the conversion of adjacent channel energy into the desired signal bandwidth.

The other contributions to analog signal jitter are the effects of fading channels and other transmission non-idealities.

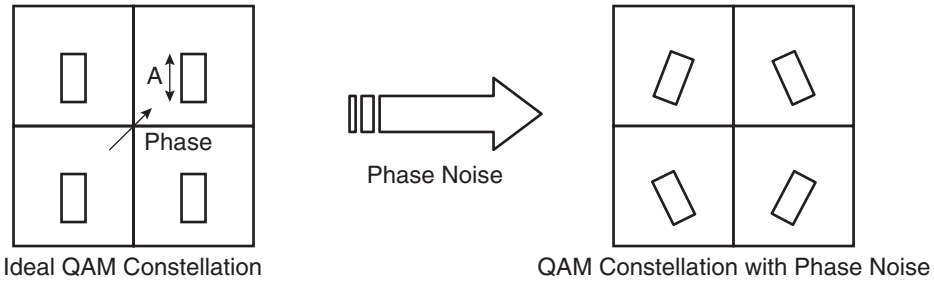
All these contributors to analog signal jitter result on the BER (Bit Error Rate) performance at the output of the ADC and the ACPR (Adjacent Channel Power Ratio) parameter and on the interference specifications, contributing to increase the signal distortion.

4.1.2 Phase Noise Consequences on Complex Modulations Constellations

As underlined previously, the phase noise is present in the carrier signal equation by a non- negligible term. The effects of phase noise are especially observable in complex modulation systems (such as QAM), where the phase noise results in shifts in the position of the constellation points. These shifts have a direct consequence on the bit error rate of the demodulated signals.

The following figure illustrates the effects of phase noise jitter on a QAM constellation:

Figure 4-2. Effects of Phase Noise on a QAM Constellation



4.1.3 HF Signal Propagation Consequences on Signal Noise and Distortion

The main sources of noise on the analog input signal are typically due to the analog signal transmission path. On its path from the transmitter and the receiver end, the analog signal travels through the air and is subject to perturbations such as interferences, reflection, fading or attenuation and refraction.

All these phenomenons induce some alteration on the signal to be transmitted and can be considered at the receiver's end as noise and distortion.

While traveling through the air, the wave is more or less absorbed in the different layers of the sky, for example the ionosphere.

It consequently decreases in energy and arrives somewhat attenuated at the receiver's end.

The refraction of the wave on the ionosphere causes this loss in energy and depends in particular on the angle of radiation, which, itself, depends on the frequency of the signal, the time of year and the time of day.

Whether the signal is transmitted during the day or in night hours, its refraction in the ionosphere will increase or decrease respectively. The seasons also have an impact on the wave propagation.

These were natural factors involved in the attenuation of a signal in the ionosphere.

Other perturbations may come from interferences. These interferences can be induced by other signal transmissions on adjacent frequency channels but also simply by a thunderstorm.

Finally, distortion may also be induced by propagational effects such as the polar echo or fading (selective fading or multipath fading).

4.2 Glossary

Symbol	Term	Definition
ACPR	Adjacent Channel Power Ratio	Ratio of the power spectral density of one channel to its adjacent channel
BER	Bit Error Rate	Probability to exceed a specified error threshold for a sample
BW	Bandwidth	Frequency range found in a given signal
ENOB	Effective Number Of Bits	Effective resolution of the ADC, taking into account the noise and distortion influences on the ADC dynamic performances
PLL	Phase Locked Loop	
QAM	Quadrature Amplitude Modulation	Amplitude Modulation scheme, where the points are mapped in a quadratic constellation
RADAR	Radio Detection And Ranging	Device, which measures the strength and round-trip time of the microwave signals that are emitted by an antenna and reflected off a distant surface or object
SFDR	Spurious Free Dynamic Range	Ratio of the RMS signal amplitude to the RMS value of the next highest spectral component (peak spurious spectral component)
SINAD	Signal to Noise and Distortion Ratio	Ratio of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics, except DC
SNR	Signal To Noise Ratio	Ratio of the RMS signal amplitude to the RMS sum of all other spectral components, excluding the first 5 harmonics
SSB	Single Side Band	Upper or Lower side band of a modulated signal
THD	Total Harmonic Distortion	Ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured fundamental spectral component
VCO	Voltage Controlled Oscillator	

4.3 References

ESG-AP Series Agilent Signal Generators Data sheet.

MB15E07SL “Single Serial Input PLL Frequency synthesizer On-chip 2.5GHz prescaler” Data sheet, Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc., “PLL Basics - Loop Filter Design”.

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